Journal of the Korean Physical Society, Vol. 75, No. 6, September 2019, pp. 471∼475

# Effect of Contact Resistance on the High-Field Characteristics of $MoS_2$ Transistors

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(Received 18 July 2019; revised 25 July 2019; accepted 25 July 2019)

Layered transition metal dichalcogenides (TMDs) display a wide range of unique electronic properties and are potentially important for electronic device applications. Much interest in these materials led to in-depth research on the device properties of TMDs such as $MoS_2$. Unlike graphene, this material has a relatively large band gap (1.3–1.9 eV) and exhibits stable on/off switching as a transistor. TMD materials represent ideal channel materials for device scalability as their few-atom-thick layers devoid of dangling bonds will be robust against short-channel effects for ultrathin channeled transistors. As $MoS_2$ devices are scaled down, robust high-field operation is essential for the development of reliable electronic systems. In this work, we explore the high-field characteristics of $MoS_2$-based transistors and investigate their relationship to the contact resistance. Importantly, we show that high-voltage characteristics, current drives, and breakdown voltages of $MoS_2$ transistors can be significantly improved through the use of a metal-insulator-semiconductor contact at the metal/$MoS_2$ interface.

PACS numbers: 73.63.−b, 73.40.Cg, 73.40.Qv
Keywords: $MoS_2$, Transistor, High-field
DOI: 10.3938/jkps.75.471

## I. INTRODUCTION

Two-dimensional materials such as graphene and $MoS_2$ with their unique physical properties have garnered great interest in the scientific community. Graphene, due to its lack of a bandgap, has limitations in electronic applications [1]. On the other hand, semiconducting 2D materials such as $MoS_2$ retain a relatively large bandgap (1.3–1.9 eV) [2] and show promise in the area of ultrathin channel devices and electronics. Although transition metal dichalcogenides (TMDs) exhibit excellent intrinsic properties for device scaling, smaller devices are commonly exposed to increased electrical fields, and the reliability of these materials at high-fields is relatively less known [3]. This study is especially important for layered TMDs for several reasons. First, creating high-quality, low-resistance contacts to semiconducting TMDs have proven to be more challenging due to Schottky barrier formation [3,4]. A conventional substitutional doping method for decreasing the contact resistance of bulk semiconductors is not suitable for TMDs as doping impurities introduce large strain to the lattice, as well as additional defect sites that lower the carrier mobility [5]. Hence, the high-resistance contacts work as joule heating sources during high-field operation [6]. Second, the conventional understanding of punch-through that relies on the traditional source/drain depletion region model does not apply to TMD channeled transistors because the conventional depletion region model does not apply low dimensional materials [7]. Last, the characterization of TMD transistors at high-fields is important because it is directly related to the ultimate scaling limit and the reliability of these materials as ultrathin transistor channels [8].

In this work, we investigate how the high voltage characteristics of $MoS_2$ transistors can be improved by using a metal-insulator-semiconductor (MIS) contact structure that lowers the contact resistance at the metal/$MoS_2$ interface [9, 10]. We also show how this method increases the current drives and the breakdown voltages of $MoS_2$ transistors. In order to understand the effect of the MIS contact in a high-field environment, we synthesize $MoS_2$ by using chemical vapor deposition (CVD) and fabricate n-type transistors in a transmission-line-measurement (TLM) structure to investigate the device characteristics [11]. $MoS_2$ was chosen as the testing material because of its relative large bandgap and stability

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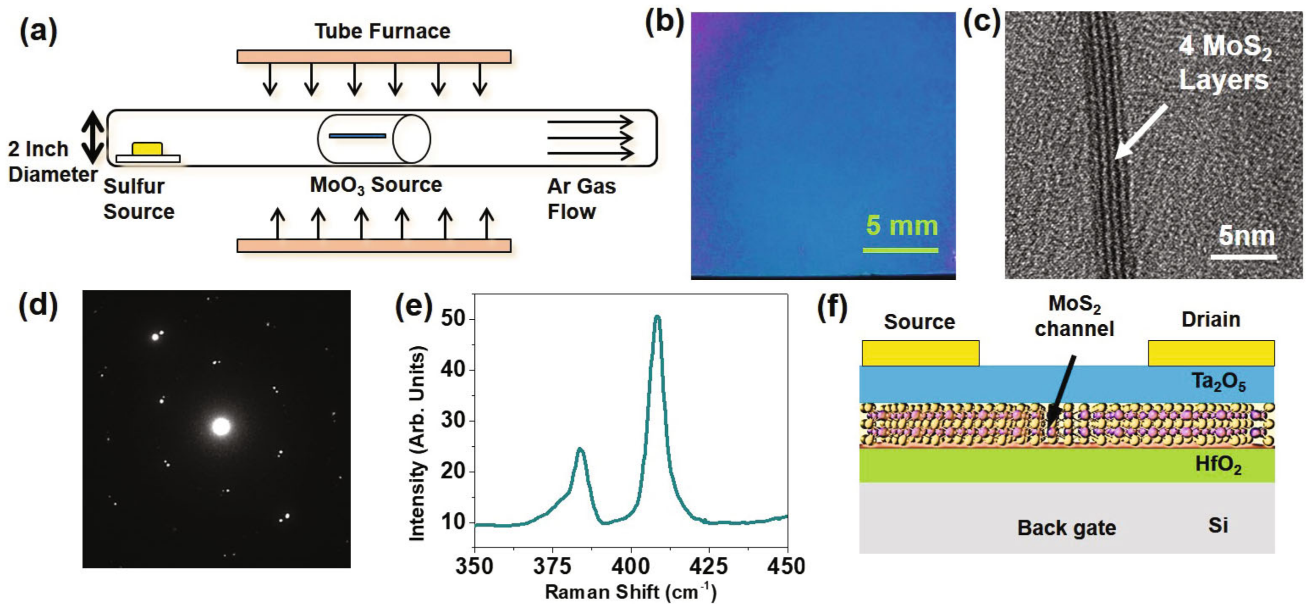


Fig. 1. (Color online) (a) Illustration of the $MoS_2$ CVD synthesis process, (b) microscope image of CVD-synthesized $MoS_2$ on a $SiO_2$ substrate, (c) TEM image of the $MoS_2$ edge, (d) selected area electron diffraction (SAED) pattern of the $MoS_2$ film, (e) typical Raman spectrum of the synthesized $MoS_2$ film, (f) illustration of fabricated $MoS_2$ transistors with a Si back gate and a $Ta_2O_5$-based MIS contact.

in ambient as a transistor channel material [12].

$MoS_2$ suffers from a large contact resistance at the semiconductor/metal contacts, which is attributed to Schottky barriers [4,9,13] and Fermi level pinning [13, 14] upon band alignment. While previous reports have reported that gold contacts to $MoS_2$ are ohmic [12,15], the linear relation is limited to the low voltage regime. Many subsequent reports confirm the existence of sizeable Schottky barriers at the contacts [4,9,13]. Experimental evidence of Fermi level pinning also has been identified, and the pinning is believed to be caused by gap state formation [14]. The resulting high barrier is the main cause for the large voltage drop and the joule heating at the $MoS_2$/metal contact and may lead to significant drops in reliability and performance of $MoS_2$-based devices in a high-field environment.

Various techniques have previously been used to reduce the contact resistance of TMD transistors. Low work function metals have been used as contact metals to improve the alignment between the conduction band edge and the metal work-function [13]. Chemical adsorption techniques, such as the use of $NO_2$ gas ambient [16] or potassium ions [17] to dope contact regions of $WSe_2$-based devices, have been shown to reduce the contact resistance. However, air stability is a major issue with these techniques because low work-function metals are susceptible to oxidation [18]. Similarly, the adsorbed chemical species may desorb from the surface and react with oxygen and water molecules upon prolonged exposure to ambient air [19,20]. Patterning the $MoS_2$ to a metallic 1T phase to exclude the semiconducting 2H phase at the contact is another technique that can reduce the contact resistance [15]. However, that technique requires flake samples to readily identify the phase direction and may not be viable for large-area CVD films.

## II. EXPERIMENTS AND DISCUSSION

An air-stable technique to reduce the contact resistance is to use metal?insulator?semiconductor (MIS) contacts, which are formed by inserting a thin, tunneling insulator between the metal and the semiconductor. Such a method has previously been shown to reduce the Schottky barrier height of metal contacts to Si [21], Ge [22], III-V materials [23,24], and $MoS_2$ [9,10,25]. The barrier height reduction in these MIS structures has been attributed to the attenuation of metal-induced gap states (MIGS) [26,27] in the insulator and/or dipole formation [28] at the insulator-semiconductor interface. In order to investigate the effect of the MIS structure on $MoS_2$ contacts, we fabricated $MoS_2$ transistors with a thin (15 Å) layer of insulator inserted between the metal contact and the $MoS_2$.

More than one hundred $MoS_2$ devices were fabricated and tested for large scale statistical analysis. Few-layer $MoS_2$ was synthesized on $SiO_2$ via the CVD method (Fig. 1(a)). The details of the CVD process have been reported elsewhere [11]. Although large-scale CVD syntheses of both monolayer and multilayer $MoS_2$ are possible, multilayer (four-layer) $MoS_2$ was used in this work because multilayer $MoS_2$ was found to have a lower contact resistance and a higher on-current. This is in agreement

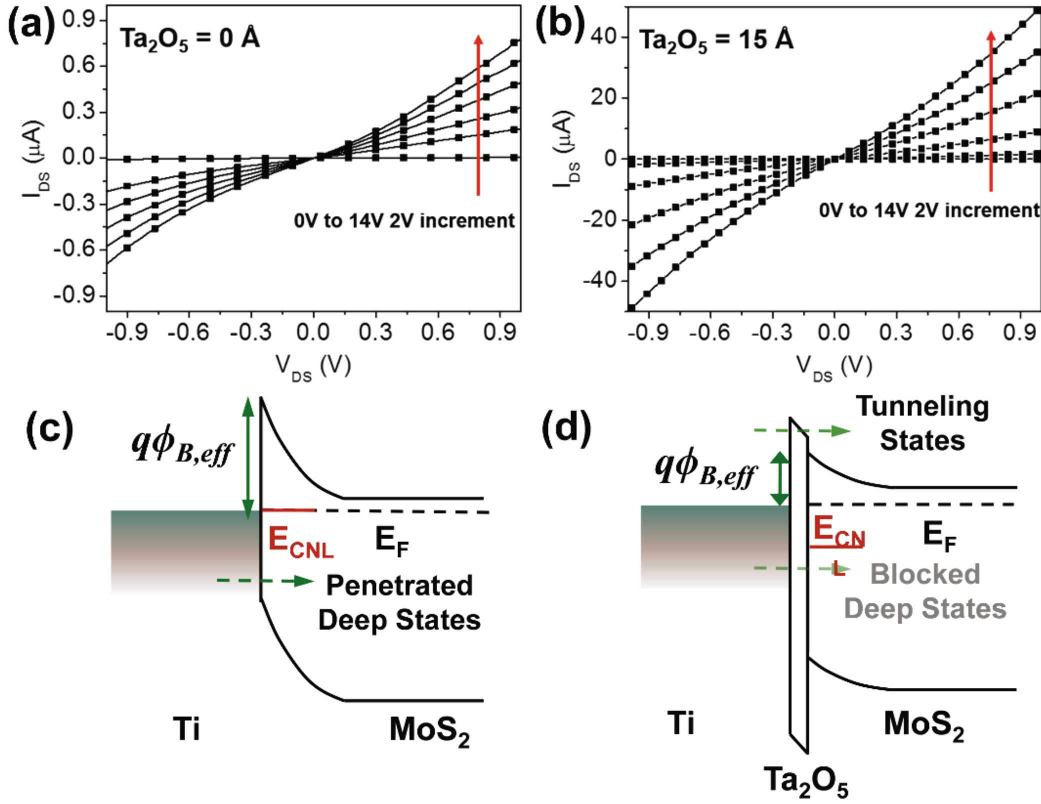


Fig. 2. (Color online) Gate controlled current drive at a low drain-source bias (a) without and (b) with the $Ta_2O_5$ tunneling layer at the contact. The energy band diagram at the contact (c) without and (d) with the $Ta_2O_5$ tunneling layer.

with several reports claiming that multilayer TMDs have higher mobility [13,29] and lower contact resistance [30] due to suppression of both interfacial Coulomb impurity scattering and the quantum confinement effect.

An optical image of the synthesized film is shown in Fig. 1(b). The number of layers was verified using Raman spectroscopy (Fig. 1(e)) and transmission electron microscopy (TEM) (Fig. 1(c)). The distinctive Raman spectrum of multilayer $MoS_2$ with two peaks, one at 385 $cm^{-1}$ (in-plane mode, $E_{2g}$) and the other at 407 $cm^{-1}$ (out-of-plane mode, $A_{1g}$), is shown clearly in Fig. 1(e). The Raman peak frequency difference between the $A_{1g}$ peak (407 $cm^{-1}$) and the $E_{2g}$ peak (385 $cm^{-1}$) was found to be 22 $cm^{-1}$, indicative of 4–5 layer $MoS_2$ according to literature [31]. The selected area diffraction pattern using TEM (Fig. 1(d)) taken from areas 1 $\mu$m in diameter shows high-quality crystalline $MoS_2$ with two domains rotated by about 5°, suggesting that the typical domain size is about 1 $\mu$m. An illustration of the transistor structure is shown in Fig. 1(f). The transistors were formed by etching $MoS_2$, followed by Ti/Au contact metallization and $Ta_2O_5$ (15-Å thick) deposition. $Ta_2O_5$, which was deposited using an atomic layer deposition technique, was selected as the tunneling insulator layer because of its low conduction band offset to $MoS_2$.

A large difference in drain currents was observed when we compared devices with and without the $Ta_2O_5$ layer. Typical gate responses of the two structures, one with (Fig. 2(a)) and the other without (Fig. 2(b)) the $Ta_2O_5$ layer between $MoS_2$ and the contact metal, are shown. At least an order of magnitude increase in drain current was observed in transistors with the 15 Å of $Ta_2O_5$ between $MoS_2$ and the Ti/Au contact. As reported in many previous papers in the literature, such increase in drain current is attributed to a contact barrier height reduction caused by the attenuation of metal-induced gap states in the insulator (Figs. 2(c) and 2(d)) [9,10].

Top-down views of the transmission-line-measurement (TLM) structures and the final transistors are shown in Fig. 3(a). Channel widths were fixed at 60 $\mu$m and the lengths were varied (0.5, 1, 2, 3, 4, 5 $\mu$m) to form a TLM structure. To investigate the effects of the MIS contacts on the breakdown voltages for the transistors, we measured the drain-source voltage at zero gate bias required to reach various current levels for different channel lengths. Figures 3(b), 3(c), and 3(d) show the $V_{DS}$ values (at zero gate bias) required to reach $I_{DS}$ currents of 10 nA, 100 nA, and 1 $\mu$A, respectively, as functions of the transistor's channel length. The $y$-intercept of each plot corresponds to the contact resistance value $R_c$ multiplied by the $I_{DS}$ current. The slope of the linear fit corresponds to the breakdown voltages per channel length for a given current value. As expected, the $y$-intercepts (*i.e.*, the contact resistances) of the transistors with MIS

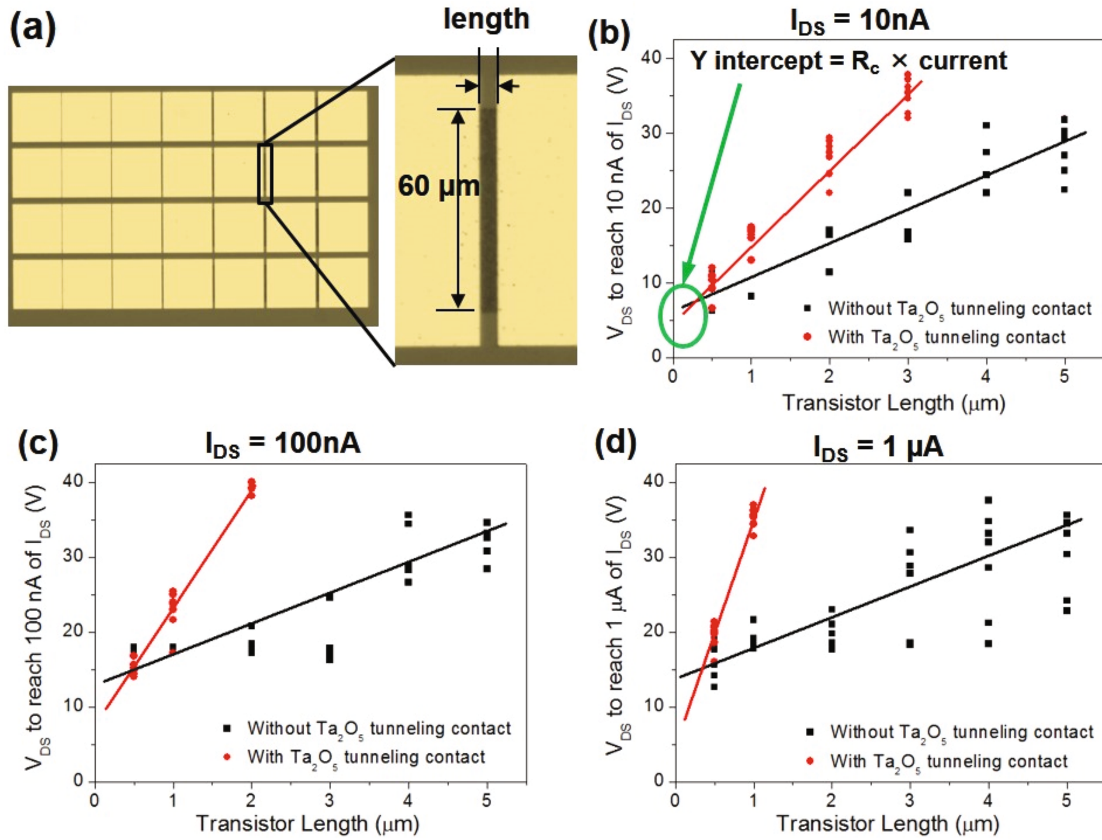


Fig. 3. (Color online) (a) Bird's eye view of the $MoS_2$ transistors fabricated in a transmission line measurement structure, $V_{DS}$ required to reach off drain current level of (b) 10 nA, (c) 100 nA, and (d) 1 $\mu$A with zero gate bias as a function of the channel length.

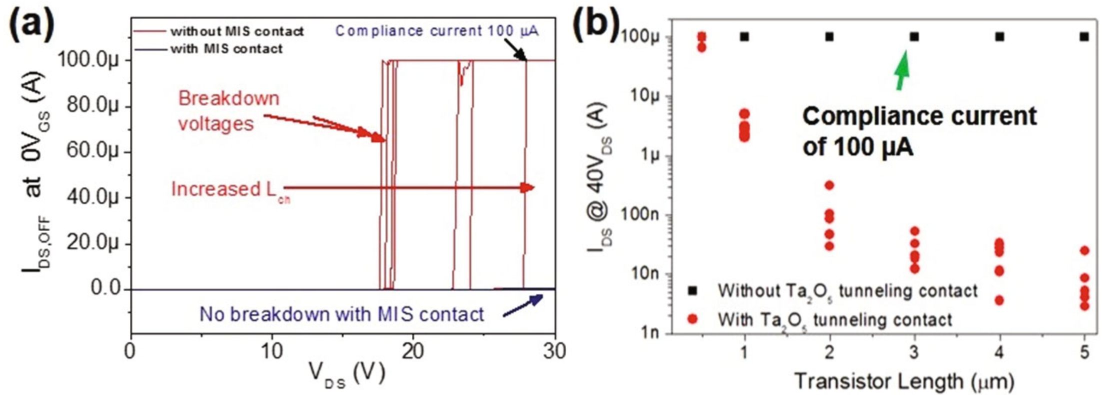


Fig. 4. (Color online) (a) Drain-source currents and breakdown voltages of $MoS_2$ devices with and without $Ta_2O_5$ MIS contacts at various channel lengths $L_{ch}$, (b) Drain-source current as a function of the transistor channel length at a 40 $V_{DS}$ bias with zero gate bias with and without a $Ta_2O_5$ MIS contact.

contacts (shown in red) are much lower than those of the transistors without MIS contacts (shown in black). More importantly, the transistors with the MIS contacts also exhibit higher breakdown voltage per channel length compared to those without the MIS contact. This is counter-intuitive because the MIS structure lowers the contact resistance and the voltage drop across the contact, which will lead to higher voltage drop across the $MoS_2$ channel. We believe devices with MIS contacts can withstand higher voltages because of the lower barrier and the lower Joule heating at the contact interface. The breakdown mechanism is due to three main contributions: the thermal instability, the tunneling effect, and avalanche multiplications [32,33]. With the reduction in

the contact resistance, the overall resistance is lowered in the transistor, as is the power dissipation and the Joule heating. Lower Joule heating also leads to a lower off $I_{DS}$ current. This results in improved thermal stability since more off current is again responsible for additional heating and avalanche multiplication.

To verify that the transistors are more robust at high-fields, we plot in Fig. 4(a) $I_{DS}$ (at 30 V $V_{DS}$, 100 $\mu$A compliance limit, zero gate bias) as a function of the channel length. We observed that all transistors without MIS contacts suffered from avalanche breakdown before a 30 $V_{DS}$ bias (zero gate bias) while the devices with MIS contacts did not. We also measured the off $I_{DS}$ current when the $V_{DS}$ bias reached 40 V and found that significantly less off-current flowed for devices with MIS contacts, as presented in Fig. 4(b).

## III. CONCLUSION

In summary, we report a significant increase in the drain-source breakdown bias and a decrease in the off current of ultrathin 2D transistors with a thin insulating layer inserted at the metal-semiconductor interface. We also report an improvement of at least an order of magnitude in the current drive in the presence of MIS contacts. We attribute these improvements to reductions in the height of the contact barrier and in the contact resistance. TMD materials such as $MoS_2$ have relatively large band gaps and are known to support very high current densities, exceeding the current-carrying capacity of copper by a factor of 50 [32]. This material is also known to be highly robust in mechanically strained environments [34]. Such properties have important implications for future applications such as ultrathin electronic system that can be used in wearable technology, flexible displays and stretchable electronics. The application of the MIS contact to the $MoS_2$ transistor is an efficient and simple method to improve the high-field reliability of such a system.

## ACKNOWLEDGMENTS

This work was supported by grants from Kyung Hee University in 2016 (KHU-20160609) and by National Research Foundation of Korea (NRF) grants funded by the Korea government (No. 2017M1A7A1A01016262) and (No. 2017R1C1B2012227). This work was also supported by the Technology Innovation Program (or Industrial Strategic Technology Development Program (No. 1008 5646, Memristor Fault-Aware Neuromorphic System for 3D Memristor array) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea). This research was also supported by the Basic Science Research Program through the NRF funded by the Ministry of Education (grant No. 2018R1A6A1A03025708, Study on integrated multifunctional sensor platforms based on autonomous energy).

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