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# Organic Memory Device with an Organic Memory Layer of Plasma Polymerized Styrene

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A floating-gate-type organic memory device was designed and fabricated by modifying a thin- film transistor structure. Thin films of plasma-polymerized methyl methacrylate (ppMMA) and plasma-polymerized styrene (ppS) were prepared for use as the functional thin film in an organic memory device. The ppMMA thin film was utilized as both an insulating and a tunneling layer. Two types of memory layers were utilized: (1) ppS and (2) vacuum evaporated Au. The fabricated devices were examined by using current-voltage measurements made using the double-sweep procedure. The memory window and the retention time of the memory devices were comparatively investigated. The device with the ppS memory layer revealed a memory window of 19 V and showed a retention time of over 2 h. We confirmed that ppS could be utilized as a memory layer for a floating-gate-type organic memory device.

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## I. INTRODUCTION

Semiconductor devices have been introduced to diverse industrial applications. Modern science and technology is focusing on the new paradigm of ubiquitous-mobile electronics, and so-called 'soft-electronics' are of great importance for wearable and flexible applications. Memory devices for storing electronic information are also inevitable because of needs and trends. Memory devices can be categorized as either volatile or non-volatile. Data stored in non-volatile memory can be sustained for a desired time even after cut-off of electric power.

Although inorganic flash memories have been successfully developed and commercialized, they are hardly adaptable for flexible computing. Organic semiconductors are inherently flexible in nature, so they could be used for flexible applications. Organic non-volatile memory transistors (ONVMTs) are a promising concept for the realization of organic memory devices because of their relatively easy device structure. Enhancement and optimization of performance for ONVMTs can be accomplished by material selection and by improving the memory layer and the tunneling layer [1–5]. A shift in the threshold voltage due to charge storage should be a key parameter for deciding the performance of ONVMTs, and the extent of the threshold-voltage shift is defined as the memory window [6].

A general trend for the preparation of organic electronic devices is to use a solution-based wet process aiming for low-cost and large-area fabrication. However, the performances and long-term of wet-processed organic electronic devices still have not been satisfactory. Modification of existing vacuum processes may still be advantageous from the viewpoint of the long-term stability of organic electronic devices. A completely dry

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Table 1. Process parameters for plasma-polymerized thin film of MMA or styrene.

| Monomer | MMA | Styrene |
|---|---|---|
| RF Power | 100 W | 100 W |
| Pressure | 5 mTorr | 10 mTorr |
| Substrate Position | 100 mm | 50 mm |
| Monomer Gas Flow | 20 sccm | 30 sccm |
| Substrate Bias | RF 20 W | RF 30 W |
| Substrate Temperature | RT | RT |

process was carried out in this research for the fabrication of a floating-gate-type organic memory device. Plasma-enhanced-chemical vapor deposition (PECVD) technology for polymers has been successfully applied to functional organic devices such as organic thin-film transistors (OTFTs) [7,8] organic light-emitting diodes (OLEDs) [9,10] and floating-gate type organic memory devices [11,12].

Plasma polymerized polymer thin films of plasma-polymerized methyl methacrylate (ppMMA) and plasma-polymerized styrene (ppS) were prepared by a PECVD process based on an inductively coupled plasma (ICP) source. The ppMMA thin films were applied to floating-gate-type organic memory device as a gate insulator, as well as a tunneling, layer. The ppS thin film was utilized as a memory layer for the organic memory device. A *p*-type organic semiconductor of pentacene was prepared by using the vacuum evaporation technique and was used as the active layer. As source and drain contacts, Au thin films were deposited by using vacuum evaporation through a shadow mask. To examine the performance of the ppS-based organic memory device, we also prepared a reference organic memory device with the same component layers except for the memory layer, a 7-nm-thick Au thin film. The performances of the floating-gate-type organic memory devices were evaluated by measuring the current-voltage ($I$-$V$) characteristics, from which key parameters, the hysteresis voltage, the memory window and the retention time were obtained. The manufacturing process used in this works for all organic thin films can be applied to a completely dry process for ONVMT fabrication. In addition, the feasibility of the ppS thin film as a memory layer for a flexible, floating-gate-type organic memory device is checked.

## II. EXPERIMENTAL METHODS

### 1. Fabrication of the floating-gate-type organic memory device

A modified structure of organic thin film transistor was designed for fabrication of a floating-gate-type organic memory device, where an additional tunneling layer (ppMMA) and a memory layer (ppS or Au) were inserted between the organic active layer and the organic gate insulator. In this research, the ppMMA and the ppS thin films were prepared by using PECVD with an ICP-based plasma-polymerization deposition process, where vaporization of the organic monomers was precisely controlled directly by using a designed bubbler system with temperature stability and a flow that could be controlled using a mass flow meter (MFC) [11].

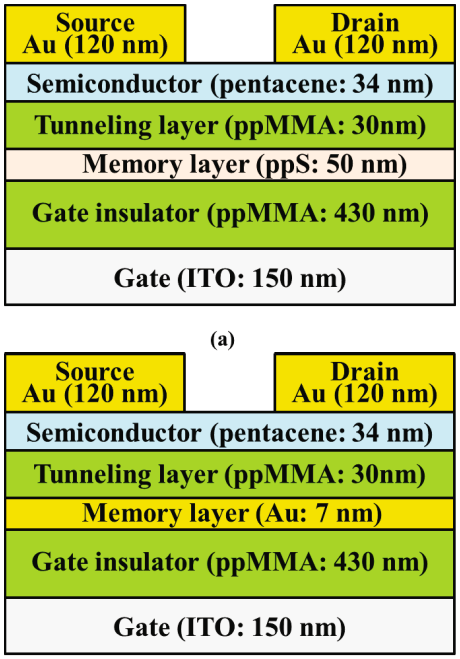


Fig. 1. (Color online) Structure of the floating-gate type organic memory: (a) ppS memory layer and (b) Au memory layer.

An ITO-coated glass substrate was used for the fabrication of floating-gate-type organic memory device, where the ITO could play the role of a gate electrode for the device. Firstly, the ITO-coated substrate was cleaned ultrasonically and was dried using conventional procedures. To minimize the leakage current to gate electrode, we selected the representative organic insulator MMA [13–15]. Table 1 presents the essential process parameters for the preparation of the ppMMA and the ppS thin films. The 430-nm-thick ppMMA thin film was prepared by using the ICP-based PECVD technique: plasma power of RF 100 W; Ar (carrier gas) flow rate of 20 sccm; working pressure of 5 mTorr; substrate bias of RF 20 W; substrate temperature of room temperature (RT). Then, a memory layer of 50-nm-thick ppS was deposited by using the PECVD technique: plasma power of RF 100 W; Ar flow rate of 30 sccm; working pressure of 10 mTorr; substrate bias of RF 10 W; substrate temperature of RT. Another memory layer of 7-nm-thick Au was prepared for a reference device by using thermal

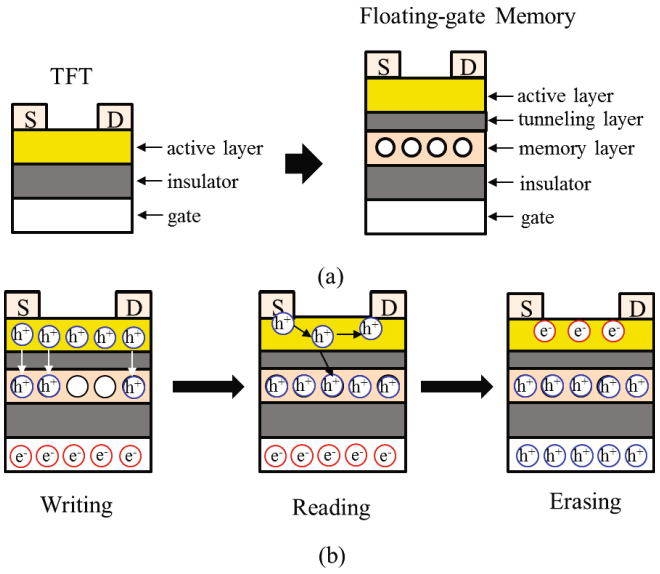


Fig. 2. (Color online) Schematics of floating-gate-type memory device: (a) structure and (b) operation principle.

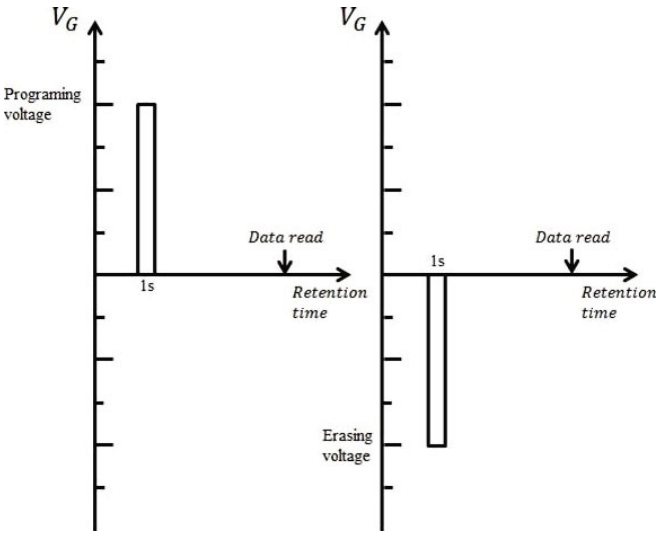


Fig. 3. Concept of the retention of time for an organic memory device [2].

evaporation with a deposition rate of 0.1 Å/sec. Then, a 30-nm-thick ppMMA layer was deposited as a tunneling layer on top of the ppS or Au memory layer. An organic active layer of pentacene was then deposited on each of the memory layers by using thermal evaporation in vacuum: deposition rate of 0.3 Å/sec. Finally, source/drain contact electrodes were formed by thermal evaporation to deposit a Au thin film (100 Å/sec) through a shadow mask: channel length of 0.1 mm; channel width of 1 mm. Figure 1 shows schematics of the two floating-gate-type organic memory device: (a) device with a ppS memory layer and (b) device with a Au memory layer. Except for the memory layer, both devices have the same component layers.

## 2. Characterization of the floating-gate-type organic memory device

A floating-gate-type organic memory device was prepared using an extended modification of the OTFT structure, where a thin memory layer and tunneling layer were inserted between the active channel layer and the insulator layer. Figure 2(a) presents schematics of the TFT and the floating-gate-type memory. The operation of the floating-gate-type organic memory can be explained using the specific operation scheme of an OTFT. Figure 2(b) shows those operation principles with three modes: programming, reading and erasing. For a *p*-channel TFT, holes are stored or erased by means of the applied gate voltage, and a hysteresis characteristic is induced in the *I-V* characteristic curve of the TFT. The hysteresis leads to a shift in the threshold voltage, which, in turn, results in two different states, programming (1) and erasing (0) [1]. If the gate of a *p*-channel TFT is biased by a voltage negatively larger than the programming (or writing) voltage, then the majority charge carriers of holes are stored in the memory layer. The holes stored in memory layer can not return to the active channel layer due to thin, but highly insulating, tunneling layer, and the states storing holes are sustained. A 'reading (1)' procedure for the 'programming state' can be carried out to measure the source-to-drain currents: for example, gate biased with a voltage negatively larger than the programming voltage and drain negatively biased compared the source. An 'erasing (0)' procedure can be carried out by biasing the gate with a voltage positively larger than the 'erasing' voltage, which results the in movement of holes stored in the memory layer back to the active channel layer.

*I-V* measurement using the double-sweep procedure was carried out for the characterization of the floating-gate-type organic memory devices, from which the key parameters of the device were obtained: (1) hysteresis voltage; (2) memory window; (3) retention time. A combination of source measurement units (SMUs) was utilized for the *I-V* measurement: Keithely 2400 and Keithely 236. The double sweep voltage ($V_{GS}$) was applied to gate by using the Keithely 2400 at a fixed drain/source bias ($V_{DS}$) of $-15$ V, and the drain current ($I_{DS}$) variation with the gate voltage was measured by using the Keithely 236. Four double-sweep procedures were carried out for each device with different voltage range: (1) $-20 \sim +20$ V; (2) $-30 \sim +30$ $V$; (3) $-40 \sim +40$ V; (4) $-50 \sim +50$ V. The hysteresis in the *I-V* characteristic curve was investigated during the double sweep process to examine the charge-storage property in the floating-gate-type organic memory devices. The extent of hysteresis for different charge-storage statuses in memory layer was defined as the hysteresis voltage [11]. A

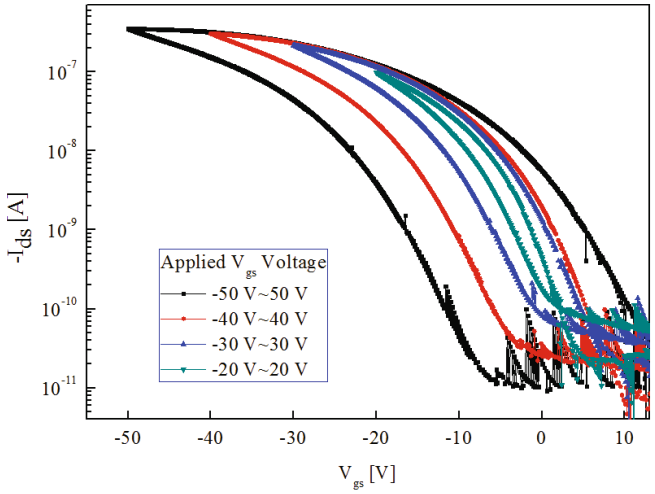


Fig. 4. (Color online) Hysteresis characteristic of the floating-gate-type organic memory device with a Au memory layer.

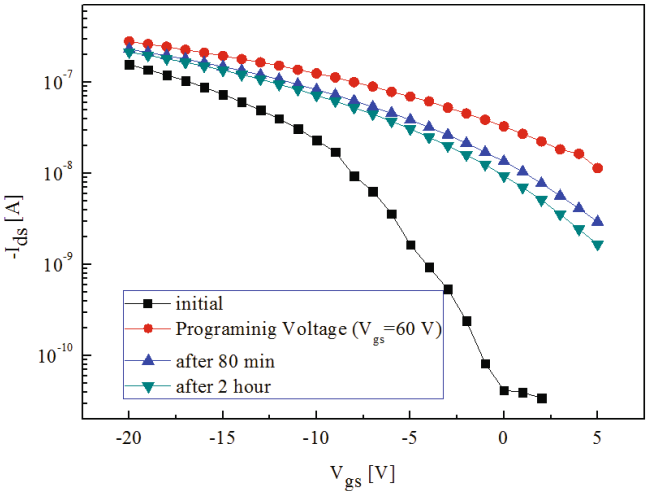


Fig. 6. (Color online) Retention time of the floating-gate type organic memory device with Au-memory-layer.

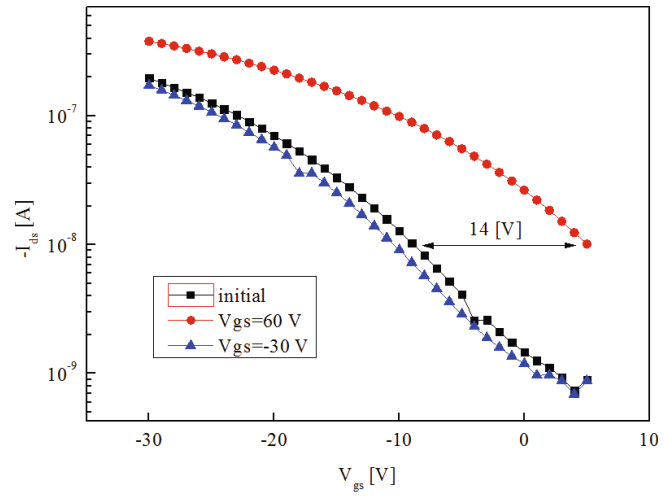


Fig. 5. (Color online) Memory window of the floating-gate-type organic memory device with a Au memory layer.

small step increment (0.1 V) in the $V_{GS}$ was adopted for the double sweep procedure so that the hysteresis variation could be captured for fine variations of the gate bias. Followed by the measurement of hysteresis voltage, a programming voltage was applied to gate. Then, an erasing voltage was applied to the gate, for which the drain current returned to its initial level. The *I-V* characteristic curves were examined for two condition of the gate bias: (1) programming voltage; (2) erasing voltage. The difference in the threshold voltages ($V_{th}$) for the *I-V* characteristic curves was defined as the memory window, which reflects the performance of floating-gate-type organic memory device [6]. Finally, the time during which the charge-storage status was sustained between the programming and the erasing voltage, which was defined as retention time was examined. Figure 3 demonstrates the concept of the retention time for an organic memory device [2].

## III. RESULTS AND DISCUSSION

Floating-gate type non-volatile organic memory devices were fabricated by using plasma polymerized organic polymer thin films as insulator, tunneling, and memory layers. A reference device was also fabricated by using a representative memory layer of a Au thin film. For all the devices, a *p*-type organic semiconductor of pentacene was utilized as the active channel layer.

### 1. Floating-gate type organic memory device with a Au-memory-layer

The data for the performance parameters, *i.e.*, the hysteresis voltage, memory window, and the retention time, are presensted in Figs. 4, 5, and 6 for the reference device with a Au memory layer (Fig. 1(b)), respectively. The insulator layer of ppMMA in the device revealed a superior breakdown voltage of over 3.0 MV/cm and a dielectric constant of 3.75 [11]. The extent of the hysteresis voltage (Fig. 4) in the *I-V* curve was larger when a higher double-sweep voltage was applied to the gate. The higher gate bias can be thought to result in a larger extent of the hysteresis voltage, which depends on the difference in charge-storage state due to the effects on the positive and negative gate biases. The memory window (Fig. 5) of the device was obtained from difference in the drain currents for the programming (+60 V) and the erasing (−30 V) voltages. The difference in the drain current can be thought to originate the LUMO levels of pentacene (semiconductor) and ppS (insulator) being larger than their HOMO [16]. Figure 5 showed that the

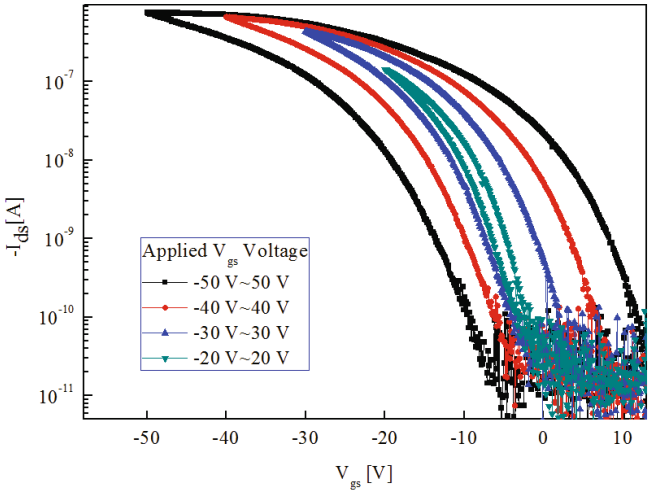


Fig. 7. (Color online) Hysteresis characteristics of the floating-gate-type organic memory device with a ppS memory layer.

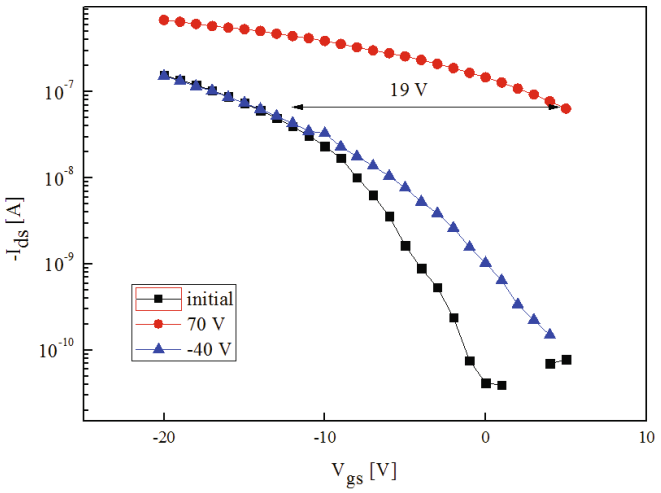


Fig. 8. (Color online) Memory window of the floating-gate-type organic memory device with a ppS memory layer.

reference device with a Au memory layer has a memory window of 14 V for the voltage setup of programming and erasing. The data-storage capability is another key performance parameter for non-volatile memory devices. The time-varying progress of the data storage for the reference device with a Au memory layer was examined by investigating the retention time, where the drain current variation was measured after having applied a programming voltage of +60 V. Figure 6 presents the retention time characteristic of the reference device with a Au memory layer. When the programming voltage is applied, the drain current decreases slightly with time, but that tendency was attenuated conspicuously after a specific time at the drain current stabilized. The reference device revealed that stored charges could be sustained at a constant level for over 2 h after having applied the programming voltage [2].

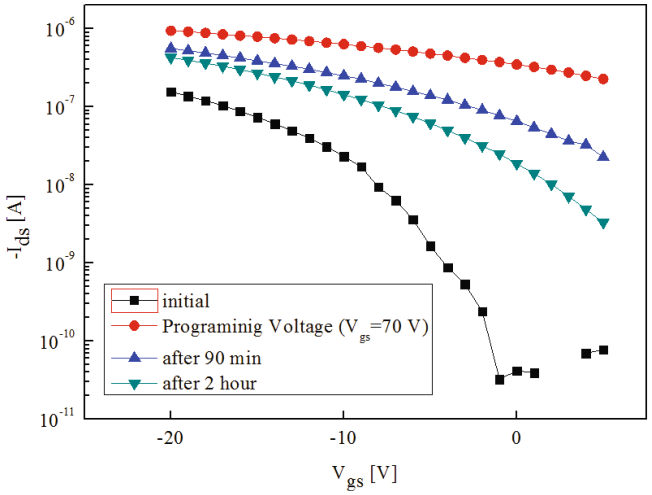


Fig. 9. (Color online) Retention time of the floating-gate-type organic memory device with a ppS memory layer.

### 2. Floating-gate-type organic memory device with a ppS memory layer

Data for the performance parameters, *i.e.*, the hysteresis voltage, memory window, and retention time, are presented in Figs. 7, 8, and 9 for the device with a polymer memory layer of ppS, where all the components are based on organic materials except for the gate and the source/drain electrodes. Polystyrene (PS) has been used as insulating layer due to its excellent insulating properties, and the charge-storage property of PS has been reported recently [17]. The ppS thin film prepared by an ICP-based PECVD process revealed a reasonable breakdown voltage of 1.5 MV/cm and a dielectric constant of 4.8, which were relatively higher than those of PS prepared by using a conventional wet process [1]. Focusing on the charge-storage property of PS, we verified the feasibility of using ppS (50 nm) as a memory layer in a floating-gate-type organic memory device (Fig. 1(a)). It is either feasible regardless of any comparison. Figure 7 shows extent hysteresis characteristics for four different setups of the double-sweep voltage. Similar to the case of the reference device (Fig. 4), the extent of the hysteresis voltage was larger when a higher double-sweep voltage was applied to the gate. The hysteresis voltage for each double sweep procedure is given in the inset in Fig. 7. The results implied that ppS could be used as a memory layer for a floating-gate-type organic memory device. Figure 8 reveals that the memory device with a ppS memory layer has a memory window of 19 V, which is slightly larger than that (14 V, Fig. 5) of the reference device with a Au memory layer. Moreover, the memory device with a ppS memory layer revealed a retention time of over 2 h. All of these properties indicate that ppS can be utilized as a memory layer for a floating-gate-type memory device.

## IV. CONCLUSION

A functional organic memory device with a memory layer of ppS was designed and fabricated on the basis of an organic thin-film transistor, and the performance of the ppS-based organic memory device was comparatively examined using a reference device with a memory layer of a Au thin film. The plasma polymerization deposition process was utilized for the fabrication of the organic polymer layers of ppS and ppMMA. We confirmed that the ppMMA could be used as both a tunneling and an insulating layer in the organic memory device, and reasonable key parameters of an organic memory device was obtained: hysteresis voltage, memory window, and retention time. The organic memory device with a memory layer of ppS showed a memory window of 19 V that was similar to that (14 V) of the organic memory device with a memory layer of Au thin film. Moreover, the organic memory device with a memory layer of ppS revealed a retention time of over 2 h. The key parameters of the ppS-based organic memory device confirmed that the plasma-polymerization deposition process could be used for the fabrication of a functional organic memory device and that ppS could be utilized as a memory layer for an OTFT-based organic non-volatile memory transistor.

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