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Electrical Transport Measurements and Degradation of Graphene/n-Si Schottky Junction Diodes

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We report on the electrical properties, such as the ideality factors and Schottky barrier heights, that were obtained by using current density - voltage ($J-V$) and capacitance - voltage ($C-V$) characteristics. To fabricate circularly- and locally-contacted Au/Gr/n-Si Schottky diode, we deposited graphene through the chemical vapor deposition (CVD) growth technique, and we employed reactive ion etching to reduce the leakage current of the Schottky diodes. The average values of the barrier heights and the ideality factors from the $J-V$ characteristics were determined to be ∼0.79 ± 0.01 eV and ∼1.80 ± 0.01, respectively. The Schottky barrier height and the doping concentration from the $C-V$ measurements were ∼0.85 eV and ∼1.76 × 10^{15} cm^{-3}, respectively. From the $J-V$ characteristics, we obtained a relatively low reverse leakage current of ∼2.56 × 10^{-6} mA/cm^{-2} at −2 V, which implies a well-defined rectifying behavior. Finally, we found that the Gr/n-Si Schottky diodes that were exposed to ambient conditions for 7 days exhibited a ∼3.2-fold higher sheet resistance compared with the as-fabricated Gr/n-Si diodes, implying a considerable electrical degradation of the Gr/n-Si Schottky diodes.

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I. INTRODUCTION

Graphene (Gr), which comprises a two-dimensional (2D) network of sp^2 hybridized carbon atoms packed into a hexagonal structure, has attracted a great deal of attention owing to the long-range ordered π-conjugation structure that is responsible for its excellent thermal, electrical, and mechanical properties [1–3]. Significant efforts have been applied toward using Gr as an electrode or channel region in the fabrication of flexible electronic devices [4]. In addition, a monolayer of Gr has a thickness of ∼0.34 nm and absorbs ∼2.3% of white light; even a 1-μm-thick Gr layer has a transparency of approximately 70%, which enables the use of Gr as a transparent electrode [5–7]. In this regard, previous uses of Gr in organic solar cell applications were mainly limited to flexible transparent electrodes as a substitute for transparent indium tin oxide or fluorine-doped tin oxide for collecting charge carriers [8]. Recently, Gr-on-silicon configurations were incorporated into solar cells by using the membrane transfer technique to form a Schottky junction with the substrate because as an energy conversion material, Gr not only contributes to charge separation and transport but also functions as a transparent electrode [9–11]. However, power conversion efficiencies of Gr-based solar cells are still very low (∼3.9% at AM 1.5) [9]. The concept of Schottky junctions made of graphene and a solid silicon substrate and a good understanding of surface passivation, doping, and junction formation will lead to the development of much more effi-

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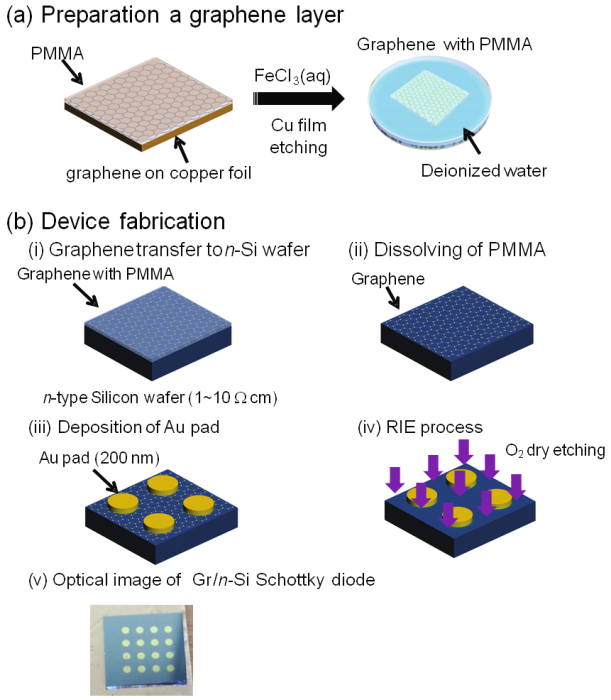

Fig. 1. (Color online) Schematic illustration of the Gr/n-Si Schottky junction diode fabrication: (a) etching of the Cu foil for graphene transfer and (b) steps for Au/Gr/n-Si Schottky junction diode fabrication.

cient and stable Gr-based solar cells with improved power conversion efficiency in the future [10]. However, if the performance of Schottky-junction-based devices such as solar cells are to be imporved, more detailed studies are required to understand the electrical transport properties and the Gr/n-Si interface layer of Schottky junction diodes on Gr/silicon including device degradation.

In this study, we fabricated Gr Schottky-junction diodes on n-type silicon substrates. To analyze the electrical transport properties of Gr/n-Si Schottky diodes, we performed both current density-voltage ($J-V$) and capacitance-voltage ($C-V$) measurements at room temperature.

II. EXPERIMENTAL DETAILS

A two-temperature-zone CVD system was used to grow high-quality Gr films. This method allows the synthesis of a monolayer Gr film on Cu foil in the same manner as we previously reported [12]. In brief, a Cu foil is first loaded into a quartz tube and is heated to ∼1000 °C with H_2 flowing at 2 sccm at 20 mTorr. After annealing for 30 min, a gas mixture of CH_4 and H_2 is passed at 400 mTorr. The samples are then rapidly cooled to room temperature. In order to detach the grown Gr film from the Cu foil, we coated a polymethylmethacrylate (PMMA) layer on the Gr film on the Cu foil by using the spin-coating method. As shown in Fig. 1(a), the PMMA-coated Gr films were detached by etching the underlying Cu with a $FeCl_3$ solution. The freestanding Gr sheets that floated on the surface of distilled (DI) water were simply transferred to the n-type silicon (n-Si) substrate in the water. For the fabrication of Gr/n-Si Schottky junction diodes, we used the n-Si wafer (100, phosphorous doped with a concentration of $\sim 2 \times 10^{15}$ cm^{-3}, a thickness of ~ 500 μm, and a resistivity of 1 − 10 Ω·cm). Prior to transferring the Gr film to the substrate, we immersed the n-Si substrate a buffered oxide etch (BOE) for 5 min to remove native oxide, rinsed it with DI water, and dried it with blowing N_2. Finally, the Gr films transferred n-Si substrates were immersed in acetone for 12 h to remove the PMMA on Gr layers. To fabricate the Gr/n-Si Schottky diode, we deposited a circular-shaped Au (200 nm in thickness) electrode with a 1-mm diameter onto the Gr/n-Si substrate through a metal mask by using an electron beam evaporation technique at a pressure of 3×10^{-6} Torr. The remaining Gr films were completely removed by using O_2 plasma reactive ion etching (RIE) to reduce the leakage current, as shown in Fig. 1(b). Finally, the rear side of the n-Si surface was coated with indium gallium (InGa) paste to form large-area Ohmic metal contacts with the n-Si substrates. Figure 1(b) shows the fabrication process of an Au/Gr/n-Si Schottky junction diode with an optical image of the diode (Figure 1(b)−(v)). The as-fabricated Gr/n-Si Schottky diodes were examined by using a semiconductor parameter analyzer (Agilent technologies, 4155C) and an LCR meter (Agilent technologies, 4284A), respectively, to perform both $J-V$ and $C-V$ measurements at room temperature without any illumination.

III. RESULTS AND DISCUSSION

Figure 2(a) exhibits the $J-V$ characteristics of the Au/Gr/n-Si Schottky diodes on both linear and semilogarithmic scales. This figure shows a clear rectifying behavior of the Schottky diode. From the $J-V$ curves, the average reverse leakage current density was found to be $\sim 2.56 \times 10^{-6}$ mA/cm^{-2} at −2 V, indicating a well-defined rectifying effect. The electrical properties of the Gr/n-Si Schottky diodes were analyzed by employing thermionic-emission (TE) theory. In Fig. 2(a), a linear fit to the forward bias $\ln(J)-V$ characteristic was plotted for the forward bias voltage range of 0.1 ∼ 0.2 V in the TE region. The charge transport mechanism of the diode was analyzed by using the following equation [13]:

$$J = J_0 \left[\exp\left(\frac{qV}{nk_BT}\right) - 1 \right], \qquad J_0 = AA^{**}T^2 \exp\left(-\frac{q\phi_B}{k_BT}\right) \quad (1)$$

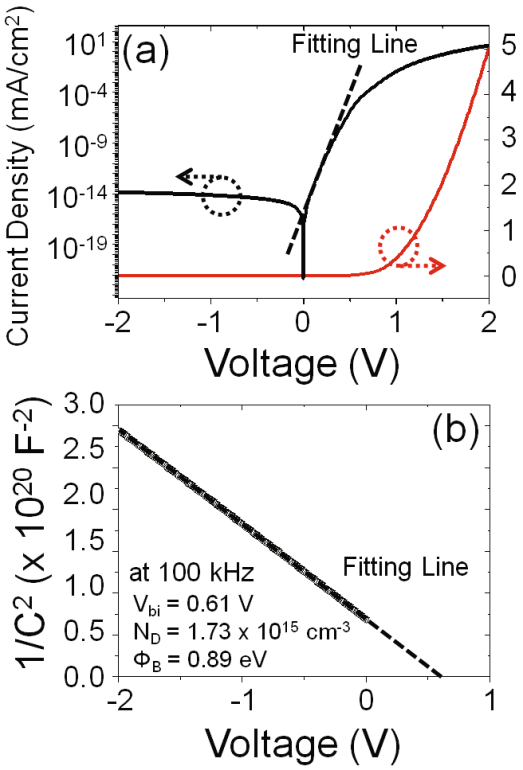

Fig. 2. (Color online) (a) The $J-V$ characteristics and (b) $1/C^2-V$ characteristics of the Gr/n-Si Schottky diodes at room temperature. The built-in voltage (V_{bi}), carrier concentration (N_D), and Schottky barrier height are also included in the figure.

where q is the electronic charge, V the voltage applied across the junction, k_B Boltzmann's constant, T the absolute temperature, J_0 the saturation current density, A the effective area of the Schottky diode, and A^{**} Richardson's constant ($\sim$112 mA/cm^{2}K^2 for n-Si). The value of J_0 was derived from the linear fit to the $\ln(J)-V$ plot at a bias voltage of 0 V, as shown in Fig. 2(a). The values of n (the ideality factor) and the Schottky barrier height (ϕ_B^{J-V}) were calculated from the slope of the fitting line in the $\ln(J)-V$ curve by using Eq. (1). The extracted values of ϕ_B^{J-V} and n are listed in Table 1. The averaged values of ϕ_B^{J-V} and n were determined to be $\sim$0.79 $\pm$ 0.01 eV and 1.80 $\pm$ 0.01, respectively. The quoted error is the standard deviation from the mean of four diodes ($n=4$). The extracted value of ϕ_B^{J-V} was in good agreement with previously reported values ($\sim$0.79 eV for Gr/n-Si) [14]. However, the measured ideality factor, n, was slightly higher than the value of $\sim$1.41 reported by Kim *et al.* [14], even though the electrical behavior that was demonstrated in those studies was similar to that of our Gr/n-Si Schottky diodes. This slight difference might be due to the different data extraction in the fitting procedure used by those authors or due to the different method of Schottky junction diode fabrication.

Table 1. Mean value of the SBH (ϕ_B) and the ideality factor (n) of as-fabricated Gr/n-Si Schottky diodes and diodes that were exposed to air for 7 days. The quoted error is the standard deviation from the mean across a sample set of 4 diodes.

Gr/n-Si Schottky diode	n	ϕ_B^{J-V} (eV)	ϕ_B^{C-V} (eV)
As-fabricated	1.80 $\pm$ 0.01	0.79 $\pm$ 0.01	0.85 $\pm$ 0.01
After 7 days	1.86 $\pm$ 0.04	0.80 $\pm$ 0.01	0.88 $\pm$ 0.01

To compare the examined values of the Schottky barrier heights of the Gr/n-Si Schottky junction diodes from $J-V$ characteristics with those obtained from other measurement technique and to obtain additional information on the interface between the Gr layer and the n-Si substrate, we performed $C-V$ measurements because this technique is crucially important for obtaining information about the rectifying contact interface of Schottky junctions and other diodes [13, 15, 16]. This technique provides both the carrier concentration of the substrates and the Schottky barrier height (ϕ_B^{J-V}). Figure 2(b) shows typical $1/C^2-V$ characteristics of an Au/Gr/n-Si Schottky diode for reverse bias voltages ranging from 0 to 2 V at a frequency of 100 kHz. As shown in Fig. 2(b), the $1/C^2-V$ characteristics for all devices were strength lines, consistent with the Schottky-Mott model and abrupt junction approximation, implying that the carrier concentration (N_D) is constant throughout the depletion width of the n-Si. The built-in voltage (V_{bi}) was determined by extrapolating the plotted $1/C^2-V$ while N_D was calculated from the slope of the plotted $1/C^2-V$ relation by using the following equations [13, 16]:

$$N_D = \frac{2}{q\epsilon_S}\left[\frac{1}{d(1/C^2)/dV}\right], \qquad \phi_B^{C-V} = V_{bi} + V_n + \frac{kT}{q} \tag{2}$$

where V is the reverse bias voltage, ϵ_S is the dielectric constant of the semiconductor, $\epsilon_S = 11.9\ \epsilon_0$ for n-Si, ϵ_0 is the vacuum permittivity, V_{bi} is the x-axis intercept at $1/C^2=0$, and V_n is the density of states at the conduction band edge calculated as $\sim$0.27 eV [15]. From the second equation in Eq. (2), we can determine the value of ϕ_B^{C-V} for the Au/Gr/n-Si Schottky junction diodes. The determined N_D and ϕ_B^{C-V} for a Gr/n-Si Schottky junction were found to be $\sim 1.73\times10^{15}$ cm^{-3} and $\sim$0.85 eV, respectively. This confirms that the value of N_D derived from the $C-V$ measurements is in good agreement with the values obtained from Hall measurements. The measured value of ϕ_B^{C-V} was $\sim$0.07 eV lower than the values reported previously [17]. This might be due to the different in sample preparation methods, including the transfer of Gr layers onto the substrates.

From the $J-V$ and the $C-V$ characteristics, we observed small differences between the values of the Schot-

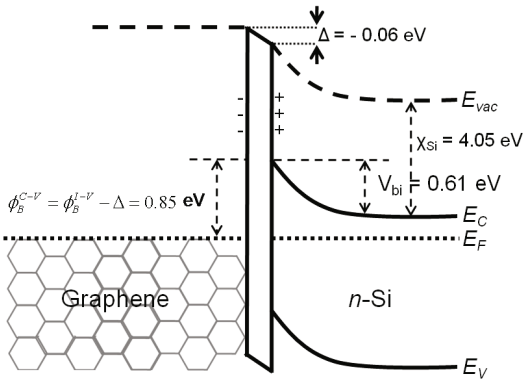

Fig. 3. Schematic energy-band diagram for the Gr/n-Si Schottky diode.

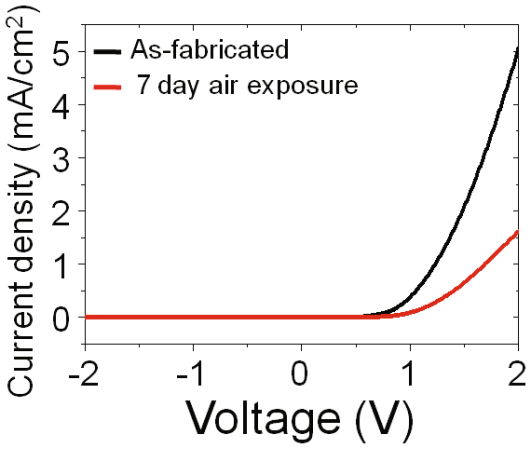

Fig. 4. (Color online) The $J-V$ characteristics of as-fabricated Gr/n-Si Schottky diodes (black line) and a Gr/n-Si Schottky diode that was exposed to air for 7 days (red line).

tky barrier height. These differences in ϕ_B^{J-V} (∼0.79 eV) and ϕ_B^{C-V} (∼0.85 eV), as summarized in Table 1, can be attributed to the characteristic nature of the $J-V$ and the $C-V$ measurement techniques and to the existence of an interfacial dipole layer at the interface (the so-called Schottky dipole), which arises from charge rearrangement between graphene and silicon [18,19]. The capacitance is generally not sensitive to potential fluctuations on a length scale smaller than the dimensions of the space charge region, and the $C-V$ measurement probes the average junction capacitance at the interface, thereby yielding an average value for the ϕ_B distribution, while the $J-V$ measurement provides a minimum value for the ϕ_B [13]. Clearly, this interfacial dipole causes a vacuum level shift (Δ), as shown in Fig. 3.

A schematic energy-band diagram of the Gr/n-Si Schottky diode in a thermal equilibrium state, including the derived junction parameters, is depicted in Fig. 3. From the vacuum level shift at the Gr/n-Si interface, we can easily extract the difference between ϕ_B^{J-V} and ϕ_B^{C-V}, which is equal to Δ if image-force lowering is neglected. Thus, as shown in Fig. 3, the value of Δ was determined to be -0.06 eV. The fact that $\Delta > 0$ at the Gr/n-Si interface may lead to a decrease in ϕ_B for electrons and an increase in electron injection efficiency [20]. This explains why Φ_B^{C-V} is higher than ϕ_B^{J-V} for Gr/n-Si Schottky junction diodes, as summarized in Table 1.

Figure 4 shows the $J-V$ characteristics of as-fabricated (black line) and 7-day air-exposed (red line) Gr/n-Si Schottky junction diodes, indicating that the air-exposed Schottky diodes are characterized by poor electrical transport behavior. The mean values of ϕ_B^{C-V}, ϕ_B^{J-V}, and n are listed in Table 1. We calculated the sheet resistance values of these diodes from the $J-V$ characteristics measured in the forward bias voltage range 1.5 ∼ 2 V. The average values of the sheet resistances for these two diodes were determined to be ∼0.17 ± 0.01 kΩ·cm^2 and ∼0.53 ± 0.04 kΩ·cm^2, respectively, indicating that the sheet resistance of the Gr/n-Si Schottky diode increased with increasing exposure time up to 7 days. This observation implies that a high-resistance layer was created at the interface between the Gr film and the substrate during the exposure to air. These results also suggest that the oxide trap, created at the interface between Gr and n-Si during the exposure to air, contributes to the degradation in the device's performance, as shown in Fig. 4 [21]. Currently, we are not able to confirm the cause of this electrical degradation in the Gr/n-Si Schottky diodes, but related research using Raman and X-ray photoelectron spectroscopy (XPS) measurements is being initiated.

IV. CONCLUSION

In summary, we used $J-V$ and $C-V$ measurements to derive the electrical transport properties of Au/Gr/n-Si Schottky junction diodes prepared on n-Si substrates by using conventional CVD and a further RIE process. The average values of the barrier heights and the ideality factors obtained from the $J-V$ measurements were ∼0.79 ± 0.01 eV and ∼1.80 ± 0.01, respectively. From the $C-V$ measurements, we noticed that the Schottky barrier height and the doping concentration obtained from the $C-V$ measurements were ∼0.85 eV and ∼1.76 × 10^{15} cm^{-3}, respectively. In addition, we confirmed that the electrical degradation of Gr/n-Si Schottky diodes was due to an interface layer created between the Gr film and the n-Si substrate during exposure to air.

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