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Effects of Controlling the Interface Trap Densities in InGaZnO Thin-film Transistors on Their Threshold Voltage Shifts

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In this paper, the threshold voltage stability characteristics of indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFT) are discussed. The IGZO TFTs were found to induce a parallel threshold voltage (V_{th}) shift with changing field effect mobility (μ_{FE}) or a sub-threshold gate voltage swing (SS) due to various thermal annealing conditions. The IGZO TFT that was post-annealed in an O_2 ambient was found to be more stable for use in oxide-based TFT devices and to have better performance characteristics, such as the on/off current ratio ($I_{on/off}$), SS, and V_{th}, than other TFTs did. The mechanism for improving the V_{th} stability in the post-annealed IGZO TFT is a decrease in the number of trap sites for the electrons and the weak oxygen bonding in the IGZO thin films. The device's performance could be significantly affected by adjusting the annealing conditions. This mechanism is closely related to that of modulation annealing, where the number of localized trapped carriers and defect centers at the interface or in the channel layer are reduced.

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I. INTRODUCTION

The development of reliable amorphous oxide-based semiconductor (AOS) thin-film transistors, especially with respect to display applications, is an important issue for TFT research. AOS TFTs are strong candidates for use in active-matrix backplanes of next-generation displays because they overcome the limitations of amorphous and polycrystalline silicon TFTs. These devices are widely used as switching elements for active-matrix liquid-crystal displays (AMLCD) and are used in pixel circuits of organic light-emitting displays (OLEDs) [1,2]. The amorphous indium-gallium-zinc oxide (a-IGZO) has excellent performances, such as low-temperature fabrication (room temperature(R.T.)), high mobility, transparency in the visible region, and a reasonable ratio of the on to the off current ($I_{on/off}$). Furthermore, the low-temperature process for a-IGZO, as compared with other materials, allows TFTs to be formed on flexible substrates (polymeric substrates) and to be applied to flexible active-matrix organic light emitting diodes (AMOLEDs) [3,4]. Thus, many studies have mainly focused on controlling the performance of a-IGZO devices, which depends on various parameters such as the sputtering power and the post-treatment [5,6]. The V_{th} stability becomes particularly important when the a-IGZO TFT is used as on active-matrix backplanes for next-generation displays. The V_{th} stability can also be an important parameter for controlling the device's performance. Thus, many studies have mainly focused on obtaining an exact understanding of the degradation behavior of oxide-based TFTs.

The electrical properties affected by the main features of oxide TFTs include the active layer, the gate insulator, and the interface trap density [7]. Among these, the interface trap density is the most complicated for various reasons; therefore, extracting any physical parameters is not easy. Several groups reported promising results based on the deposition of high-k metal oxides such as HfO_2, TiOx/SiNx and Al_2O_3 [8–10], by using ZnO-based oxide TFTs. However, very little is known about the effect of the post-annealing process on the interface trap density in SiO_2/a-IGZO-based semiconductor systems or about the threshold-voltage degradation of IGZO-based oxide transistors, even though the mobility is the most critical parameter for high-performance transistors.

In this study, we report on the effects on the threshold voltage shift and on the device performance of a-IGZO TFTs of the change in the interface trap density caused by the post-annealing process. This involves understanding how the O_2 ratio influences the electronic properties and how the electronic behavior can be controlled.

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II. EXPERIMENTS

We fabricated bottom-gate top contact TFTs with an inverted staggered bottom-gate structure using an a-IGZO active layer. The 200-nm-thick gate-insulator SiO_2 film was grown on a heavily-doped silicon wafer by using the thermal oxidation method. The upper gate insulator, the a-IGZO channel layer, was deposited by using RF magnetic sputtering with a single target (In : Ga : Zn = 2 : 2 : 1 mol %). The sputtering base pressure was under 5×10^{-6} Torr. The working pressure of the sputtering chamber, the O_2 gas mixing ratio and the rf-magnetron power were 3.5 mTorr, 32%, and 80 W, respectively. Then, The post annealing of the a-IGZO/SiO_2/heavily-doping Si films was performed using a conventional furnace at temperatures of 300 and 450 °C for 60 minutes with and without an O_2 ambient. Finally, 100-nm Al-metal source and drain electrodes were deposited and patterned on the a-IGZO channel layer by using an evaporator.

The TFT had an inverted staggered-bottom gate-type structure with a channel length of 160 μm and a channel width of 1000 μm. The electric characteristics of the a-IGZO TFT were measured by using an Agilent 4145B device parameter analyzer at room temperature in the dark. The physical characteristics of the channel layer were measured by using X-ray photoelectron spectroscopy (XPS), and the characteristics of the a-IGZO thin films were measured by using atomic force microscopy (AFM), X-ray diffraction (XRD) and ellipsometery.

III. RESULTS AND DISCUSSION

Figures 1(a) and (b) shows the drain current - gate voltage characteristics of the TFTs at different annealing temperatures with and without an O_2 ambient, which clearly show that increasing the post-annealing temperature leads to a negatively-shifted V_{th}. In contrast, the V_{th} was shifted toward the positive direction in the O_2 ambient. Thus, the V_{th} shift of the IGZO TFT depends on the post- annealing condition.

Charge trapping in the gate insulator was previously reported to be the dominant mechanism of the V_{th} shift of a TFT under constant gate bias [11]. However, post annealing for 90 minutes is thought to have cured some defect states, which could trap electrons in the IGZO active layer.

Figures 1(c) shows the evolutions of ΔV_{th} in IGZO TFTs annealed at different temperatures with and without an O_2 ambient. When annealed in an oxygen ambient, the off-state current (I_{off}) decreased a little, and the V_{th} of the IGZO TFTs shifted in the positive direction. However, the SS and the $I_{on/off}$ ratio were improved for annealing in an O_2 ambient rather than in air. Thus, the

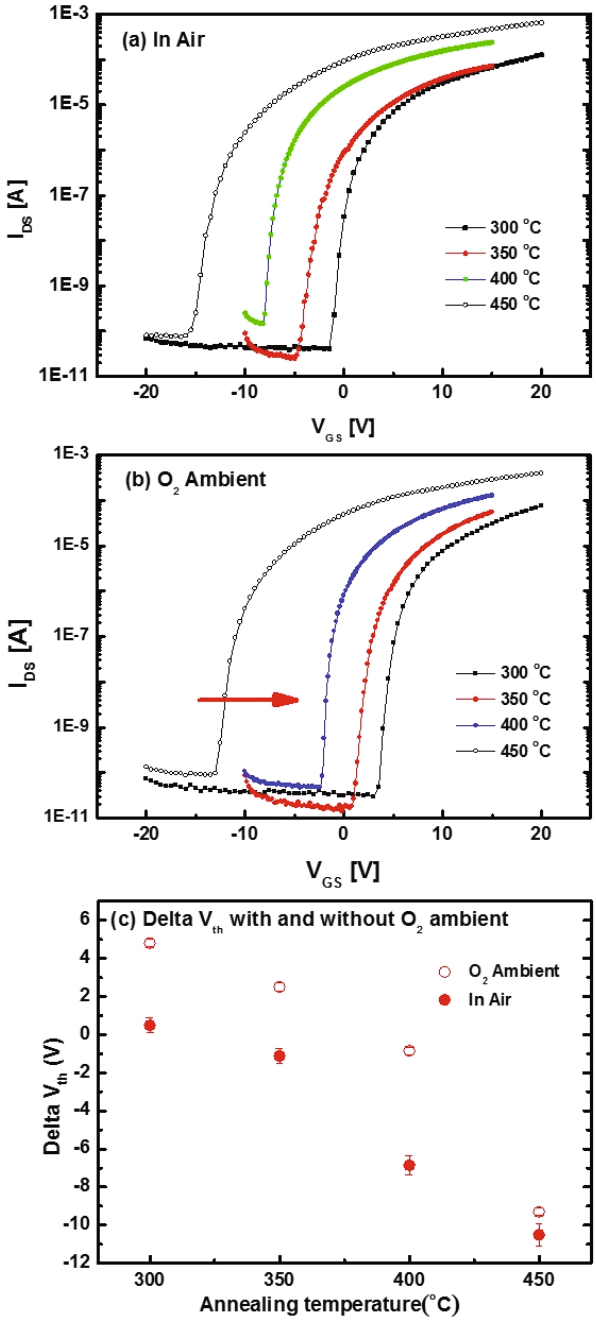

Fig. 1. (Color online) Drain current-gate voltage characteristics of the TFTs annealed at different temperatures of (a) with and (b) without an oxygen ambient. (c) The evolutions of the V_{th} shift in IGZO TFTs annealed at different temperatures from 350 °C and 450 °C of with and without an oxygen ambient.

off current, V_{th} and SS can be controlled by changing the processing parameters.

The field effect mobility (μ_{FE}) and the threshold voltage variation (ΔV_{th}) derived from the saturation characteristics of the annealing conditions were directly related to the crystallinity of the IGZO thin film grown with

annealing. This agreed with the good performance of the IGZO TFT fabricated at a reasonable post-annealing temperature in an O_2 ambient in terms of the V_{th} stability. To confirm the origin of the dependence of the change in the V_{th} stability of the IGZO TFT on the post-annealing process, we observed the trap densities in the interface and in the IGZO bulk by using an analysis of the physical characteristics.

Table 1 shows the electrical characteristics of the post-annealed IGZO TFTs with and without an O_2 ambient. The saturation mobility was markedly reduced at all temperatures after the post annealing with an O_2 ambient. We suggest that post annealing with an O_2 ambient can reduce the free-electron carrier density in the IGZO channel layer. Consequently, the entire SS value of the IGZO TFT is significantly improved by post annealing with an O_2 ambient. These improved characteristics are due to the optimized number of oxygen vacancies in the IGZO channel layer and to the crystalline growth. Thus, optimizing the trap density in the IGZO channel layer is important for making a reasonable TFT.

We investigated the effect on the bias stability of the resulting IGZO TFTs due to the post annealing in an O_2 ambient. Figures 2(a) − (c) shows the degradation in the normalized sub-threshold slope (ΔSS) in devices annealed with and without an O_2 ambient as a function of the stress time for a bias stress of 20 V. The values of ΔSS for both devices are slightly degraded as the stress time increases, which indicates that the trap charges are trapped at the IGZO/SiO_2 interface, although it is not the dominant mechanism behind the bias-stress-induced ΔV_{th} in either device. The change in the value of ΔSS is due to trap generation at the IGZO/SiO_2 interface and/or at the grain boundaries in the IGZO channel region. We should note that the degradation is greater for annealing in air than it is for annealing in an O_2 ambient. The relatively larger ΔSS in the device annealed in air shows that stress-induced traps are more easily created at the IGZO/SiO_2 interface than they are in the device annealed in an O_2 ambient.

Figure 3(a) shows the XRD patterns of the IGZO thin films annealed at temperatures ranging from 300 to 450 °C. In general, the deposited IGZO thin film shows an amorphous phase while the films annealed at temperatures above 350 °C exhibits a weak crystalline phase with (101) peaks [12], as seen in the XRD measurements. As the annealing temperature was increased to higher temperatures (300 − 450 °C), four diffraction peaks appeared. The weak crystalline peak at 31.7 degrees corresponds to the diffraction of the IGZO channel layer, and its intensity increased with increasing temperature. However, the IGZO film formed by annealing in an O_2 ambient had a weak crystalline phase for annealing temperatures above 350 °C. In addition, the crystallinity of the IGZO thin film annealed in an O_2 ambient (not shown in this paper) was less than that of the film annealed in air. The growth of a weak crystalline phase might have been due to oxygen radicals around the IGZO

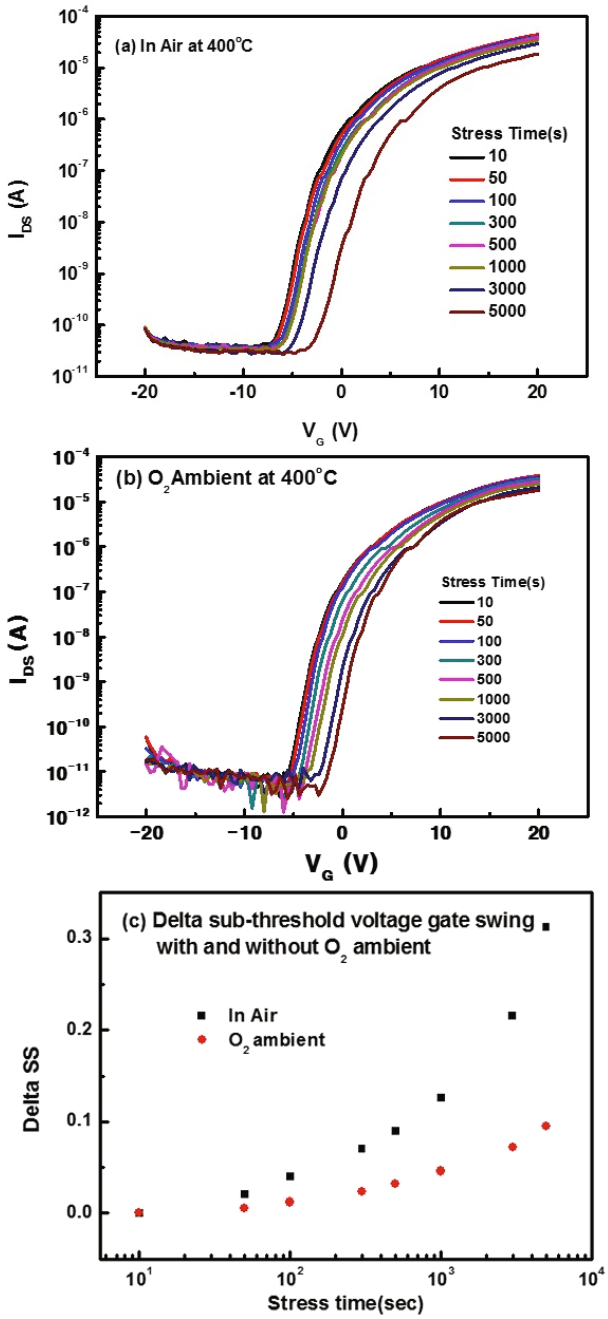

Fig. 2. (Color online) The evolution of the transfer characteristics for the IGZO TFTs annealed (a) with and (b) without an oxygen ambient at 400 °C and (c) the ΔSS as a function of the stress time.

thin film that had been activated by the annealing temperature. As shown in the electrical results, the μ_{FE} of the IGZO thin films improved with increasing annealing temperature while the V_{th} stability tended to deteriorate.

The XRD results are in good agreement with the high-resolution TEM (HRTEM) images and diffraction patterns of the samples annealed at 450 °C. As shown in the Fig. 3(b), the IGZO thin films had thicknesses of

Table 1. Electrical properties for various annealing conditions. The IGZO TFTs show the best electrical stability when annealed at 400 °C in an O_2 ambient.

Condition		I_{off} (A)	SS (V/decade)	$I_{on/off}$ ratio	V_{th} (V)	Mobility (cm^2/Vs)
300 °C	Air	3.9×10^{-11}	0.39	3.2×10^{6}	0.48	2.98
	O_2	2.9×10^{-11}	0.37	2.6×10^{6}	4.8	1.75
350 °C	Air	2.5×10^{-11}	0.59	2.9×10^{6}	−1.13	3.4
	O_2	1.4×10^{-11}	0.38	3.9×10^{6}	2.5	2.6
400 °C	Air	1.5×10^{-10}	0.32	1.6×10^{6}	−6.85	11
	O_2	4.5×10^{-11}	0.24	2.9×10^{6}	−0.85	6
450 °C	Air	7.5×10^{-11}	0.55	8.7×10^{6}	−10.5	15.3
	O_2	8.9×10^{-11}	0.36	2.4×10^{6}	−9.3	9.25

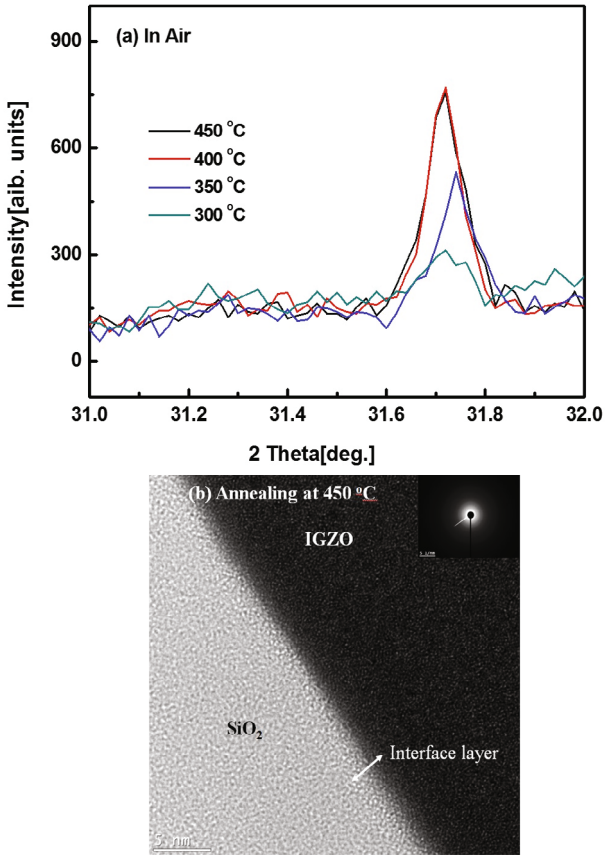

Fig. 3. (Color online) (a) X-ray diffraction patterns and (b) cross-sectional high-resolution TEM images of the IGZO thin films annealed in air at 450 °C.

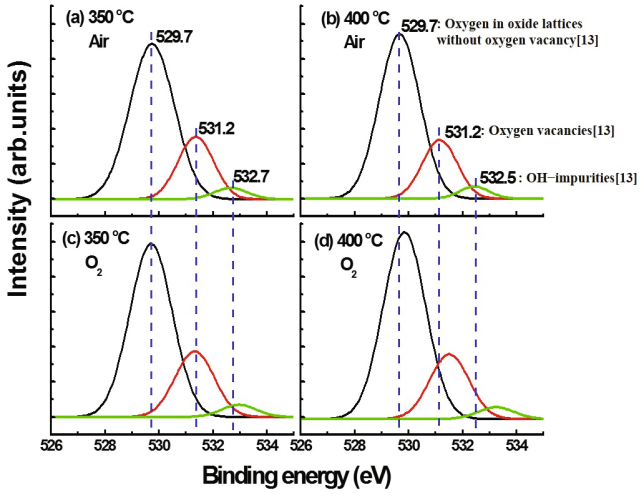

Fig. 4. (Color online) Deconvolution of the O1s peak of the XPS spectra by the method of curve fitting for IGZO films with different post annealing conditions.

about 30 nm and an amorphous-like phase. In the case of the sample annealed at 450 °C, a very small amount of crystallization was observed to occur at the interface layer between the SiO_2 gate insulator and the IGZO thin film. Thus, the low density and the small range of these crystals result in their producing diffraction peaks in the XRD measurements and diffraction patterns. The weak crystalline growth even with annealing is related to increases in the number of free elections and the number of oxygen vacancies at the interface layer.

In order to investigate the origin of the above results, we used XPS to analyze the chemical and the structural evolutions of the a-IGZO thin films fabricated under different annealing conditions. Figure 4 presents the deconvolution of the O1s peak of the XPS spectrum by the method of curve fitting for IGZO films with different post-annealing conditions. The O1s peaks centered at binding energies of 529.7, 531.2 and 532.7 eV are, respectively, related to oxygen in oxide lattices without oxygen vacancies, with oxygen vacancies and with OH- impurities [13]. It clearly the relative shift of the oxide lattices without an oxygen-vacancy-related peak increased as a result of post-annealing in an O_2 ambient at temperatures above 400 °C. The increasing portion of the 529.7 eV peak with increasing annealing temperature in an O_2 ambient indicates a reduce trap density due to crystal growth in the IGZO thin films. The peak positions of The two kinds of OH- impurities in the IGZO channel layer shifted during post annealing in an O_2 ambient with increasing annealing temperature because the increase in

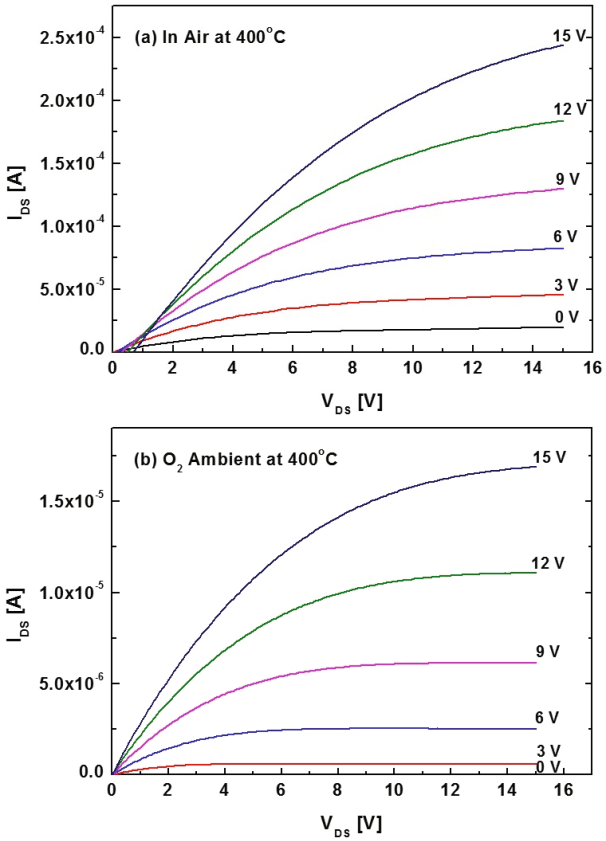

Fig. 5. (Color online) Representative output characteristics of the IGZO TFTs annealed (a) with and (b) without an oxygen ambient at 400 °C, respectively.

the binding energy from 532.9 to 533.2 eV might indicate that the IGZO thin film annealed at a higher temperature in an O_2 ambient had fewer oxygen vacancies. This result agrees well with the mobility and the positively-shifted V_{th} shifted with increasing annealing temperature from 300 to 400 °C in an O_2 ambient. The generation of oxygen vacancies was proven to be relevant to the density of charge trapped in the gate insulator/IGZO thin film. The results of the chemical characterization of the IGZO thin films corresponded to the XPS results.

Figures 5(a) and (b) show representative output characteristics of the IGZO TFTs annealed with and without an O_2 ambient at 400 °C, respectively. We note that a drain current of roughly 1 μA is required to manifest a full white-gray color in the AMOLED device [14]. The saturation drain current for the a-IGZO TFT annealed without an O_2 ambient at 400 °C was 2.53 μA at V_{GS} = 6 V while a value of 45.8 μA was achieved even at a low V_{GS} of 3 V for the IGZO TFT annealed in an O_2 ambient at 400 °C.

The stability of the a-IGZO TFT post annealed in an O_2 ambient is worth mentioning. The stabilities of the a-IGZO TFT after post annealing with and without an O_2 ambient were compared. The a-IGZO TFT post annealed with an O_2 ambient was more stable. Also, the SS, $I_{on/off}$ and other parameters were found to be significantly improved by post annealing in an O_2 ambient at 400 °C.

IV. CONCLUSION

We have investigated the interface trap densities of IGZO/SiO_2 thin films prepared on heavily-doped Si substrates by using various annealing temperatures with and without an O_2 ambient. The electrical characteristics of the IGZO TFTs with and without an O_2 ambient have been compared by plotting the transfer characteristics. The IGZO TFT post-annealed in an O_2 ambient is found to be more stable and to have better performance characteristics, such as the $I_{on/off}$ ratio, SS, and V_{th}. The transfer and the output characteristics of the IGZO TFTs were controlled to achieve the optimum annealing conditions.

The post-thermal-annealing process is used to repair the interface traps in the IGZO thin film and to reduce the bulk traps in the channel. The trap charge in the bulk, which is compensated for during the annealing process, clearly shows that increasing the annealing temperature leads to a negatively-shifted V_{th}. Thus, the weak crystalline growth under annealing conditions is related to increases in the numbers of free elections and of oxygen vacancies at the interface layer.

Post-annealing improves the V_{th} stability in IGZO TFTs because the carrier concentration is decreased due to the number of trap sites for electrons being reduced and to the weak oxygen bonding in the IGZO thin films. This work is expected to be useful to further advance oxide-based TFT technology for future devices.

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