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Inkjet-printed Zinc-tin-oxide TFTs with a Solution-processed Hybrid Dielectric Layer

Hye-Ryun JANG,* Young-Jin KWACK* and Woon-Seop CHOI†
Department of Display Engineering, Hoseo University, Asan 336-795, Korea

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Sol-gel TiO_2 was synthesized and used as a gate dielectric for oxide thin-film transistors (TFTs). A hybrid gate insulator composed of sol-gel TiO_2/thermally-grown SiO_2 was applied to the inkjet-printed zinc-tin oxide (ZTO) TFTs for the first time. The electrical properties of an inkjet-printed ZTO TFT with a hybrid gate insulator show a mobility of 0.17 cm^2/Vs, an on-to-off current ratio of 5 $\times 10^4$, a subthreshold slope of 0.8 V/dec, and a threshold voltage of 0.6 V. The hybrid gate insulator for the inkjet-printed ZTO TFT shows a much improved operating voltage and subthreshold slope and a lower mobility compared to the SiO_2 gate insulator.

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I. INTRODUCTION

Amorphous-silicon thin-film transistors (TFTs) have been widely used for switching devices for displays. However, the mega trend of displays has focused on the demand for large-scale and high-resolution semiconductors with high mobility and better electrical properties. One such semiconductor is low- temperature polysilicon (LTPS), which is used for active-matrix organic light-emitting diodes (OLED) fabrication. However, the problems of LTPS are its poor uniformity and the need for expensive laser equipment. Recently, amorphous-oxide TFTs with $(n-1)\ d_{10}\ ns_0$ (n $\geq$ 4) electron configurations have attracted attention. Among them, In_2O_3, ZnO, In-Zn-O (IZO), In-Ga-Zn-O (IGZO), and Zn-Sn-O (ZTO) are being developed for potential industrial applications [1]. These amorphous-oxide TFTs show higher mobility than a-Si TFTs and better uniformity compared to TFTs with LTPS. This is a big advantage for industry because the sputter system and other equipment used for oxide TFTs are compatible with those used for the current a-Si TFTs.

Another advantage of oxide TFTs is solution-processability for applying printed electronics. Solution-processibility has several advantages over the conventional lithography process. These advantages include direct patterning, less chemical usage, and no need for expensive equipment. Currently, various printing techniques, such as ink-jet printing [2,3], spray pyrolysis [4, 5], electrohydrodynamic (EHD) spraying [6], and EHD cone-jet printing [7,8], have been used for oxide TFTs. Micro-patterning techniques and high-performance devices are under developed. However, most research on solution-processed TFTs has focused on the development of solution-processed semiconductors. If fully-printed TFTs are to be made, electrodes and gate dielectrics should be solution-processed. Most research papers have reported on oxide TFTs either with thermally-grown SiO_2 on a highly-doped silicon wafer [2,3,5,6], with gate dielectrics fabricated by using a vacuum process or with solution-processed semiconductors [7–9]. High-k gate dielectric layers in TFTs increase the capacitive coupling between the gate electrode and the semiconductor layer, improving the subthreshold gate swing and the operation voltage range and resulting in low power consumption in display devices. Well-known potential high-k materials for oxide TFTs are Al_2O_3 (k∼8) [10], HfO_2 (k∼16) [11], Y_2O_3 (k∼18) [12], ZrO_2 (k∼18) [13], and TiO_2 (k∼40) [14].

There are several reports on Al_2O_3, Zr_2O, and HfO_2 as gate dielectrics, but none on TiO_2 fabricated by using a solution process. Therefore, a study of high-k TiO_2 fabricated by using a solution process combined with an oxide semiconductor fabricated by inkjet-printing is worthwhile because no research on the application of a TiO_2-based hybrid gate dielectric to inkjet-printed oxide TFTs has been reported yet. We synthesized sol-gel TiO_2 and coated it on SiO_2 to make a hybrid gate dielectric for inkjet-printing ZTO TFTs for the first time.

*These authors contributed equally to this work.
†E-mail: wschoi@hoseo.edu

II. EXPERIMENTS

1. Sol-gel TiO_2

Sol-gel TiO_2 was synthesized by using methods similar to those in the literature [15–17]. Forty mL of 2-methoxyethanol, 8 mL of titanium isopropyloxide, and 4 mL of ethanol amine were charged in a round-bottom flask with magnetic stirring at 800 rpm under an argon atmosphere to remove oxygen and to minimize moisture. After the flask had been kept at 80 °C for 10 min, the temperature was increased to 120 °C. The temperature was kept at 120 °C until the color solution changed from a wine color to a sol-gel. After the formation of the sol-gel, 20 mL of ethanol was added, and the color of the solution turned light yellow. To make the film, we diluted the solution with ethanol and filtered it by using a poly-tetrafluoroethylene (PTFE) syringe filter (0.2-μm pore).

2. Inkjet-printed TFTs

The sol-gel TiO_2 solution was spin-coated on the SiO_2 dielectric layer, which was treated with UV/O_3 for 10 min. After the TiO_2 film has been pre-baked at 80 °C on a hot plate for 10 min, the film was annealed at 150 °C for one hour under vacuum conditions as in the literature [15–17] or at 500 °C for one hour in air. A 0.3-M precursor solution was prepared from zinc acetate dihydrate and tin chloride at the same molar ratio in a 2-methoxyethanol solvent and acetylacetone cosolvent. The solution was stirred for 10 hours at room temperature. An UV/O_3 treatment for 10 min was performed on the TiO_2 gate dielectric to improve the inkjet wetting properties for forming ZTO thin films. A ZTO TFT without the TiO_2 dielectric was also prepared as a reference. An inkjet printing system (Unijet, Omnijet Mini-100) with a 50-μm nozzle size was used for jetting of the oxide solution. After inkjet printing of the ZTO active layer, the device was thermally annealed at 500 °C for one hour in air. Aluminum was deposited to a thickness of 100 nm by using thermal evaporation at 1×10^{-6} Torr for the source and the drain with a channel width of 1500 μm and a length of 100 μm.

The film's thickness was measured by using a Nanoview system (Nano System, E-1000). The surface morphology was examined by using an atomic force microscope (AFM, PSIA, XE-150). The formation of a jetting dot from the ZTO solution was monitored using a video microscope (Hirox, KH-3000). All current voltage (I-V) characterizations of the ZTO TFTs were carried out using a semiconductor parameter analyzer (Keithley 4200) in a dark box at room temperature.

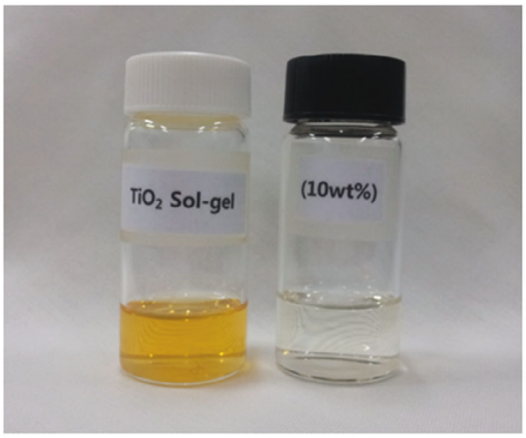

Fig. 1. (Color online) Synthesized sol-gel TiO_2 and 10-wt% solution in ethanol.

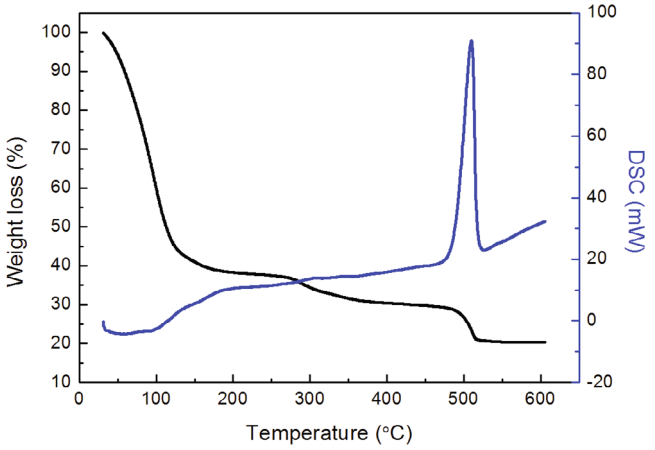

Fig. 2. (Color online) TG/DSC thermogram of a solution-processed TiO_2 gate dielectric.

III. RESULTS AND DISCUSSION

Various synthesis methods, as described in Experimental, have been reported for sol-gel TiO_2 [15–17]. However, the important factors for the preparation of sol-gel TiO_2 are the reaction temperature and the removal of the reaction vapor. The reactant begins to boil at 120 °C, and the vapor that is formed during the reaction should be properly exhausted to get a sol-gel. A wine-colored viscous sol-gel is prepared after a one-hour reaction. Figure 1 shows (a) the synthesized sol-gel TiO_2 and (b) the 10-wt% TiO_2 solution in ethanol used for coating. The synthesized pristine product was wine-colored, and it turned from a yellow to a clear solution with ethanol addition. When the sol-gel TiO_2 was spin-coated, the ethanol-based solution was easily volatilized. With care, a relatively uniform thickness of 35 nm could be obtained in a solution-processed TiO_2 gate dielectric.

Figure 2 shows the thermogravimetric/differential scanning calorimeter (TG/DSC) thermogram for the sol-gel TiO_2 solution. The solution was vaporized by heating

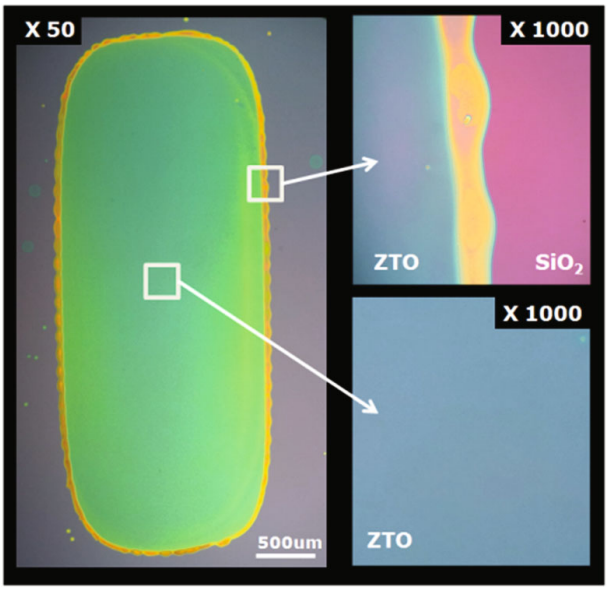

Fig. 3. (Color online) An optical microscopic image of a multi-inkjet-printed ZTO active area.

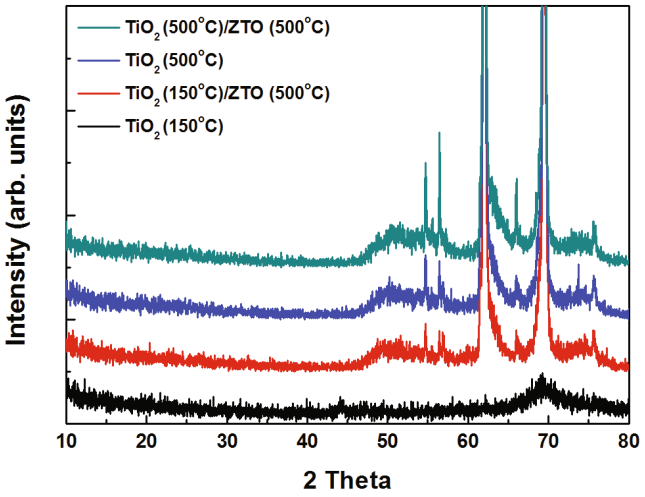

Fig. 4. (Color online) XRD spectra of the TiO_2 thin films annealed at 150 °C under vacuum and 500 °C in an oven: TiO_2 (500 °C)/ZTO (500 °C) and TiO_2 (500 °C), and TiO_2 (150 °C)/ZTO (500 °C) and TiO_2 (150 °C) under vacuum and in an oven, respectively.

at 110 °C under vacuum to remove a certain amount of solvent before the measurements. In the thermogravimetric analysis (TGA), the solvent and the water were vaporized at 100 − 150 °C, and organics were vaporized at approximately 300 − 350 °C. All chemical residuals were completely removed, and crystalline TiO_2 was formed at approximately 500 °C. After the TiO_2 thin films had been annealed under two different thermal conditions, vacuum annealing at 150 °C and hot-plate annealing at 500 °C, the films were treated with UV/O_3 for 10 min to obtain uniform inkjet ZTO films. The drop-on-demand inkjet-printing parameters were optimized with a jetting frequency of 1,000 Hz, a distance between the jetting head and substrate of 0.5 mm, and a substrate temperature of 50 °C [18]. In general, inkjet-printed thin films show different surface morphologies due to the so-called coffee-ring effect. In order to make an active area, we performed multiple inkjettings to obtain a 2000 × 5000 μm^2 pattern size. The patterned ZTO active layer had a smooth surface and enough area to cover the source and the drain electrodes with a relatively small coffee-ring edge as shown in Fig. 3. The thickness of the active layer was 15 nm with a coffee-ring edge of 35 nm.

The inkjet-printed ZTO semiconductor thin film was annealed at 500 °C. In a solution process, high-temperature annealing at a temperature above 400 °C is required for the removal of organic residues and for oxide lattice formation [19]. Chemical reactions, such as dehydration, dehydroxylation, and polycondensation, take place during oxide lattice formation and create metal hydroxides, oxygen vacancies, and organic impurities. Therefore, low-temperature annealing produces lattice defects and organic impurities, causing a leakage current with a 'normally on-state' of the TFT. Meanwhile, at higher annealing temperatures, polycrystallization with a grain boundary, which acts as a leakage current pathway, occurs [20–22]. Therefore, the annealing temperature is an important factor in the solution process, and a gate dielectric material with low leakage current density is highly desirable for a low-temperature solution process.

Figure 4 shows XRD spectra of TiO_2 thin films for different annealing conditions. The TiO_2 annealed at 150 °C under vacuum showed an almost amorphous structure except for a broad SiO_2/Si (004) peak around 69 degree [23]. In the case of TiO_2 annealed at 500 °C, the strong TiO_2 peaks at 62.0° (403), 66.1° (514), and 75.6° (623), with Si/SiO_2 peaks at 51.5°, 54.5°, and 69.3° [23, 24] indicate a crystalline anatase state. This crystallinity was also observed in TiO_2 after active annealing. These peaks were identified by using JCPDF: 00-046-1238 data. The crystallization was also confirmed by the TG/DSC thermogram.

The surface roughness of TiO_2 annealed under different conditions was analyzed by using an AFM as shown in Figs. 5(a) and (b). The values of R_q (root-mean-square roughness) were 0.32 nm and 0.72 nm while the values of R_a (average roughness) were 0.25 nm and 0.54 nm and the values of R_{pv} (peak-to-valley roughness) were 3.73 nm and 8.42 nm for TiO_2 annealed at 150 °C and 500 °C, respectively. Interestingly, the surface roughness of TiO_2 annealed at 500 °C was almost twice that of TiO_2 annealed at 150 °C. This is attributed to the crystalline domains and grain boundaries [25]. The different growth directions between grains produced many boundaries and tiny gaps between them [26]. The grains of TiO_2 annealed at 500 °C showed round-type morphologies with large scales, which was consistent with

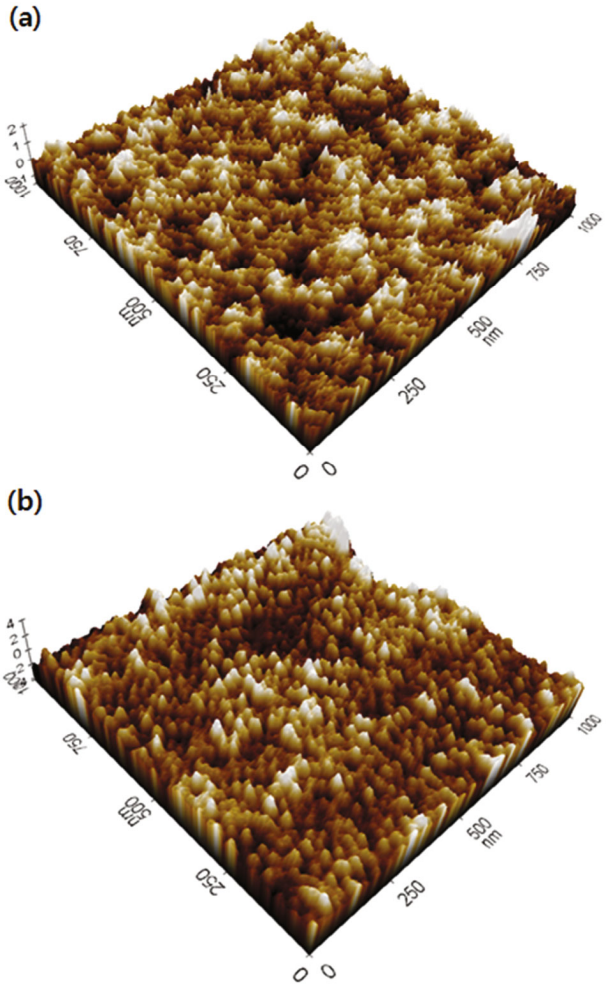

Fig. 5. (Color online) Atomic force microscopy (AFM) surface roughness of TiO_2 films annealed at (a) 150 °C and (b) 500 °C.

the XRD results.

Figure 6 shows the capacitance values of gate dielectrics in metal-insulator-metal (MIM) structures. The values were obtained by using a CV meter. The measured capacitance of silicon dioxide was 12.1 nF/cm^2, and the capacitances of solution-processed TiO_2-SiO_2 hybrid gate dielectrics were approximately 11.5 nF/cm^2 and 12.2 nF/cm^2 for the annealings at 150 °C and 500 °C, respectively. Interestingly, the solution-processed TiO_2 did not influence the capacitance of the SiO_2 gate dielectric.

Figure 7 shows the transfer characteristics of inkjet-printed ZTO TFTs with different gate dielectrics: SiO_2, TiO_2/SiO_2 (annealed at 150 °C), and TiO_2/SiO_2 (annealed at 500 °C). The electrical properties of thermally-grown silicon oxide showed a higher on-current and on-to-off current ratio with better mobility compared to the hybrid gate dielectric layer of SiO_2/TiO_2. The mobilities were 2.84, 0.17 and 0.01 cm^2/V·s, the on-to-off current ratios were 7 × 10^5, 5 × 10^4 and 3 × 10^4, the subthreshold slopes were 1.3, 0.8 and 2.3 V/dec, and the threshold voltages were −2.7, −0.6 and 0.9 V for SiO_2, TiO_2/SiO_2 (annealed at 150 °C) and TiO_2/SiO_2 (annealed at 500 °C), respectively. In general, the deterioration of the mobility comes from Coulomb scattering by ionized fixed charges and phonon scattering by lattice vibrations. The degradation of the mobility by inserting the TiO_2 layer was attributed to the Coulomb scattering mechanism rather than the phonon scattering mechanism of the TiO_2 layer [27]. The interface between the active layer and the gate dielectric layer is a key factor in the TFT's performance. The thermally-grown SiO_2 films were more uniform and denser than the solution-processed TiO_2 films. Therefore, TiO_2 in a hybrid gate dielectric with defects and poor density has poor interfaces with the active layer, resulting in degraded properties. In the solution process, this trend is worse due to the film's quality, defects, and poor density due to the low-temperature annealing process.

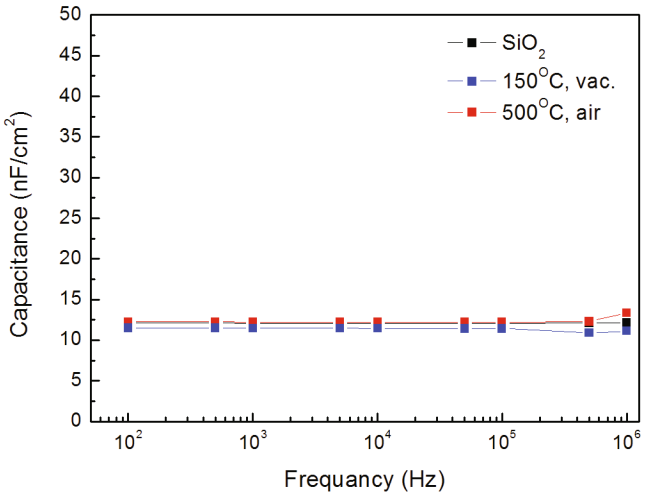

Fig. 6. (Color online) Capacitance as a function of frequency for different gate dielectrics, (a) silicon dioxide, (b) TiO_2/SiO_2 annealed at 150 °C in vacuum, and (c) TiO_2/SiO_2 annealed at 500 °C in air.

Even though the mobility and the on-to-off current ratio of the SiO_2/TiO_2 hybrid gate dielectric were lower than those of SiO_2 gate dielectric, the threshold voltage was improved to nearly zero volts, and the subthreshold slope was improved. The improved subthreshold suggests that the interfacial trap density was protected by the TiO_2 layer. The improved threshold voltage implies that the TiO_2 in the hybrid dielectric layer has a positive fixed charge density. Similar results with degraded mobility were reported for a vacuum-deposited TiO_2 gate dielectric in oxide TFTs [27,28]. IGZO TFTs were prepared with different gate dielectric, SiNx and $SiNx/TiO_2$, by using vacuum techniques, and the mobility was shown to decrease with increasing TiO_2 thickness. With an 8-nm thickness of TiO_2, the subthreshold slope was almost constant, and the mobility and the

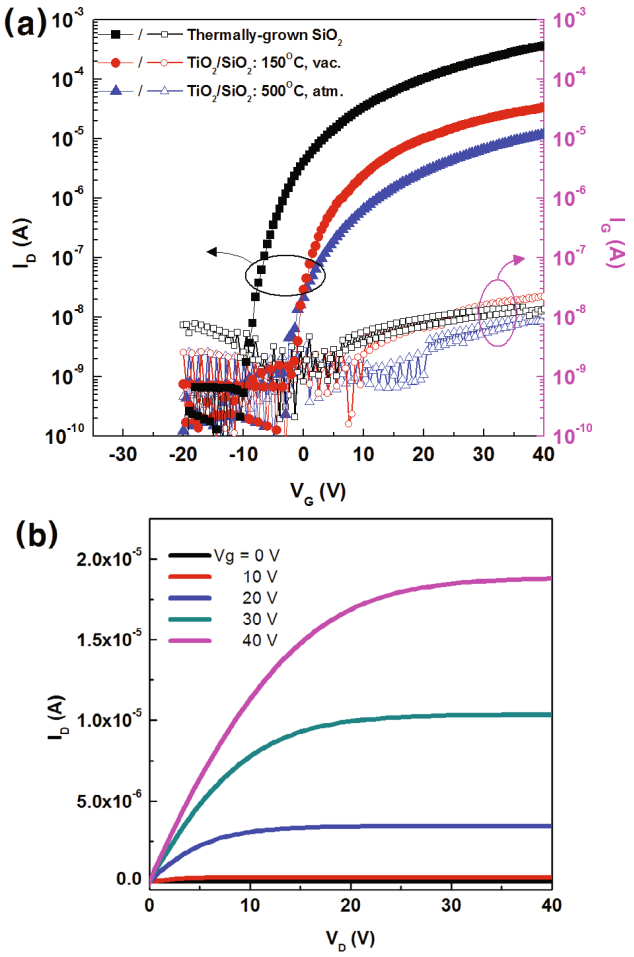

Fig. 7. (Color online) (a) Transfer characteristics of inkjet-printed ZTO TFTs with various gate dielectric layers. (b) Output characteristics of inkjet-printed ZTO TFTs based on a TiO_2/SiO_2 hybrid dielectric layer annealed at 150 °C for various gate voltages (Vg).

on-to-off current ratio were decreased from 12.5 to 1.8 cm^2/Vs and from 10^8 to 3×10^7, respectively. However, the threshold voltage was improved from 10 to 5 V [27]. In ZTO TFTs with similar gate dielectric structures of SiNx and $SiNx/TiO_2$, the mobility was also decreased with $SiNx/TiO_2$ [28]. The output characteristics of a ZTO TFT with a hybrid gate dielectric (SiO_2/TiO_2 annealed at 150 °C) are shown in Fig. 7(b). The output curves show good contact and a clear pinch off with solid saturation behavior.

One interesting thing is the different electrical properties for the hybrid SiO_2/TiO_2 gate dielectric. The electric properties of ZTO TFTs fabricated at a higher annealing temperature were inferior to those of ZTO TFTs fabricated at low annealing temperature for the same thickness of TiO_2. The main reason is the surface roughness and the crystalline structure. From AFM images and XRD spectra, the surface roughness and the crystallinity increased with increasing annealing temperature. The electrical properties of the TFTs are significantly affected by the surface roughness and morphologic compatibility with the gate dielectric. A smooth surface improves the electrical properties of TFTs due to the improved interfacial properties between the semiconductor and the gate dielectric, resulting in mobile charge carriers being formed and the quality of the current channel in the semiconductor being improved [22].

We found that the use of high-k materials as gate dielectrics was not the only solution for improving the electric properties in dielectrics. In solution-processed gate dielectrics, controlling the annealing temperature so that is below the crystallization temperature should be considered to obtain the desired properties by minimizing Coulomb scattering and by improving the surface roughness.

IV. CONCLUSION

In order to fabricate inkjet-processed ZTO TFTs, we prepared a hybrid gate dielectric layer by depositing solution-processed sol-gel TiO_2 on thermally-grown SiO_2 for the first time. The semiconductor layer was inkjet-printed on the solution-processed hybrid gate dielectric. The morphology of the sol-gel TiO_2 film annealed at 150 °C was much smoother than that of TiO_2 annealed at 500 °C. TiO_2 annealed at high temperature has a crystalline structure, resulting in inferior properties. The electrical properties of thermally-grown silicon oxide showed a mobility and an on-to-off current ratio higher than those of a SiO_2/TiO_2 hybrid gate dielectric layer. However, the threshold voltage was improved from −2.7 to −0.6 V, and the subthreshold slope was improved from 1.3 to 0.8 V/dec for the SiO_2/TiO_2 hybrid gate dielectric. We found that the use of high-k materials as gate dielectrics was not the only way to improve the electric properties and that controlling the annealing temperature to one below the crystallization temperature and controlling the surface roughness should also be considered.

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