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Introducing scalable 1-bit full adders for designing quantum-dot cellular automata arithmetic circuits

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Abstract: Designing logic circuits using complementary metal-oxide-semiconductor (CMOS) technology at the nano scale has been faced with various challenges recently. Undesirable leakage currents, the short-effect channel, and high energy dissipation are some of the concerns. Quantum-dot cellular automata (QCA) represent an appropriate alternative for possible CMOS replacement in the future because it consumes an insignificant amount of energy compared to the standard CMOS. The key point of designing arithmetic circuits is based on the structure of a 1-bit full adder. A low-complexity full adder block is beneficial for developing various intricate structures. This paper represents scalable 1-bit QCA full adder structures based on cell interaction. Our proposed full adders encompass preference aspects of QCA design, such as a low number of cells used, low latency, and small area occupation. Also, the proposed structures have been expanded to larger circuits, including a 4-bit ripple carry adder (RCA), a 4-bit ripple borrow subtractor (RBS), an add/sub circuit, and a 2-bit array multiplier. All designs were simulated and verified using QCA Designer-E version 2.2. This tool can estimate the energy dissipation as well as evaluate the performance of the circuits. Simulation results showed that the proposed designs are efficient in complexity, area, latency, cost, and energy dissipation.

Key words: Quantum-dot cellular automata (QCA); Full adder; Ripple carry adder (RCA); Add/sub circuit; Multiplier
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1 Introduction

Nanotechnology has made a lot of progress in the field of integrated circuit fabrication. Many innovative methods and technologies have been engendered. All have specific advantages (Song et al., 2020). The process of scaling down the feature size of transistors in standard complementary metal-oxide-semiconductor (CMOS) technology has become more arduous in the last few years. Deep sub-micron undesirable responses in CMOS make alternative solutions more attractive (Navidi et al., 2021).

Quantum-dot cellular automata (QCA) are well-known. Their remarkable energy consumption compared to the standard CMOS is of great interest (Das and De, 2017). QCA circuits consist of some cells containing four quantum dots with a pair of electrons (Lent et al., 1993). The electrons in a single cell circulate quickly through the dots. According to the Coulomb repulsion between these charges, the QCA cell can be polarized to two values (P=+1 and P=−1). The cell polarization P=+1 is encoded as binary 1 (logic 1) and P=−1 is encoded as binary 0 (logic 0) (Cesar et al., 2020).

Data transfer in QCA is the responsibility of the clock. The clocking scheme includes four clock signals, and each consists of four phases, namely switch, hold, release, and relax (Singh et al., 2018). These four phases have a difference of 90° from each other. In the switch phase, the potential barriers inside cells

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are raised. Thus, the cells become polarized. In the hold phase, the barriers are held high. Thereupon, the cells get a determined polarization. In this case, each cell affects its neighborhoods' polarity. Unlike the switch phase, cell barriers are lowered in the release phase. Therefore, in the fourth and final phase (relax), the barriers are at their lowest possible level (Debnath et al., 2019). Fig. 1 shows a QCA clocking scheme.

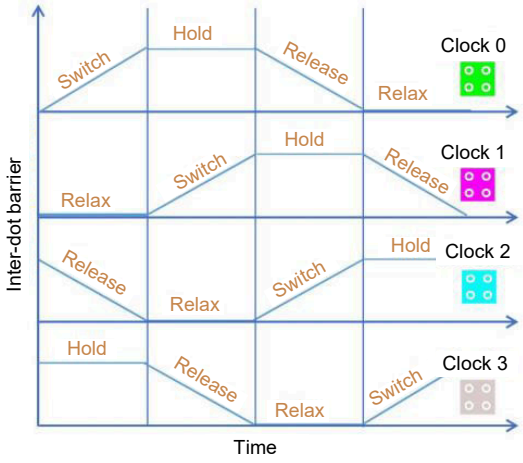

Fig. 1 QCA clocking scheme

The QCA's superiorities are the operating speed at the order of THz, high device density, ultra-low energy dissipation, and considerable flexibility for scaling down the minimum cell size to the dimensions of atoms (molecular implementation) (Blair, 2019).

A full adder is a rudimentary element of arithmetic systems. Designing an optimized full adder structure is essential for designing related intricate circuits because full adders are used extensively in larger circuits, such as multipliers. Also, adder and subtractor circuits with more entry bits need more full adder blocks in their structures.

This paper illustrates 1-bit full adders based on the interactions between QCA cells. The proposed full adders have low energy dissipation, low latency, little area usage, and low complexity (small number of cells used) compared with existing ones. We have used these structures in larger circuits, including a 4-bit ripple carry adder, a 4-bit ripple borrow subtractor, and an add/sub circuit. Finally, a 2-bit array multiplier has been designed using the proposed adder structure.

2 Background

2.1 QCA design basics

The design of QCA circuits is based on several basic structures. The QCA wiring is a primary part of each design. By putting together multiple cells in the horizontal/vertical direction, a wire will be formed. Data flows from the beginning of the wire to the end by the interaction of adjacent cells. There are two types of wiring, i.e., 90° and 45° (Xiao et al., 2012). As shown in Fig. 2, the data flows the entire 90° wire without changing the applied polarization at the beginning of the wire. However, the second type, which is known as the inverter chain, reverses the input polarity in an even number of cells. Fig. 3 shows two ways of constructing an inverter gate.

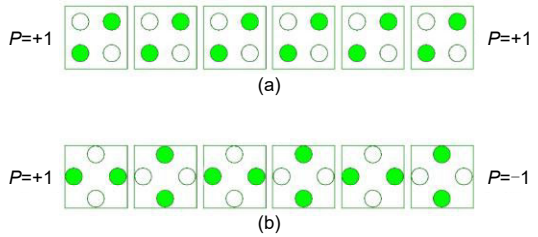

Fig. 2 Two types of wire in QCA: (a) 90°; (b) 45°

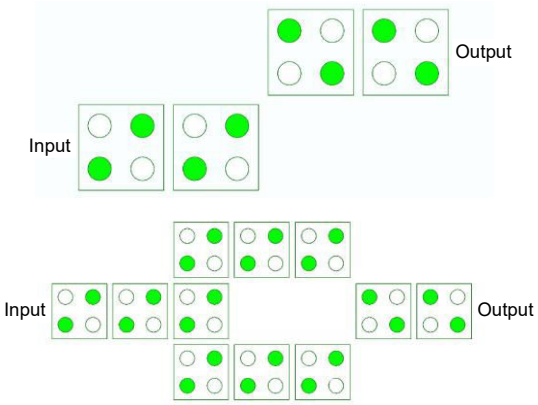

Fig. 3 QCA inverter forms

The last basic structure is the majority gate that is indispensable in almost every QCA circuit design. The majority gate depicts the most applied input polarity in its output cell. The Boolean equation of the 3-input majority gate is

$$\mathbb{M}(A,B,C)= AB + BC + AC. \quad (1)$$

By applying a fixed polarization −1/+1 to one of the majority gate's inputs, the gate transforms to AND/OR gates. Fig. 4 shows a 3-input majority gate.

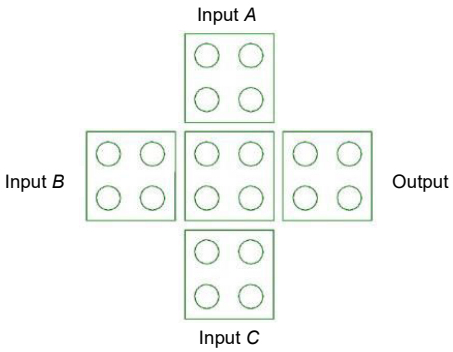

Fig. 4 The 3-input majority gate

There are three ways to cross two separate wires. The first way is to use 90° and 45° wires together, which is called coplanar crossover. The second way is to use more than a layer for crossing multiple wires. This method is multi-layer crossover. The third way is to pass two wires with a difference of two clock zones from each other at the intersection (logical crossover). Fig. 5 shows these three types of crossover in QCA designs.

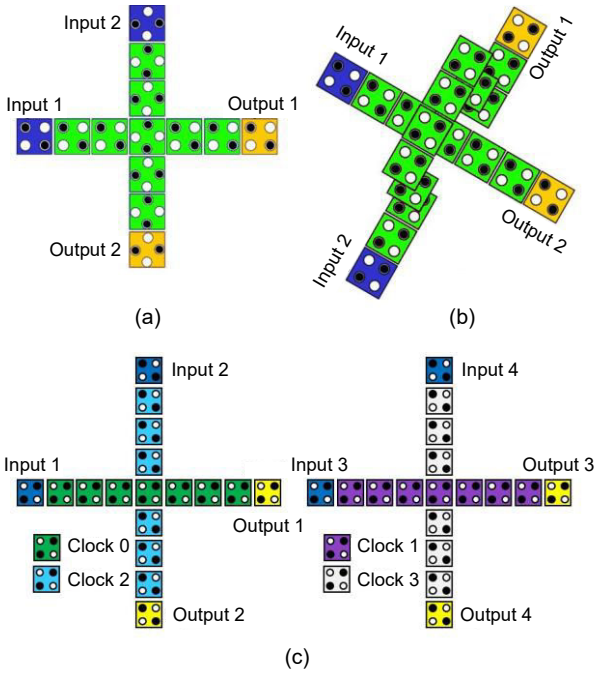

Fig. 5 Three types of crossover in QCA: (a) coplanar crossover; (b) multi-layer crossover; (c) logical crossing

2.2 Overview of full adder designs

The full adder is a digital arithmetic block with three input variables (A, B, C_{in}) and two outputs (Sum, C_{out}). The summation of input variables results in the outputs (Babaie et al., 2019). The C_{in} is quoting from the previous adder. The adder without C_{in} as input is called a half adder. Output functions are expressed by Eqs. (2) and (3), where $\mathbb{M}$ is the 3-input majority gate. Fig. 6 shows the logical diagram of a 1-bit full adder block.

$$\text{Sum} = A \oplus B \oplus C_{in}, \tag{2}$$

$$C_{out} = AB + C_{in}(A \oplus B) = \mathbb{M}(A,B,C_{in}). \tag{3}$$

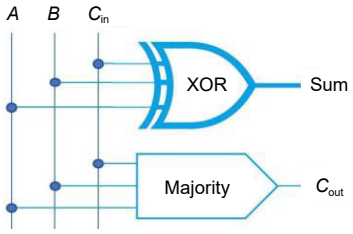

Fig. 6 Logical diagram of a 1-bit full adder block

A half subtractor can be constructed from a full adder if the second operand (second input's digits) are inverted and the carry input is set to 1. Indeed, the subtractor is the sum of the first operand and the second two's-complement operand. The output function can be attained by Eq. (4):

$$F = A + \overline{B} + 1. \tag{4}$$

Various new QCA designs have been presented for the 1-bit full adder. These designs can be classified into single-layer and multi-layer types (Mohammadi et al., 2016; Seyedi and Navimipour, 2018; Adelnia and Rezai, 2019; Heikalabad et al., 2020; Hasani and Navimipour, 2021). Layouts are designed in three QCA layers. Sasamal et al. (2018) and Erniyazov and Jeon (2019) used coplanar crossovers in their designs plus shifted (translated) some cells horizontally. In Ahmadpour et al. (2018) and Arani and Rezai (2018)'s layouts, some cells were also shifted. Shifting cells horizontally/vertically in the QCA layout is not a recomended approach. It increases the chance of a displacement fault. Gassoumi et al. (2021) and Salimzadeh and Heikalabad (2021) have

lowered the number of cells, but the simulation results showed that their outputs-signal strength is weak. Maharaj and Muthurathinam (2020) provided a novel design and used very few cells. However, the simulation results showed that its outputs unwantedly rise and fall at some of the edges.

3 Proposed QCA combinational logic circuits

In this section, the architecture of our proposed structures will be clarified. All designs, including the QCA layouts and inputs/outputs waveform, were validated by the QCA Designer-E version 2.2 (an extension of the QCA Designer version 2.0.3 of Walus et al. (2004)). In the QCA Designer-E designs, green, purple, cyan, and white cells represent the clock zones 0, 1, 2, and 3, respectively. The coherence vector (w/Energy) simulation engine was used to simulate the designs.

3.1 One-bit full adder

Fig. 7 shows our low-complexity 1-bit full adder layouts. This structure is designed on a single layer. To present a half adder using the proposed full adder, the polarization of C_{in} must be set to −1. As Fig. 6 illustrates, our proposed full adder consists of two gates, i.e., a majority and an XOR. Physical verification has been performed to ensure the correct operation of the XOR gate. For this purpose, the external electrostatic energies between the output cell and the others (kink energies) are calculated. It has been done by applying all possible combinations of inputs for the XOR gate. Here, an example is offered to illustrate that the gate works correctly. It has been assumed that the polarization of inputs A, B, and C_{in} is −1, 1, and −1, respectively. The interaction between cells (kink energy) can be obtained from Eq. (5). Then, the summation of kink energies (total electrostatic energy) U_{T} can be achieved from Eq. (6).

$$U_{ij} = \frac{1}{4\pi\varepsilon_0\varepsilon_{\text{r}}}\frac{q_i q_j}{d_{ij}} = \frac{kq_i q_j}{d_{ij}}, \tag{5}$$

$$U_{\text{T}} = U_{\text{T}x} + U_{\text{T}y} = \sum_{i=1}^{n} U_{ix} + \sum_{i=1}^{n} U_{iy}. \tag{6}$$

ε_0 and ε_{r} are vacuum and substance relative permittivity coefficients, respectively. q_i and q_j are the electron charges of dots in a cell, and d_{ij} is the space between these two dots. The energy must be calculated for all adjacent cells. The stable state is then defined clearly; i.e., it is the lowest summed energy obtained between the two output states. Fig. 8 shows two cases for the output cell with different polarization. The calculation of kink energies for both positions is tabulated in Table 1. By comparing the calculation results in these two cases, it can be concluded that the electrons inside the output cell will be located in position Fig. 8a because of the lower kink energy in contrast with that of Fig. 8b. Therefore, the output cell shows the binary value 1, which is the correct value.

The first proposed full adder has low complexity and area usage. Although one of its inputs is located at the center of the circuit, it can be used in multi-layer concepts with higher scalability and connectivity. The second and third proposed full adders are designed to be fully scalable. Their inputs and outputs are located around the circuit. The full adder 2 is built without any crossover. In the following, we use these structures in more complicated circuits.

3.2 Add/Sub circuit

The add/sub circuit is a combinational logic circuit that can sum or subtract two n-bit numbers by setting a value (0 or 1) for the selector pin. Fig. 9 shows our proposed add/sub QCA circuits. The circuit is transformed to a half subtractor or a half adder by setting the mode (M) pin polarization to +1 or −1, respectively.

3.3 Four-bit ripple carry adder

The structure of the ripple carry adder is based on cascading multiple 1-bit full adders. So, an adder with a higher number of input bits will be acquired. The C_{out} of each full adder block is the C_{in} of the next stage. If the C_{in} gets ignored at the first stage, the first full adder can be substituted with a half adder. So, the circuit sums two 4-bit numbers and displays the summation in 5 bits. Fig. 10 shows our proposed 4-bit ripple carry adders.

3.4 Four-bit ripple borrow subtractor

The structure base of the ripple borrow subtractor is the same as that of the ripple carry adder. As mentioned above, a full adder block and a NOT gate are

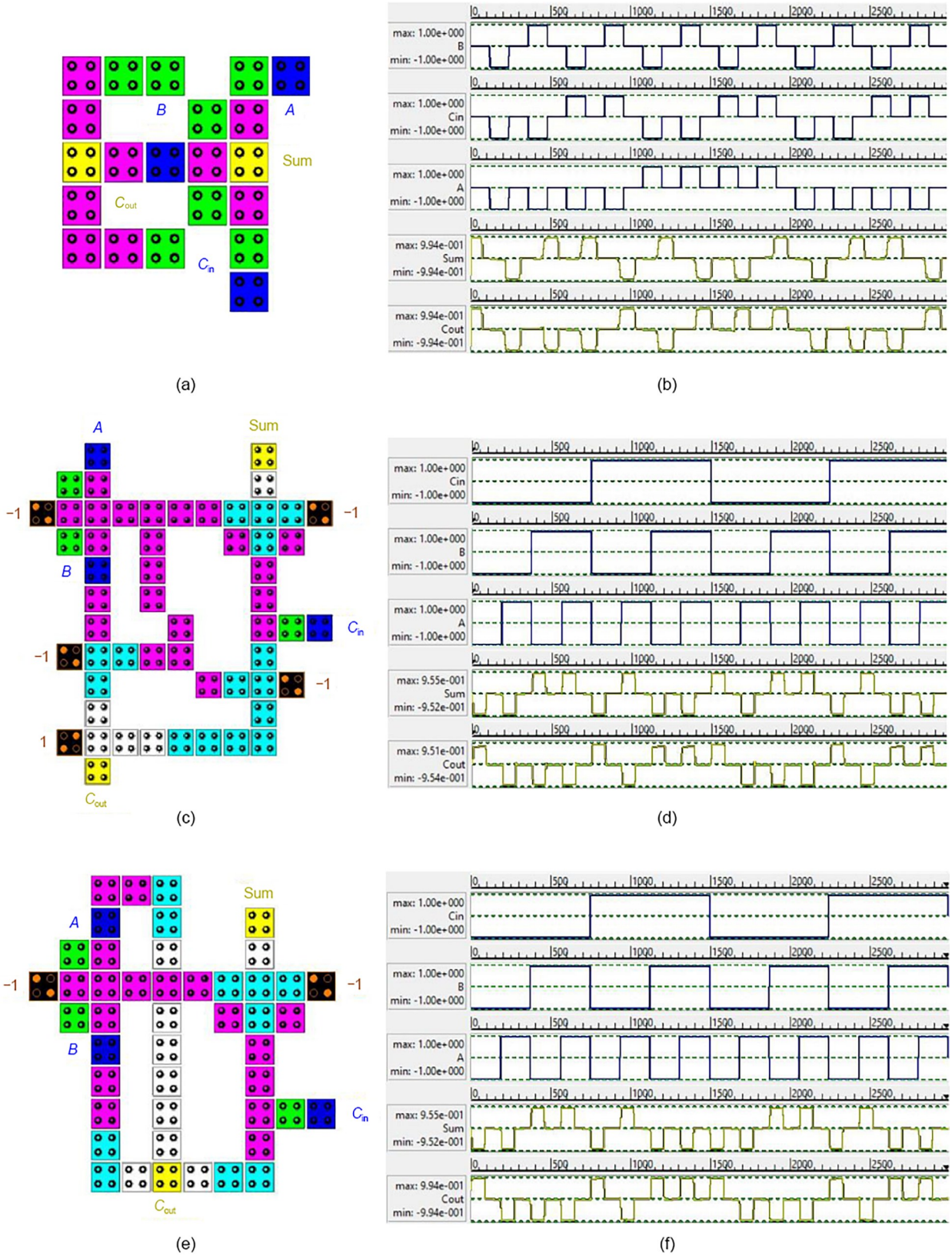

Fig. 7 Proposed 1-bit full adders: (a) full adder 1 QCA layout; (b) full adder 1 simulation results; (c) full adder 2 QCA layout; (d) full adder 2 simulation results; (e) full adder 3 QCA layout; (f) full adder 3 simulation results

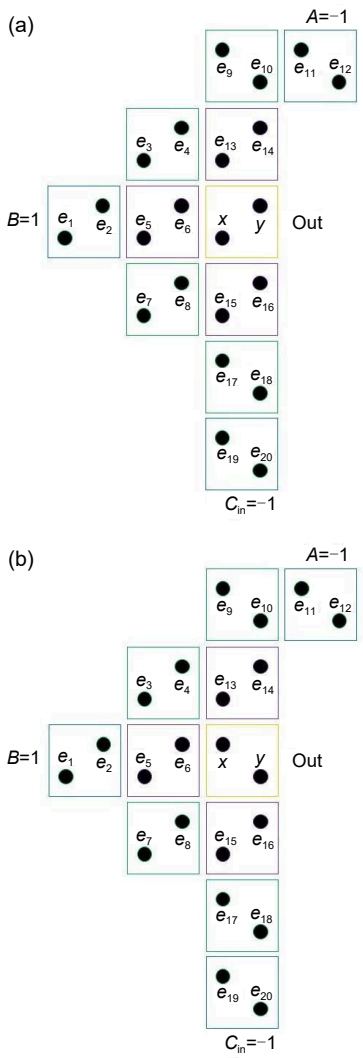

Fig. 8 Cells polarization in a case where the inputs (*A*, *B*, and C_{in}) are (−1, 1, and −1) by considering the output cell which shows 1 (a) and the output cell which shows −1 (b)

used to construct a subtractor. Fig. 11 shows our proposed 4-bit ripple borrow subtractors.

3.5 Two-bit array multiplier

An array multiplier is a combinational logic circuit used for multiplying two binary numbers by employing an array of AND gates and adders. Figs. 12 and 13 show the proposed 2-bit array multiplier structures and its simulation results, respectively. This circuit was designed on a single layer without any crossover.

4 Simulation and comparison results

In this section, the simulation results and energy dissipation for all proposed circuits are displayed. Also, our proposed full adder structure is compared with the most recent works.

4.1 Performance evaluation

Tables 2 and 3 show simulation setup parameters and performance evaluation of the proposed designs, respectively. The coherence vector (w/Energy) simulation engine allows designers to consider their system's energy dissipation. In the software QCA Designer-E version 2.2, Sum_bath and Avg_bath are the summation and average energies conceded to the bath within the complete simulation, respectively. Sum_clk and Avg_clk are the summation and average energies moved to/from the clock within the all-over simulation process, respectively (Abdullah-Al-Shafi and Bahar, 2018). More explanations about these energies and how they can be calculated were described in Walus et al. (2004).

4.2 Comparison results

There are two cost functions to evaluate QCA designs. One of the cost metrics is based only on the occupied area (A) and delay (T) with no consideration about the number of fundamental gates (majority and NOT gates) in the circuit. Eq. (7) shows this cost metric (Liu et al., 2014). The other metric is based on the numbers of inverters and majority gates. The crossover is important in this metric. Eq. (8) shows this cost metric which shows greater efficiency in QCA designs. In this metric, M, I, and C stand for the numbers of majority gates, inverters, and crossovers, respectively. T indicates the delay of the circuit, and k, l, p are the exponential weightings (Liu et al., 2014).

Table 1 Physical verification for Fig. 8: kink energies between adjacent cell electrons (e_1 to e_{20}) and output cell electrons (x and y)

Case	Applied kink energy to x electron (J)	Applied kink energy to y electron (J)	Total (J)
Fig. 8a	16.773e−20	14.791e−20	31.564e−20
Fig. 8b	17.210e−20	14.952e−20	32.162e−20

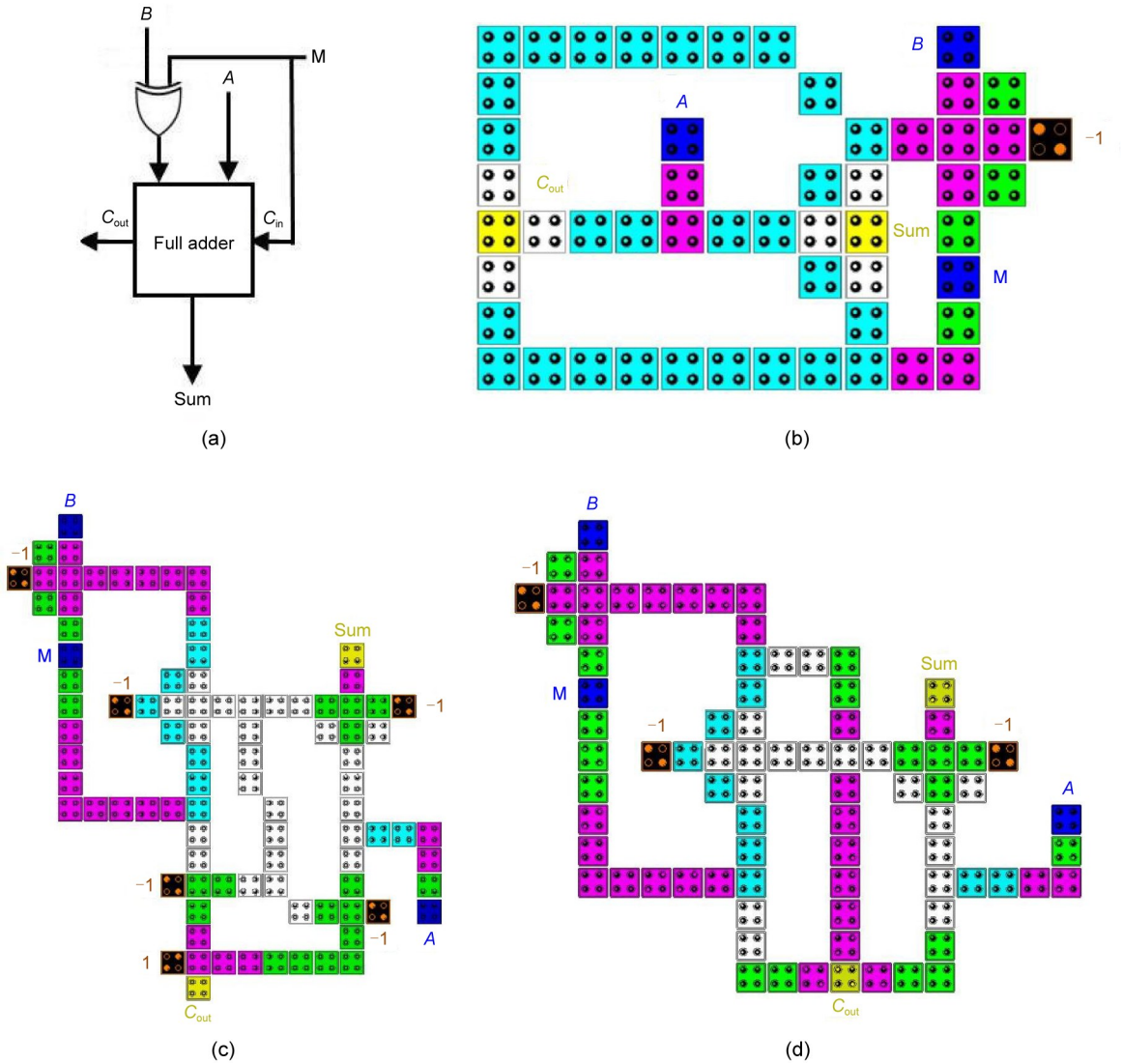

Fig. 9 Proposed 1-bit add/sub circuit: (a) logical diagram; (b) QCA layout 1; (c) QCA layout 2; (d) QCA layout 3

$$\text{Cost} = A \times T^2, \tag{7}$$

$$\text{Cost} = (M^k + I + C^l) \times T^p. \tag{8}$$

Table 4 shows the comparison between our proposed 1-bit full adder and recent ones. Only the single-layer-schematic designs without any rotating or shifting cells have been considered in this comparison.

Scalability and connectivity are important factors in designing extendable QCA circuits. The location of applying inputs should not disarrange the design architecture in larger circuits. All the inputs and outputs should be located around the circuit to make them easier to access, unless using them in multi-layer concepts. The designs whose inputs and outputs are located around the circuit are marked as scalable in Table 4.

Each clock zone should be configured with at least two cells to have stable and robust connectivity. The designs that have accounted for this point in their architecture are distinguished in Table 4.

All designs have been evaluated by both forms of cost metrics defined above. The exponential weightings (k, l, p) are considered to be (2, 2, 2), as was introduced in Liu et al. (2014).

The simulation results reveal that our circuits are superior in many aspects such as scalability, connectivity, complexity (cell count), area usage, delay (clock cycles), and energy dissipation. Also, in our

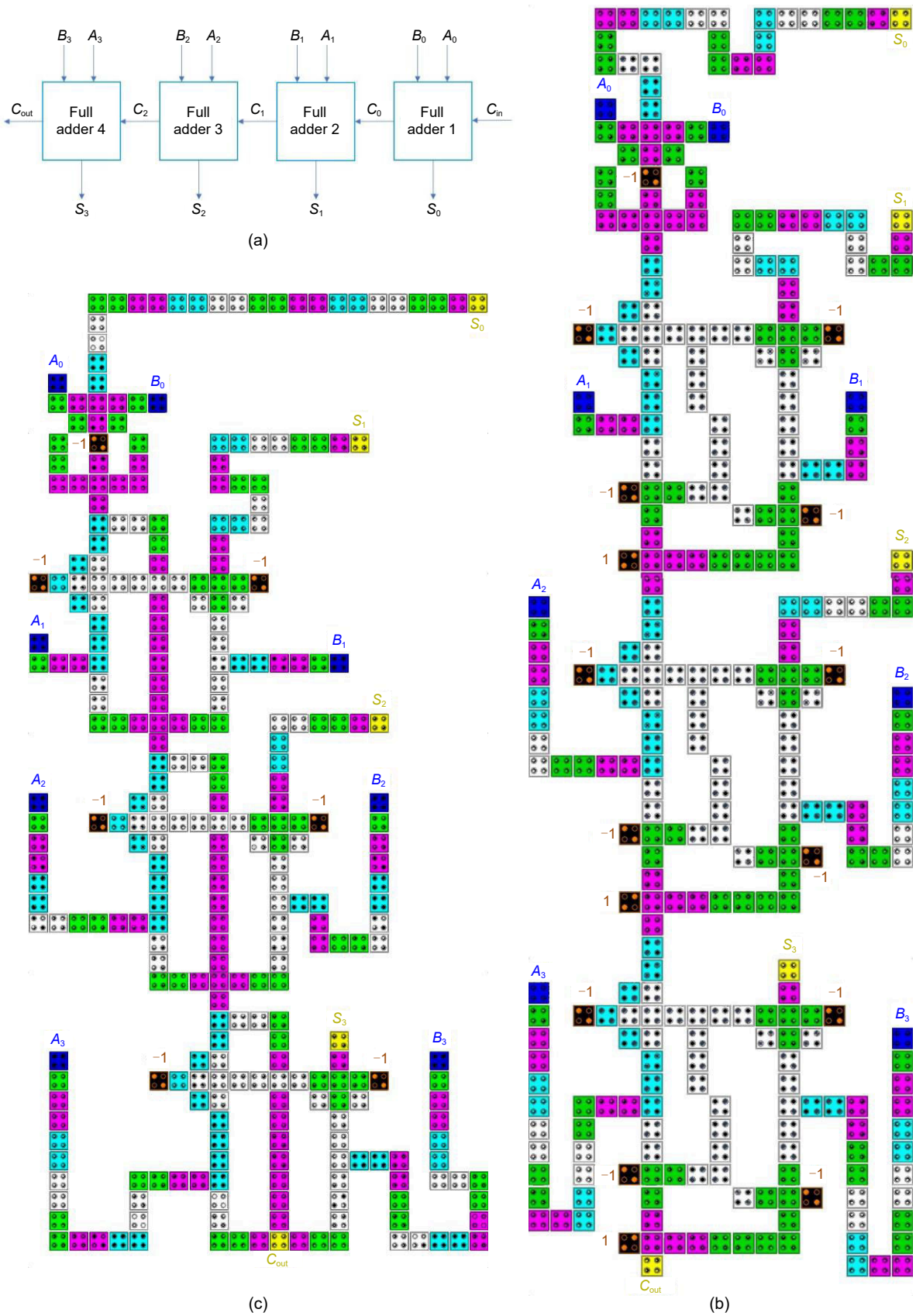

Fig. 10 Proposed 4-bit ripple carry adder: (a) logical diagram; (b) QCA layout 1; (c) QCA layout 2

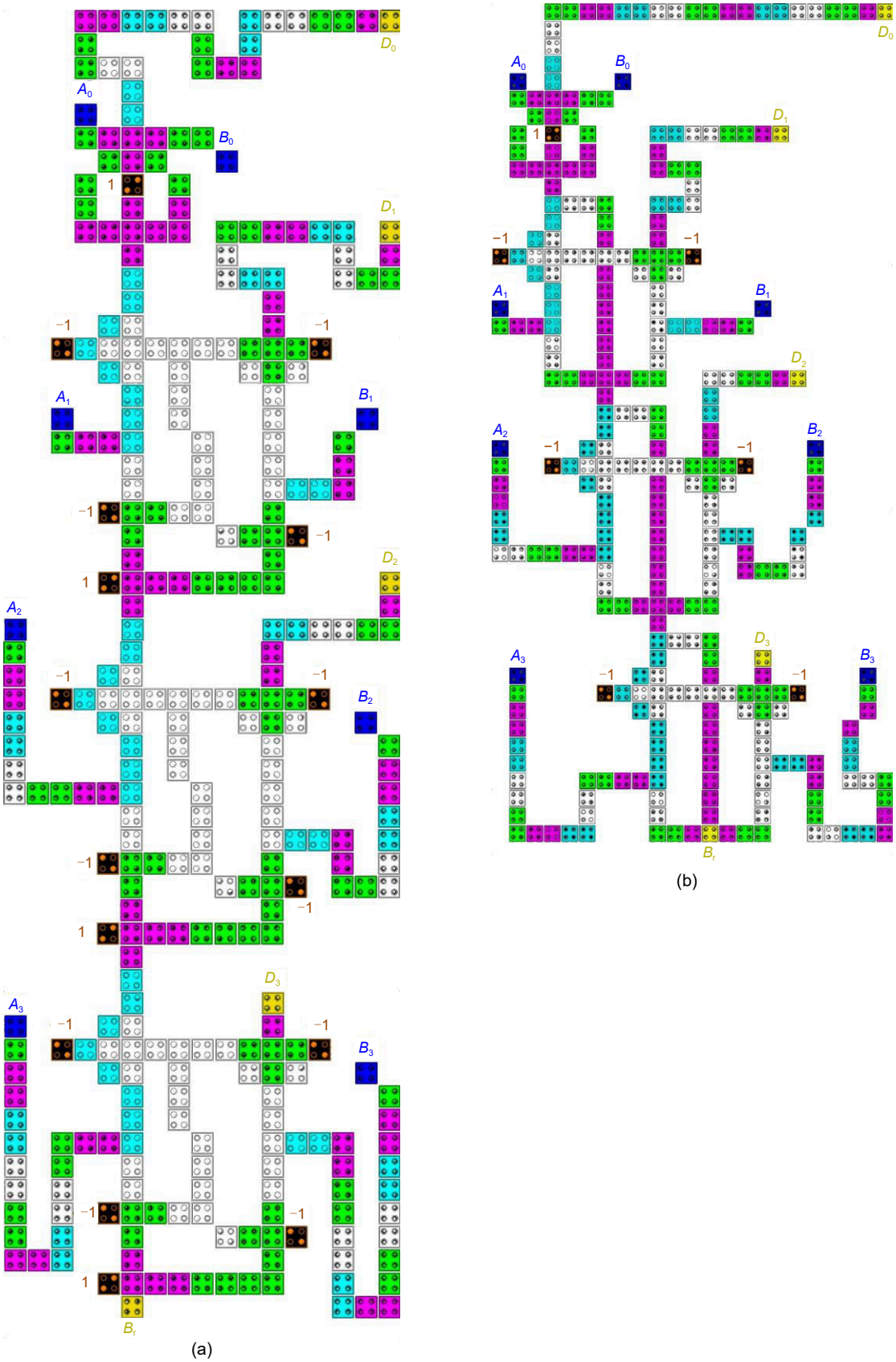

Fig. 11 Proposed 4-bit ripple borrow subtractor structures: (a) QCA layout 1; (b) QCA layout 2

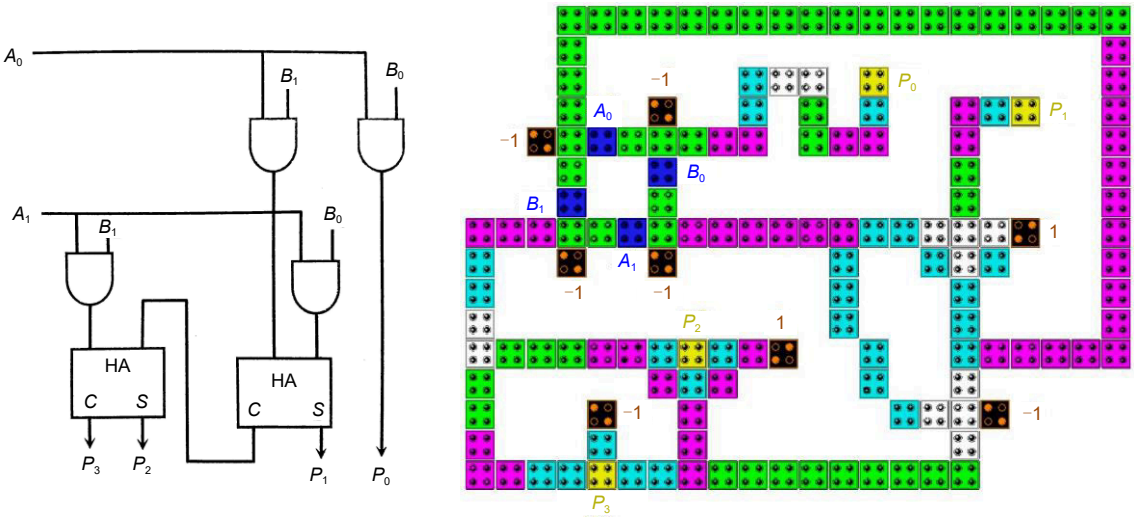

Fig. 12 Proposed 2-bit array multiplier structures: (a) logical diagram; (b) QCA layout

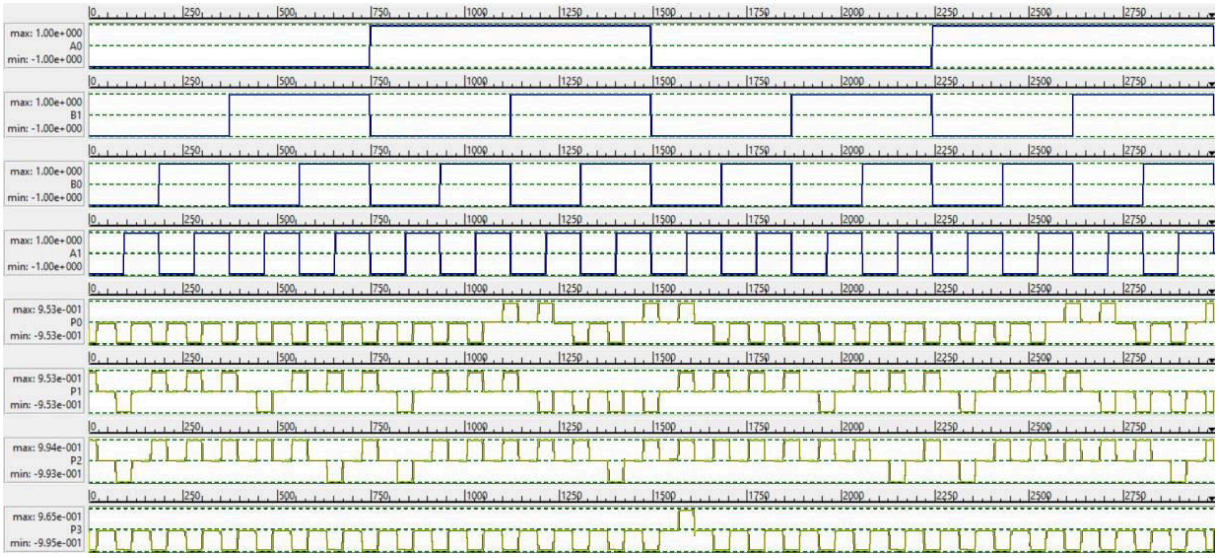

Fig. 13 Simulation results of the proposed 2-bit array multiplier

Table 2 The simulation setup parameters

Parameter	Value	Parameter	Value
Cell width (nm)	18.00	Total simulation time (s)	5.00e−011
Cell height (nm)	18.00	Clock high (J)	9.80e−022
Dot diameter (nm)	5.00	Clock low (J)	3.80e−023
Temperature (K)	1.00	Clock shift	0.00
Relaxation time (s)	1.00e−015	Clock slope Gauss (s)	1.00e−012
Clock period (s)	4.00e−012	Radius of effect (nm)	80.00
Input period (s)	4.00e−012	Relative permittivity	12.90
Time step (s)	1.00e−016	Calculation method	Euler method

Table 3 Performance evaluation of the proposed designs

Desgin	Number of cells	Delay (c.c)	Area (μm^2)	Sum_bath (eV)	Avg_bath (eV)	Sum_clk (eV)	Avg_clk (eV)
1-bit full adder 1	21	0.5	0.01	2.06e−2	1.87e−3	7.52e−4	6.83e−5
1-bit full adder 2	55	1	0.05	3.39e−2	3.09e−3	−1.72e−2	−1.60e−3
1-bit full adder 3	46	1	0.04	2.73e−2	2.48e−3	−2.80e−3	−2.55e−4
1-bit add/sub 1	53	1	0.04	3.15e−2	2.86e−3	−8.70e−3	−7.90e−4
1-bit add/sub 2	93	1.5	0.13	4.93e−2	4.48e−3	−2.96e−2	−2.70e−3
1-bit add/sub 3	83	1.5	0.11	3.90e−2	3.55e−3	−1.71e−2	−1.60e−3
4-bit RCA 1	331	3.5	0.38	1.44e−1	1.31e−2	−1.01e−1	−9.20e−3
4-bit RCA 2	309	3.5	0.44	1.14e−1	1.03e−2	−6.79e−2	−6.20e−3
4-bit RBS 1	332	3.5	0.38	9.83e−2	8.93e−3	−7.32e−2	−6.70e−3
4-bit RBS 2	310	3.5	0.44	9.02e−2	8.20e−3	−5.23e−2	−4.80e−3
2-bit array multiplier	145	1.75	0.14	6.28e−2	5.71e−3	−2.53e−2	−2.30e−3

RCA: ripple carry addrer; RBS: ripple borrow subtractor; (c.c): clock cycles

Table 4 Comparison of 1-bit QCA full adder designs

Reference	Number of cells	Delay (c.c)	Area (μm^2)	Total energy dissipation (eV)	Crossover	Scalability	Connectivity	Cost Eq. (7)	Cost Eq. (8)
Abdullah-Al-Shafi and Bahar, 2018	28	0.5	0.02	2.10e−2	Not required	×	√	0.005	3.25
Balali and Rezai, 2018	39	1	0.04	3.51e−2	Logical crossing	√	×	0.04	11
Heikalabad et al., 2018	41	1	0.03	3.48e−2	Not required	√	×	0.03	51
Babaie et al., 2019	26	0.5	0.03	2.45e−2	Not required	×	√	0.007	3.25
Mosleh, 2019	30	0.75	0.03	2.20e−2	Not required	×	×	0.016	7.312
Wang and Xie, 2019	45	1	0.05	2.53e−2	Not required	×	×	0.05	27
Majeed et al., 2020	37	0.75	0.04	2.23e−2	Not required	×	√	0.022	6.178
Safoev and Jeon, 2020	56	1	0.05	2.72e−2	Logical crossing	×	√	0.05	14
Wang and Xie, 2020	60	1	0.06	2.60e−2	Not required	×	×	0.06	53
Joy et al., 2021	61	1	0.06	2.93e−2	Not required	×	×	0.06	8
This paper (Proposed 1)	21	0.5	0.01	2.06e−2	Not required	×	√	0.002	3.25
This paper (Proposed 2)	55	1	0.05	3.39e−2	Not required	√	√	0.05	55
This paper (Proposed 3)	46	1	0.04	2.73e−2	Logical crossing	√	√	0.04	30

proposed circuits, outputs are designed in a single clock signal. This is an important issue in extended parallel-circuit design.

5 Conclusions

In this paper, we present optimal 1-bit QCA full adders. The proposed full adders are designed on a single layer with no rotated or shifted cells. One of our proposed 1-bit full adders is constructed out of 21 QCA cells with 0.5 clock cycle latency. The total occupied area and the energy dissipation are 0.01 μm^2 and 2.06e−2 eV, respectively. The others are designed to be fully scalable. Our full adders are compared with the most recent ones, and the results indicate their superiority. We have also designed other relevant arithmetic circuits. The 1-bit add/sub, 4-bit ripple carry adder, 4-bit ripple borrow subtractor, and 2-bit array multiplier are proposed and simulated.

Contributors

Hamideh KHAJEHNASIR-JAHROMI and Pooya TORKZADEH designed the research. Hamideh KHAJEHNASIR-JAHROMI processed the data and drafted the paper. Pooya TORKZADEH helped organize the paper. Pooya TORKZADEH and Massoud DOUSTI revised and finalized the paper.

Compliance with ethics guidelines

Hamideh KHAJEHNASIR-JAHROMI, Pooya TORKZADEH, and Massoud DOUSTI declare that they have no conflict of interest.

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