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INTRODUCTION

SRC-led materials research: 40 years ago, and now

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Abstract

Today, we are living through a pivotal moment when the semiconductor industry is moving towards 3D-integration including the close integration of logic and memory, the tighter integration of mixed-signal circuits, spintronic, embedded memories, sensors, communications, and improved power management. It is expected that 3D monolithic and heterogeneous integration will result in a new, truly multi-functional platform that drives continued system progress in the coming decades. Thus, over the next 40 years, the semiconductor industry will require significant innovation. At the heart of that is the need for significant contributions from the materials ecosystem to drive materials from the laboratory to the factory. For this perspective article, a selected group of distinguished SRC Scholars have been invited to present their research in the context of the potential impact that their work will drive for the future of microelectronics.

Introduction

Semiconductor Research Corporation, the world's first public–private partnership in semiconductor research, was formed in 1982. In retrospect, it is interesting to ask what we would not have today if basic semiconductor materials research had not been undertaken in such a way 40 years ago? Below we highlight just a few examples of how basic research conducted early in SRC's history has driven remarkable changes in people's everyday life:

1. The precise control of atoms in semiconductor materials—To make microchips with hundreds of millions and billions of transistors, it is critical to precisely control the positions of dopant atoms and point defects in semiconductor materials. A complete understanding was developed in 1981–1989 as a result of basic research by Prof. Plummer's group at Stanford through the support of SRC [1]. This basic research enabled the shrinking of critical device dimensions on a chip and led to the production of new generations of chip technology starting with the 130nm node, e.g., Intel and AMD microprocessors or Micron's Gbit-scale memory chips.
2. The degradation mechanisms in thin film insulators were understood in 1984–1990 as result of basic research by Prof. Hu's group at Berkeley, with support from SRC [2]. The degradation of insulating materials impacts the reliability and scalability of memory devices. This work opened the way for flash memory to become a mass storage medium. As an illustration, more than 10 billion NAND flash chips were sold in 2021, resulting in a revenue of $67.1 billion [3].
3. The "copper revolution"—New interconnect materials were needed to break the 1 GHz frequency barrier and

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reduce the power consumption of integrated circuits. The big challenge that industry faced was the replacement of aluminum interconnects, then the mainstream interconnect material, with copper, which required the development of an entirely new deposition and integration process to solve the severe reliability issues, such as copper diffusion and electromigration, observed in early attempts. SRC funded a basic research program on copper interconnects that started in 1989 (with research groups at RPI [4] and Cornell [5]) which resulted in the introduction of Cu interconnects in commercial products in IBM's PowerPC750 chip in 1998.

The above research was instrumental in driving the two-dimensional (areal) scaling of semiconductor devices and chips to its limits and enabled fantastic manufacturing technologies that we often take for granted today. Now, we are living through another pivotal moment when the semiconductor industry is moving towards 3D-integration techniques that will enable greater functionality per area including the close integration of logic and memory, the tighter integration of mixed-signal circuits, spintronics, embedded memories, sensors, communications, and even improved power management. It is expected that 3D monolithic and heterogeneous integration will result in a new, truly multi-functional platform that drives continued system progress in the coming decades.

With this transition, the industry faces major challenges on the manufacturing side arising from the aggressive introduction of new materials and interfaces. This includes all steps of semiconductor manufacturing, from front-end devices to back-end interconnects, advanced packaging, etc. (Fig. 1). There are many enabling process technologies required to support this transition which are currently in development. Overall, the practical processing of diverse materials at the atomic and mesoscale requires a deeper understanding of surface physics and chemistry as well as the development of new metrology methods. All this creates tremendous opportunities for the next generation of scientists and engineers, to unleash the next wave of semiconductor materials and integration schemes in ways that positively impact the next 40 years of semiconductor technologies. For this perspective article, a selected group of distinguished SRC Scholars have been invited to present their research in the context of the potential impact that their work will have on the future of microelectronics.

Expanding the semiconductor patterning toolbox with simultaneous deposition and etching

A key-emerging trend in semiconductor fabrication is chemically driven, bottom-up patterning by low-temperature area selective deposition (ASD) to augment top-down lithographic patterning. New approaches for ASD are becoming critical to achieve patterning and feature alignment needed for novel device designs. Important needs include ASD of metal interconnect materials in multilevel metallization, and ASD of dielectric materials to alter surface topography and mitigate edge placement error. Both atomic layer deposition (ALD) and atomic layer etching (ALE) are essential for fabrication, but these two processes are typically performed as separate operations. Recently, direct integration of deposition and etching, in both sequential deposition/etch cycles and as simultaneous

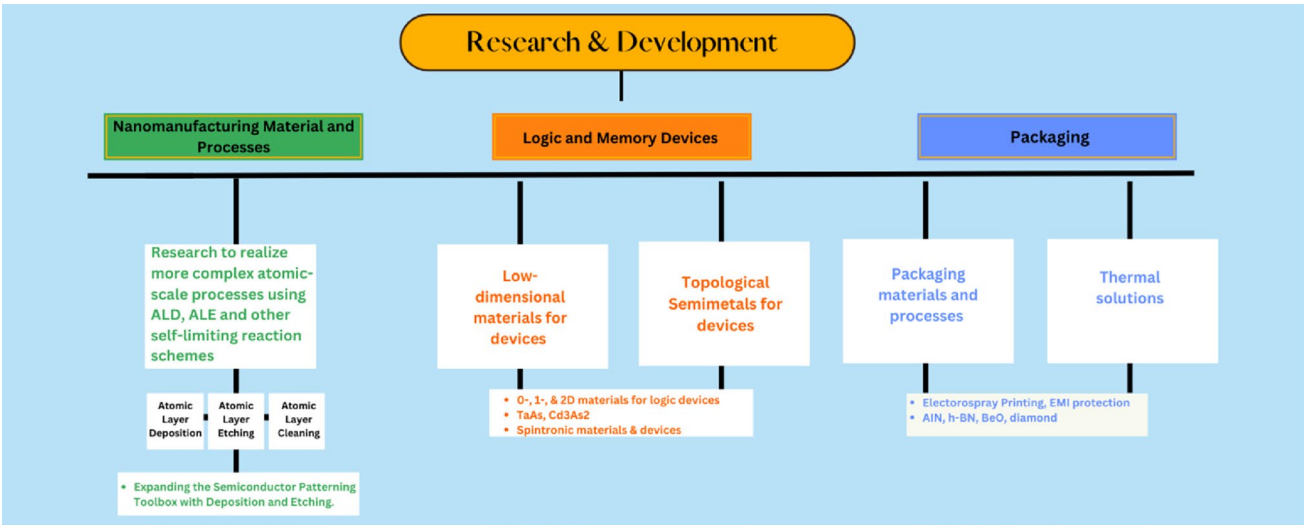

Fig. 1 Partial representation of SRC programs on microelectronics manufacturing with the topics of this perspective article as examples

co-processes, have provided fruitful new directions for ASD. ASD provides a route to build structures that are inherently self-aligned without costly lithographic and etching steps by using structures already present on the wafer to guide structure formation from the bottom-up. However, to advance the field of ASD-assisted patterning, more understanding is needed regarding mechanisms of thin-film nucleation, particularly when nucleation proceeds where thin-film deposition is not desired.

Studies of chemical vapor etching have revealed that some metal–organic vapor reactants used in semiconductor fabrication can be exploited to achieve two distinct outcomes. For example, trimethylaluminum (TMA) is widely used as a deposition precursor during ALD of solid Al_2O_3 films, but when it is exposed to solid AlF_3 within a desired temperature range, it can act as an etching reactant, where it undergoes ligand exchange to produce volatile aluminum-fluoro-methyl species. Therefore, on a surface with multiple materials exposed, if both deposition and etching are thermodynamically favorable within a shared temperature range, then deposition could occur on one surface while, simultaneously, under the same conditions, etching occurs selectively on an adjacent exposed surface in the absence of kinetic limitations. In this system, deposition is limited to the surface area being etched because the deposition reactant is consumed by the etching reaction. In principle, the process could proceed until the etched material is consumed.

Figure 2a shows a representative example of tungsten ASD using simultaneous deposition and etching where a pre-patterned TiO_2/Si–H surface is exposed to sequential pulses of SiH_4 and WF_6 gases at 220 °C. In this case, the WF_6 allows W deposition on the Si–H region, but on the TiO_2 surface, WF_6 produces volatile WO_2F_2 and TiF_4. As shown in Fig. 2b, we have also explored increasing the starting TiO_2 thickness to more closely monitor the changes in the exposed surfaces as the reaction proceeds. We find that while both reactions proceed favorably within a certain temperature range, they do so at different rates. For example, ALD is self-limiting, and the growth rate does not change significantly with temperature, but chemical vapor etching (CVE) is not self-limiting and the etch rate does change with temperature. This combination of temperature dependence and independence leads to interesting results, shown also in Fig. 2b.

In addition to the ASD results achieved so far, we expect that simultaneous deposition and etching can provide other capabilities not enabled by common processes. For example, as shown in Fig. 2c, we find that at low temperatures, W lateral overgrowth does not occur in the regions exposed by TiO_2 removal. Therefore, the critical dimension of the W features may be controlled by varying the starting TiO_2 pitch size. At moderate temperatures, another possible outcome

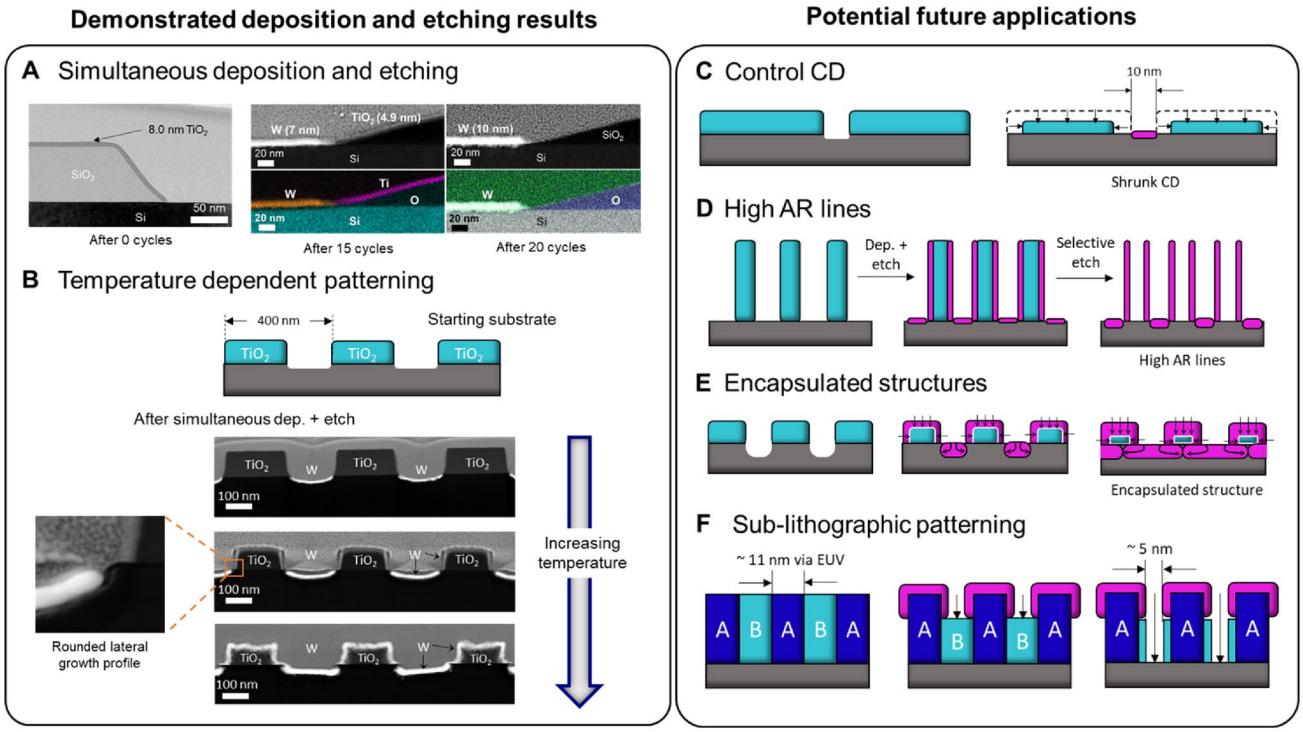

Fig. 2 Simultaneous atomic layer deposition and atomic layer etching

not yet tested is that high AR lines may be constructed by first patterning metal via simultaneous deposition and etching on the sidewalls and trenches of high AR lines and then removing the remaining sacrificial material with a selective etch back, as shown in Fig. 2d. At high temperatures, both the sacrificial material and underlying substrate are consumed rapidly by the etchant, resulting in growth in both regions. In this case, the film is discontinuous as shown in Fig. 2b and begins to grow underneath the SiO_2 support in the Si regions. We expect that extending high-temperature deposition and etching will cause the sub-surface lines to coalesce, creating a fully encapsulated structure as shown in Fig. 2d. On a coplanar-patterned substrate, we expect that the desired material will grow laterally onto the sidewalls of the growth surface as they are exposed by removal of the adjacent sacrificial material. Then, we expect that a line-of-sight selective-etching process will remove the exposed sacrificial material and leave behind the material that is "masked" by the metal features (Fig. 2f). Therefore, simultaneous deposition and etching may be exploited in future semiconductor fabrication for the potential of sub-lithographic patterning CD's.

Two-dimensional materials and devices

Advancement of the semiconductor industry necessitates a continuous improvement in integrated circuit (IC) performance, decrease in device dimensions, and reduction in production costs. Although many materials innovation efforts—including the adoption of copper interconnects, high-*k* dielectrics, and metal gates, along with the exploration of alternative device architectures—have been introduced to meet these objectives, further size reductions in silicon-based circuits risk increased power consumption and limited performance gains. To sustain effective scaling, the exploration of alternative material paradigms is paramount.

Two-dimensional (2D) materials such as graphene, transition metal dichalcogenides (TMDs), and emerging candidates such as silicene and germanene open-viable avenues to scale down channel thicknesses to the atomic level, enhance electrostatic control, and mitigate short channel effects [6]. Moreover, the weak van der Waals bonding inherent in 2D materials enables facile assembly of heterostructured stacks, exhibiting superior properties compared to the constituent materials alone. Therefore, 2D materials offer a promising route towards devices that can be integrated into complementary metal–oxide–semiconductor (CMOS) chips with enhanced scaling compared to silicon, allowing Moore's law to continue for additional decades with exponential increases in compute performance vs. power.

For these reasons, 2D materials have already found their place in logic scaling roadmaps of many major semiconducting companies, and co-integration of 2D materials with silicon CMOS technology has become a desirable objective. However, to achieve successful integration of 2D materials into devices, a firm knowledge of fundamental materials processes, encompassing oxidation, interfacing, etching, defect formation, and contact engineering within the 2D system, are required. Owing to the van der Waals-bonded surfaces of 2D materials, these processes can be significantly different to those present in covalently bonded silicon or germanium [7].

We here draw attention to one key example where fundamental knowledge of 2D material properties is crucial—the issue of TMD oxidation, from understanding chemical processes at the level of atoms, to projecting the importance of controlled oxidation for future microelectronic manufacturing. Control over oxidation is among the most critical aspects of semiconductor processing. This is evident in the evolution of traditional semiconductors, most importantly silicon, where process control challenges contributed to the decades lag between MOSFET patents and their commercialization [8]. Precise control of oxidation mechanisms is no less crucial for microelectronic integration of emerging layered and 2D semiconductors, such as TMDs, which are prone to oxidizing under a range of conditions [8, 9]. Uncontrolled oxidation can limit device performance, while controlled oxidation can enhance functionality, such as surface passivation, semiconductor-dielectric interfaces, and resistive switching [10, 11].

Our work focusses on oxide formation mechanisms of MoS_2, the most widely studied TMD semiconductor. Previous work has shown that MoS_2 is resistant to oxidation under ambient conditions, but it can oxidize under dry (O_2) and wet ($O_2 + H_2O$) thermal conditions [12, 13]. Oxidation can be accelerated by defects, illumination, and organic absorbates, and has been observed to cause layer-thinning and self-limited amorphous oxide formation in device-processing environments like ozone, plasma, and wet etchants [13–15]. Many of these studies provide important kinetic insights at the micron scale; however, as current devices shrink to one or two atomic layers, understanding oxidation mechanisms at the nano- and atomic scale becomes crucial for material integration into advanced technology nodes [13, 15].

Our work builds on current state of the art to understand the *atomic-level kinetics* of MoS_2 oxidation, towards morphology and phase control of the resulting semiconductor/oxide interface [16]. We also highlight the use of correlative metrology techniques, scanning transmission electron microscopy (STEM), and spectroscopic ellipsometry (SE), in oxidative processing. Figure 3a, b shows STEM images of MoS_2 thermally oxidized in 0.2 atm O_2 at 500 °C for 1 h, resulting in the formation of blocks of layered, crystalline α-MoO_3 with textured relationship to the underlying MoS_2. We observe a shoulder in the electron energy loss

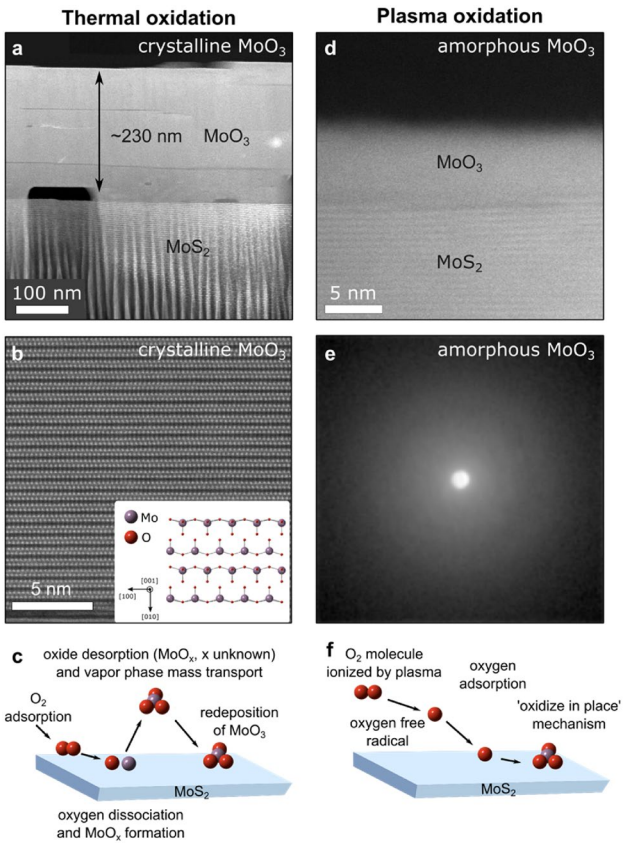

Fig. 3 Kinetic control of MoS_2 oxidation. **a** Cross-sectional STEM image of freshly exfoliated MoS_2 oxidized at 500 °C for 1 h in 0.2 atm O_2. The darker region beneath each void and the vertical wrinkles in the substrate are curtaining artifacts caused by focused ion beam (FIB) preparation. **b** Atomic-resolution STEM high-angle annular dark field (HAADF) image of MoO_3 lattice (Mo atoms visible). Inset: corresponding atomic model looking down the MoO_3 [001] zone axis. We use conventional indexing for α-MoO_3, with the long axis along $\hat{b}$. **c** Proposed model for MoS_2 thermal oxidation showing vapor phase mass transport and redeposition. **d** Cross-sectional STEM image of MoS_2 produced via radiofrequency (RF) oxygen plasma. **e** Convergent beam electron diffraction (CBED) pattern from a STEM nanodiffraction dataset averaged over the plasma MoO_3 film. The absence of diffraction spots in the CBED pattern indicates that the film is amorphous. **f** Proposed model for MoS_2 plasma oxidation showing oxidize in place mechanism. Figure panels adapted from [* MERGEFORMAT 17]

spectra (EELS), consistent with a non-negligible concentration of oxygen vacancies and sulfur incorporation in the α-MoO_3 layer [17, 18]. Experiments with remote substrates and patterned MoS_2 indicate that thermal oxidation proceeds via vapor-phase mass transport and redeposition (Fig. 3c). We show that this is promising for islanded, crystalline, and textured semiconductor/oxide interfaces—such as those often desired in catalytic applications—but a challenge to forming thin, conformal oxide films required in planar device processing.

In contrast, oxygen plasma processing is known to produce thin and conformal amorphous MoO_3 layers on MoS_2, via an 'oxidize in place' mechanism [15]. Our studies characterize the atomic-scale morphology, phase, and kinetic formation of this conformal oxide (Fig. 3d–f). We provide guidelines for device processing, using SE to map how the thickness and roughness of the amorphous MoO_3 layer vary with oxidation time and plasma conditions [17]. The plasma oxidation process exhibits a near-constant < 5 nm oxide thickness for processing times of 20 min or longer. We also use EELS to show that the band gap of the resulting oxide layers varies based on their crystallinity and oxygen vacancy concentration. The band gap of amorphous MoO_3 produced via oxygen plasma processing is estimated to be 3.6 ± 0.1 eV, while the band gap of crystalline α-MoO_3 produced via thermal oxidation is estimated to be 4.1 ± 0.1 eV [17]. By understanding the interplay between atomic-scale growth kinetics, both crystalline and amorphous phases as well as islanded and thin-film morphologies can be tailored via TMD oxidation. For example, amorphous conformal oxide layers could be processed in desired thickness via oxygen plasma, followed by light thermal or laser annealing to induce crystallization, if conformal crystalline properties are desired; conversely, thermal oxidation could be utilized to create crystalline, facetted MoO_3 islands on masked substrates, followed by plasma amorphization if desired.

Such kinetic control of atomic structure and thin-film morphology can aid in the processing of TMD devices to limit uncontrolled oxidation, perform controlled etching, and design 2D semiconductor/oxide heterojunctions for desired applications. For example, MoO_3 is often considered too conductive act as an effective dielectric for transistors but is useful as high work-function contacts or in memristive and memcapacitive switching [12]. Control of oxide structure, defect concentration, and interface morphology are particularly crucial here, and we look forward to further studies of how plasma processing parameters affect properties such as hole transport, passivation, and resistive switching capabilities. Controlled oxidation of other TMDs, such as $HfSe_2$ or $ZrSe_2$, may result in high-k dielectric/semiconductor interfaces, which would require conformal planar processing [19]. In the future, we envision that high-throughput STEM metrology combined with correlative SE data collection will streamline oxidative TMD processing and determination of atomic-scale mechanisms for a wide variety of TMD materials [20]. Our work illustrates how TMD oxidation differs significantly from oxidation of legacy semiconductors, most notably silicon, and that detailed kinetic understanding of the competing oxidation processes is essential for future TMD device integration. It is worth noting that oxidation is just one example of fundamental materials processes that are essential to understand for 2D material CMOS integration. Other scientific and technical challenges include identifying

low ohmic contact materials, interfacing with gate dielectrics, atomically precise doping, and defect engineering [21–23]. Understanding these processes at the atomic scale will allow us to surpass current CMOS material limitations by manufacturing a novel class of nanoscale devices utilizing low-dimensional materials.

Spin-dependent phenomena in topological semimetals

The discovery that the topology of the band structure of a solid can have dramatic implications over its macroscopic behavior has completely changed the way we approach material science and condensed matter physics [24]. Topological classification has allowed us to look past the details of different materials and consider large families of them that share common properties [24, 25]. Some of the topological aspects of these materials (like the presence of spin polarized surface states, a high electrical conductivity and high-spin orbit coupling) make them ideal candidates to be used in electronic devices that function using the spin of the electron [26, 31]. This has given birth to a nascent field of technology called topological spintronic. These devices are useful for spin sensing and to make low power non-volatile magnetic random-access memory. They have an advantage in applications where low energy consumption and high-fidelity storage (even in the absence of power) are of vital importance. For this reason, spintronic devices have been used in aerospace and automotive applications. [27, 28] Moreover, a non-linear device that switches between two states can be thought as a perceptron, which is the basic building block of a neural network and could allow the implementation of machine learning systems on chip with lower power consumption and a higher level of bio-fidelity for different artificial intelligence applications [29]. In this context, we have used a bottom-up approach and investigated new families of topological materials that can be used in spintronic. We report the synthesis and spin-dependent transport characterization of Cd_3As_2 and TaAs which are archetypal members of the families of topological Dirac and Weyl semimetals [30, 31]. We show that like topological insulators, it is possible to control the spin of electrons on these new families of topological materials using electrical means via the spin Hall and Rashba-Edelstein effects [32, 33] and show that they are promising candidates for the next generation of spintronic devices.

We have used molecular beam epitaxy to synthesize thin films of Cd_3As_2 and TaAs in different III, V-compatible substrates (GaAs, GaSb) in a manner described elsewhere [34, 35]. Among different characterization techniques, we use high-angle annular dark-field transmission electron microscopy (HAADF-TEM) (Fig. 4c, e) to understand the

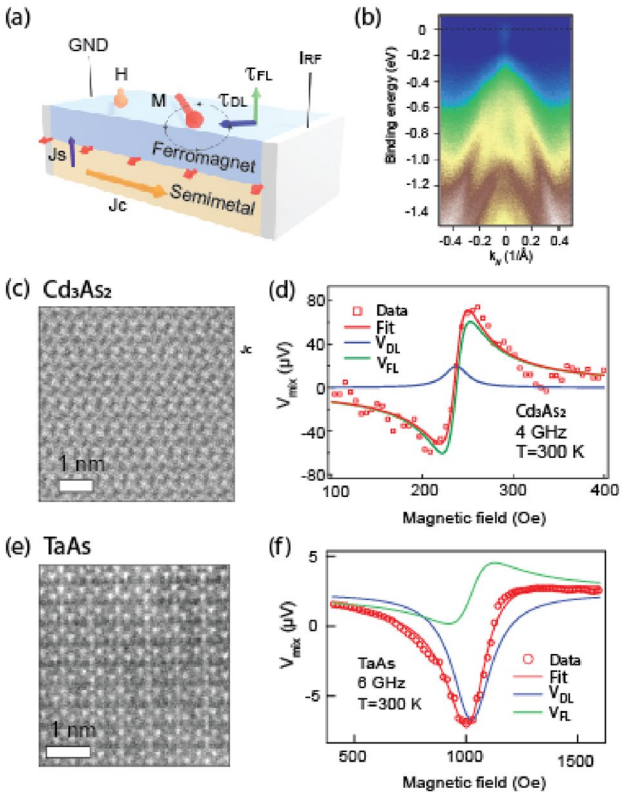

Fig. 4 **a** Schematic diagram of the devices used for spin transport measurements. **b** Energy spectrum showing Dirac fermion behavior in thin films of Cd_3As_2 obtained using angle-resolved photoemission spectroscopy (ARPES). **c** and **e** High-angle annular dark-field transmission electron microscopy (HAADF-TEM) image showing the crystal structure of Cd_3As_2 and TaAs thin films. **d** and **f** Spin torque ferromagnetic resonance (ST-FMR) spectra used for the determination of the charge to spin conversion efficiency in topological semimetals. We show the data and fits that correspond to the damping like and field like torques in the heterostructure. Figure adapted from Fig. 1, 2, 3 in [* MERGEFORMAT 34] and Fig. 2, 3 in [* MERGEFORMAT 35]

microscopic structure of our films and combine it with angle-resolved photoemission spectroscopy (ARPES) (Fig. 4b) to precisely determine the quantum state (energy and momentum) of the electrons in the crystal. This level of understanding of our system is fundamental for fast discovery, synthesis, and optimization of these families of materials and for theoretical modeling and prediction of its quantum properties.

Considering the impact that these materials can have in technology, we have focused on understanding the macroscopical physical implications of spin in the electrical behavior of topological semimetals. We have combined Cd_3As_2 and TaAs films with a soft ferromagnet (permalloy, NiFe) and studied the interconversion between charge and spin. In our experiment, we pattern 50×10 um bars and apply radiofrequency electrical current to the

heterostructure. This produces a flow of angular momentum (spin current) towards the ferromagnet due to the spin Hall or Rashba-Edelstein effects. Under the right conditions of radiofrequency and external magnetic field, the magnetization of the ferromagnet is going to process due to the torque produced by the spin current generated in the topological semimetal. This spin torque-induced ferromagnetic resonance (ST-FMR) phenomenon can then be measured as a rectified voltage in the heterostructure (Fig. 4d and f), produced due to the varying anisotropic magnetoresistance of the ferromagnet. The spectra can be fitted using a symmetric and antisymmetric Lorentzian distribution corresponding to the damping-like and field-like torques applied on the magnetization of the ferromagnet. Using this information, we can compute the efficiency ξ_{FMR} of the charge-spin conversion (Eq. 1) which is proportional to the ratio of the amplitudes of these distributions and geometrical and physical factors of the heterostructure [34, 35].

$$\xi_{FMR} = \frac{V_S}{V_A}\left(\frac{e}{\hbar}\right)\mu_0 M_S t_{SM} t_{NiFe}\left[1+\left(\frac{M_{Eff}}{H_{Res}}\right)\right]^{\frac{1}{2}}. \quad (1)$$

Here, V_S (V_A) is the amplitude of the symmetric (antisymmetric) Lorentzian distributions, $\hbar$ is the reduced Planck constant, e is the charge of the electron, μ_0 is the permeability of free space, $M_S = 560kA/m$ is the saturation magnetization of permalloy, t_{SM} is the thickness of the topological semimetal, t_{NiFe} is the thickness of the ferromagnet, M_{Eff} is the effective magnetization obtained from fitting the Kittel ferromagnetic resonance equation to the spectra, and H_{Res} is the magnitude of magnetic field at which the resonance happens.

We have determined that the charge-spin conversion efficiency in Cd_3As_2 ($\xi_{FMR} = 0.10$) and TaAs ($\xi_{FMR} = 0.27$). These values can be combined with the electrical conductivity σ of these materials to determine a lower bound on their spin Hall conductivity $\sigma_{SH} \geq |\xi_{FMR}|\sigma$ due to the imperfect transparency at the topological semimetal/ferromagnet interface. We obtain the spin Hall conductivity to be $\sigma_{SH} = 63\frac{\hbar}{e}\frac{S}{cm}$ in Cd_3As_2 and $\sigma_{SH} = 424 \pm 110\frac{\hbar}{e}\frac{S}{cm}$ in TaAs [34, 35]. These efficiencies effectively show that is possible to electrically control the spin of electrons in the Dirac and Weyl families of topological semimetals and make them ideal candidates for the next generation of low power magnetic memory. We hope that future improvements on material synthesis will allow us more control of the heterostructure and allow us to better understand the intrinsic and extrinsic mechanisms of the charge to spin charge to spin conversion in these families of topological materials and the role of topology on spin transport.

Thermal materials

Three-dimensional (3D) heterogeneous integration, or stacking-integrated circuits vertically, is one approach to continuing Moore's law. 3D vertical stacking not only increases transistor density per unit area but also opens pathways for more efficient computing. For example, it has been proposed that by physically reducing the distance between (traditionally separate) memory and computation through vertical stacking, it is possible to reduce the time and energy required to shuttle data between them, leading to more energy efficient and powerful methods of computing [36]. In recent years, the 3D stacking approach has been utilized by semiconductor manufacturers at the chiplet level (e.g., Intel's Foveros) [37]. Foveros utilizes traditional CMOS fabrication on separate substrates, and face-to-face bonding of chips using wafer-packaging techniques to enable stacking. However, this approach is ultimately limited in the number of layers that can be stacked. To overcome the constraints of chiplet stacking, one approach is monolithic 3D stacking, which emphasizes sequential fabrication of device layers on top of previously fabricated layers, all atop a single substrate.

Engineering monolithic, three-dimensional (3D) stacked, high-density memory, and computation demand two critical thermal and material considerations: back-end-of-the-line (BEOL) compatible deposition temperatures (< 500 °C) [38–40] and high thermal conductivity for effective heat dissipation within the stacked layers. Dielectrics which fulfill both criteria are extremely difficult to obtain and require a fundamental evaluation as heat spreaders, passivation layers, and thermal interface materials (TIMs) within densely packed systems.

Scalable, BEOL temperature-compatible deposition techniques suitable for the semiconductor industry include atomic layer deposition (ALD), sputtering, and chemical vapor deposition (CVD) [40]. Instead of relying on thermal energy from high-temperature processes, these techniques may utilize the energy of plasma or high energy electrons [41, 42]. These deposition techniques offer a high degree of control over tuning electrical conductivity, enabling deposition of dielectrics, semiconductors, and metals. In contrast, precise engineering of phonon transport poses a major challenge to the deposition of *high thermal conductivity* dielectrics. For example, silicon oxide and silicon nitride can be deposited at low temperatures, but only as amorphous, defective films with low thermal conductivities on the order of 1 W/m/K. Conversely, the high thermal conductivities (> 50 W/m/k) of wide band gap materials such as diamond, aluminum nitride (AlN), and hexagonal boron nitride (hBN) are facilitated by strong covalent bonds and a high degree of crystallinity, both of which are

typically achieved only by deposition or synthesis at high temperatures (Fig. 5).

For BEOL compatible thermal budgets, recent advances in low temperature deposition methods of various wide band gap materials with high theoretical thermal conductivities merit closer inspection. Recently, aluminum nitride (AlN) has been reported to be able to be deposited at BEOL compatible temperatures via sputtering [43]. Additionally, electron-enhanced atomic layer deposition (EE-ALD) has been used to deposit turbostratic boron nitride (BN) at room temperature [44]. Low-temperature chemical vapor deposition of diamond is another promising technique for integrating wide band gap heat spreaders at low temperature [45].

To complement low-temperature depositions, other techniques may be considered, including low-temperature material integration processes that allow highly crystalline materials to be grown at high temperatures and transferred to arbitrary substrates at significantly lower temperatures. Such methods have been demonstrated in fabricating electronic devices out of Van der Waals materials [46] and offer promise for large area, scalable transfer of high thermal conductivity, wide band gap (e.g., hexagonal Boron Nitride) thin films for thermal management.

Understanding and tuning thermal conductivities and boundary resistances are critical to regulating heat transport within complex systems. For densely packed integrated circuits, overheating and thermal degradation are major factors contributing to semiconductor device failure. In 3D-stacked systems, heat buildup necessitates effective heat dissipation from hotspots (with high thermal conductivity materials), while also considering the need to shield devices from hotspots in the vicinity (using low thermal conductivity materials). Refinement of various low-temperature material deposition and transfer techniques offers many exciting opportunities for the future of high thermal conductivity heat spreaders within 3D systems.

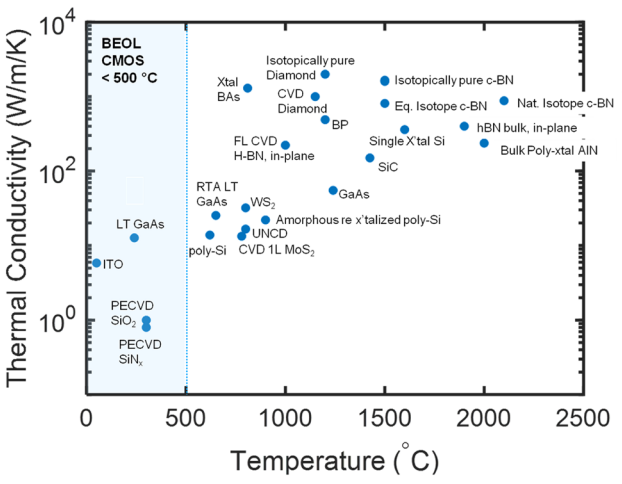

Fig. 5 Room-temperature thermal conductivity vs. synthesis or deposition temperature for various materials. The upper left corner of the plot represents the ideal heat spreader which has high thermal conductivity and the ability to be deposited at low temperature. (Reproduced with permission from Perez et al. "High Thermal Conductivity of Sub-Micron Aluminum Nitride Thin Films Sputter-Deposited at Low Temperature", ACS Nano, in press (2023) and Chen et al. "Electrical and Thermal Properties of Boron Nitride Thin Films Deposited at Room Temperature" *in preparation*)

Low-temperature diamond as an effective self-heating spreader

The rising demand for higher power density in electronic applications, from dense computing (e.g., 3DICs) to 5G/6G networks, makes thermal management in devices both crucial and challenging. Joule heating followed by localized high-temperature spikes in the device channel or other power delivery points cause performance degradation and premature failure. These effects can be mitigated by developing of novel approaches using highly thermally conductive polycrystalline diamond to increase the heat transfer coefficient from the channel to the heat sink [47, 48].

Integration of diamond to the top of the electronic devices, in a close proximity to the channel, can be achieved through modified direct chemical vapor deposition techniques [49]. The standard diamond growth temperature using CVD techniques varies between 600 and 1000 °C, which makes this process suitable only for high thermal budget materials and not compatible with low-thermal budget materials and device-level integrations. Therefore, to expand the effective diamond growth window, it is required to lower the temperature to < 400 °C to be compatible not only with low thermal budget material technologies but also with back-end-of-line processes. While low-temperature (LT) diamond was reported between 100 and 500 °C in various gas systems such as $O_2/CH_4/H_2$, $CO_2/CH_4/H_2$, Ar/CH_4, CO/H_2, $CO/O_2/H_2$, and $Ar/CH_4/H_2$, the resulting quality of the LT-grown diamond was not comparable in its properties to the high-quality high-temperature (HT)-grown diamond [50, 51].

We have shown that for higher-quality diamond growth at temperatures < 500 °C in addition to gas chemistry adjustments from H_2/CH_4 to $CO_2/H_2/CH_4$ or $O_2/H_2/CH_4$, an optimized nucleation layer is critical [52]. Adding oxygen to the chamber during the growth enhances sp^2 carbon etching by breaking the double C=C bonds (due to the high electronegativity of oxygen atoms) and providing reaction sites for single C–C bonds (sp^3 carbon). Using this method, we were able to grow stress-mitigated diamond grains at 400 °C with considerably similar shapes and phase purity (97.1%) to HT diamond grains grown at 700 °C in wafer scale (Fig. 6a and c). The anisotropy ratio (Thickness/Grain Size) was reduced from > 10 to 1.21, with multiple optimization techniques,

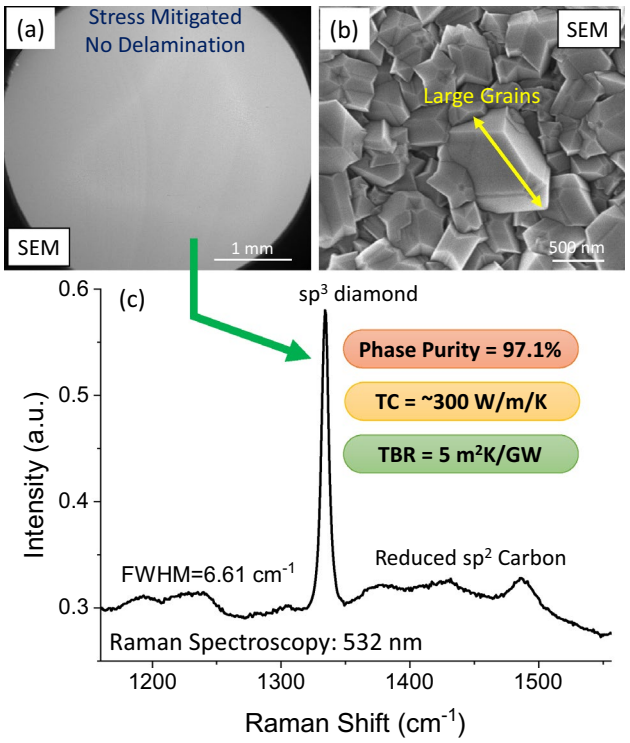

Fig. 6 SEM micrographs showing **a** large-scale uniform diamond growth with **b** low anisotropy ratio. **c** Raman spectra of the LT diamond with sharp sp^3 peak and reduced sp^2 carbon signature

bringing it closer to an anisotropy ratio of 1.12, which was achieved previously by our group only with HT growth [53] (Fig. 6b). This grains offered a relatively high thermal conductivity ($TC_{LT} \approx 300$ W/m/K, [52]) on a ~ 600–800 nm-thick diamond due to the reduced phonon scattering rate in the lateral direction, aided by their low anisotropy. The thermal boundary resistance (TBR) between LT diamond and the substrate was measured to be 5 m^2K/GW, only ~ 2 m^2K/GW higher than HT diamond TBR of 3.1 m^2K/GW (was reported previously by our group [53]). The low TBR is due to the abrupt and high-quality sp^3 carbon nucleation at the interface (confirmed by EELS analysis [52]).

LT diamond enables diamond integration on various semiconductor technologies such as Si, GaN, SiC, InP, and Ga_2O_3, and opens up a pathway for heat spreading solution for wider applications that were not achievable in the past.

Packaging materials and processes

Thin films of metallic, polymeric, and semiconductor materials support a multi-disciplinary range of applications. In electronics manufacturing, thin films are used to aid or inhibit thermal transport [54, 55], provide moisture and corrosion protection [56, 57], and modify surface conductivity [58]. The next generation of microelectronics requires advanced packaging with outstanding thermal, mechanical, and electrical functionalities [59]. This will require improved thin-film materials and novel approaches for their deployment.

Electrospray printing is a low-cost, additive manufacturing technique that creates thin films with tunable surface morphologies [60, 61]. A precursor solution composed of a solute material (i.e., polymers, metals, etc.) in a volatile solvent is atomized using a high electric potential to produce a spray of solvent-encapsulated solute droplets (Fig. 7). The droplets have a high surface area to volume ratio, allowing for rapid in-flight evaporation of the carrier solvent. Dry solute material can be deposited onto a target surface to create a thin continuous and conformal film [62, 63]. Electrospray

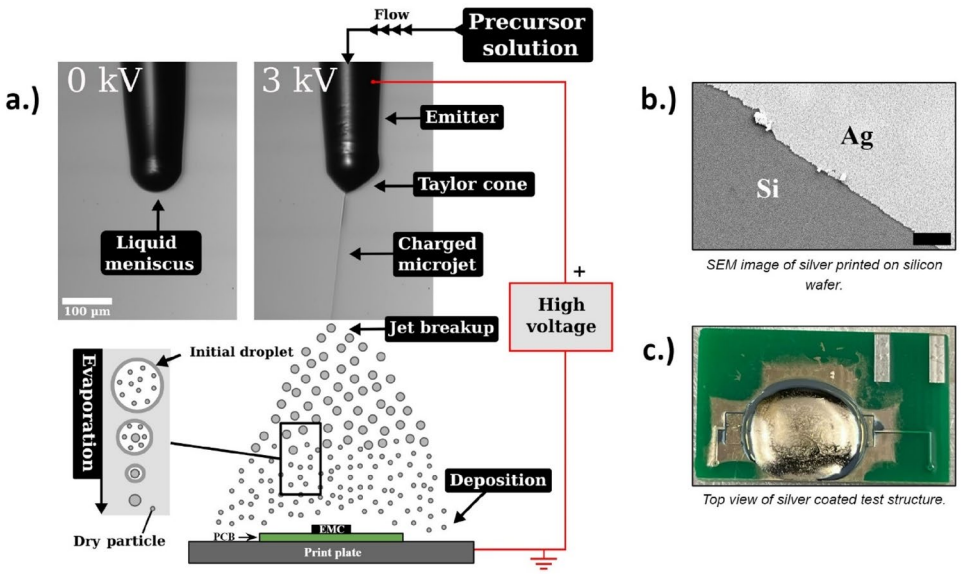

Fig. 7 **a** Electrospray printing onto a model test structure (epoxy molding compound on a printed circuit board). A precursor solution of 35 wt% silver in triethylene glycol monomethyl ether is pumped to a microfluidic emitter and subjected to a high electric potential. The solution atomizes into a spray of solvent-encapsulated solute droplets that evaporate in-flight. The solute material (silver) is deposited onto the target to create a film. **b** SEM image of an electrospray printed silver film on a silicon wafer. The scale bar is 5 µm. **c** Top view of model test structure coated with silver

printing is an electric-field driven process and substrates with 3D topographies (e.g., wires, sharp corners, undercuts) can be conformally coated, even in regions not in the direct line-of-sight of the emitter [64, 65]. The solute material will track the path of the electric field lines and deposit on areas where those lines terminate. The print material will preferentially deposit on conductive surfaces to form thicker films, while insulating surface will accumulate less material to produce thinner films. We have used electrospray to deploy polyimide for electronics manufacturing and packaging applications [66]. These films showed outstanding thermal, optical, and dielectric properties. When compared to competing thin-film manufacturing techniques, such as chemical vapor deposition or sputtering, electrospray provides improved coverage on complex topographies, lower material waste, and lower costs.

Recently, we have used electrospray printing to deploy silver with the goal of providing compartmental electromagnetic interference (EMI) protection for system-in-package (SiP) architectures. Contemporary board-level shielding requires ample space and is difficult to implement into constrained environments, inhibiting the potential for device miniaturization [67]. Thin conformal silver films built using electrospray printing are space efficient, materials conservative, and, since they are made additively, can be produced at high-throughput. Our work aims to establish a relationship between the print processing parameters, such as flow rate, emitter-to-target separation distance, print time, and the optimal film characteristics for shielding. The electrospray print parameters govern the film microstructure, and thus, its physical characteristics and performance [61, 68]. We are probing the relationship between the print processing parameters and the key film characteristics, including uniformity, electrical continuity, adhesion, and isolation performance.

Electrospray printing is a novel method for deploying thin-film materials for advanced packaging applications. With further development, it will provide enhanced capabilities for semiconductor manufacturing and improve the functionality of devices. Future work will focus on developing a better understanding of the process fundamentals and translating this knowledge to support industry use of this technology.

Summary

Over the last 40 + years, society has realized enormous gains in the computer and communication efficiency of semiconductor chips and packages, which have driven both global economic prosperity and the rise of our modern world. This was accomplished through planar (2D) device compaction that relied upon an endless stream of material-related insight, research, innovations, and commercialization and used the entire period table. Those 2D scaling breakthroughs were only achieved thanks to the close collaboration of experts in academia and industry.

Today, 40 years later, we face a new reality: (i) the traditional path to performance gains, namely the 2D scaling of semiconductor chips, has been stopped by fundamental physical limits, and (ii) there are new physical limits driven by sustainability. In recognition of these facts, SRC has brought forward the 2030 Decadal Plan for Semiconductors [69] which brings attention to expanding our advanced chip-making and chip-packaging efforts into three dimensions as one of the research priorities that can help us to meet the needs of future generations. For the next microelectronic system revolution, emerging materials and physics will be leveraged for new advanced packaging solutions that can have system-level benefits. As a result, the semiconductor industry is pivoting away from the 2D-electronics paradigm and shifting its thinking to new value propositions that involve 3D monolithic and heterogeneous integration technologies as the key driver. Herein, we have highlighted a small subset of the materials research that we see as promising for the future of semiconductor manufacturing. To assure future design, development, and manufacturing of heterogeneously integrated chips an industry-wide new roadmap—the NIST Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap has been developed [70], which is the first 3D semiconductor roadmap to guide the forthcoming microelectronic revolution, like the International Technology Roadmap for Semiconductors (ITRS) has served in the past.

The semiconductor industry must now excite and support the broader materials community so that these experts can help to solve many of the research and commercialization challenges of next generation compute and communication devices. This includes sustainable chip manufacturing and packaging at all length scales, device performance, and the movement of data in increasingly efficient ways, and management of the form factor and thermal performance of these amazing packaged devices. These are tough problems that cannot be solved without your ideas and energy.

One thing is certain, over the next 40 years, the semiconductor industry will require significant innovation. At the heart of that is the need for significant contributions from the materials ecosystem to drive materials from the laboratory to the factory.

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Declarations

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