



Inter-layer coatings for softening polymer-based neural interfaces

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Abstract

This paper reports the successful fabrication of softening polymer (SP)-based devices with inter-layer coatings for neural interface applications. SPs are flexible biocompatible polymers that soften upon implantation into the body, thus capable of reducing mechanical stress on the surrounding tissue and increasing the conformability of the implant. The softening process relies on water uptake into the polymer that can affect its electrical insulation capabilities. Employing an amorphous silicon carbide (a-SiC) thin film inter-layer between the metal traces and the SP is expected to provide a reliable water-barrier while allowing the SP plasticization once the device is implanted. We report the electrochemical properties and leakage current characteristics of various structures with a-SiC and polyimide inter-layer coatings under simulated physiological conditions. The fabricated structures demonstrated appropriate electrical properties and were found to be reliable up to a 2.5 mm radius of curvature when bending in compression.

Introduction

Current polymeric material-based neural interfaces are being investigated for chronic use as they reduce the mechanical mismatch between the nervous tissue and the device compared to Si-based devices. They provide good biocompatibility, insulation, flexibility, fabrication-processing, and long-term reliability [1]. Polymeric substrates, such as Parylene-C, polyimide, and silicones are replacing Si substrates as they conform better over the target tissue and reduce damage, as they are softer than Si and oxide/nitride encapsulation used in neural devices [2–5]. Considering the same size of devices, the softer the implant, the less inflammatory response is observed in surrounding tissue [6]. However, to minimize trauma during insertion into the cerebral cortex, it is preferred to use thin-stiff materials ($E > 2\text{GPa}$) [6–8]. Softening polymers (SPs) are responsive materials whose elastic modulus (E') can be accurately controlled when certain

stimuli, such as temperature and humidity are applied. Their elastic modulus (E') can be reduced from $\sim 2\text{GPa}$ at 27°C to $\sim 10\text{MPa}$ when soaked at 37°C in phosphate-buffered saline (PBS) [9]. This modulus reduction enables the devices to conform to neural tissue while promoting positional stability. In addition, the fabrication, handling, and positioning of the devices occur when the polymer is in its glassy state, making it easier to manipulate. Once implanted the polymer softens, reducing the foreign body response and implant migration [10–14]. However, as the degree of polymer softening increases, the insulation properties have been shown to decrease [9]. Therefore, the use of insulation layers to reduce deleterious leakage currents between the metal traces within the softening polymer is being investigated as an approach to enable higher degrees of softening for neural applications while minimizing leakage. The most used insulation layers are thin films of SiO_2 and Si_3N_4 . Both PECVD deposited thin films have been shown to have the average in vivo dissolution rates of 3.5 and 2.0 nm/day, respectively [15]. Amorphous silicon carbide (a-SiC) is an alternate thin film insulator that has become increasingly important for neural interface applications as it can improve device longevity [16]. A-SiC has a dissolution rate of 0.1 nm/day at 90°C in PBS (pH = 7.4) and a non-measurable dissolution rate at 37°C in PBS, suggesting it is a suitable encapsulation material for integrated neural interfaces [17–19]. However, a-SiC application in neural interfaces may be limited

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as it might require a carrier substrate to handle and position devices at their target tissue [20, 21]. A multilayer (a-SiC/SP) may overcome these limitations by enabling straightforward implantation of long-lasting a-SiC thin film-based devices while minimizing neural tissue damage [22].

Materials and methods

Four types of devices were fabricated for this study using the methods described in the Supplemental Information (SI): Type 1 is an SP device with Au traces but no additional insulation layers; Type 2 includes patterned polyimide and a-SiC layers having one layer of SP as the main carrier; Type 3 includes the SP, polyimide and a-SiC full layers; and

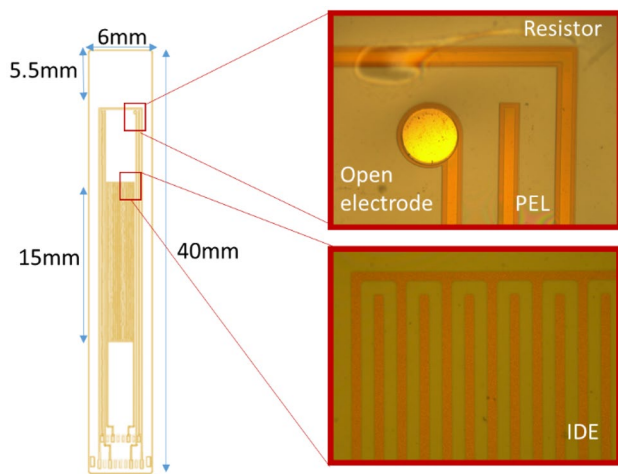
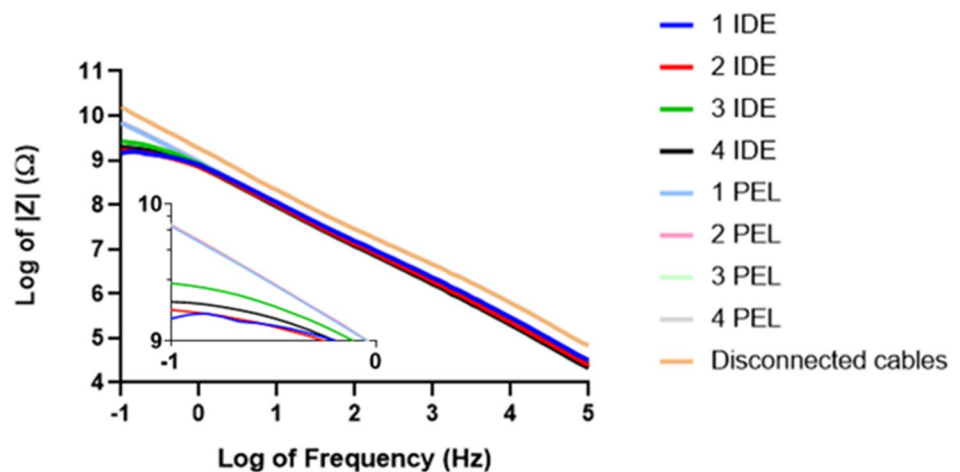


Fig. 1 Device layout design for electrical and mechanical testing. The device includes an IDE, PEL, resistor, and two open electrodes. The insets show optical microscope images of fabricated structures. The trace width and trace separation in the IDE layout were both 50 μm . The trace width of PEL was also 50 μm , but the two traces were positioned 3.45 mm apart along the two sides of the IDE

Fig. 2 Mean impedance amplitude as a function of frequency of IDE and PEL structures ($n = 5$) of four types of samples. The inset shows an expansion of the 0.1 to 1 Hz frequency range revealing lower impedance for IDEs than for PELs at low frequencies



finally, Type 4 has the first polyimide and both a-SiC layers patterned, but has a full layer of polyimide and SP.

The design used for all devices included a pair of interdigitated electrodes (IDE), parallel encapsulated lines (PEL), open electrodes, and a continuous line that serves as a test resistor, as shown in Fig. 1. All device structures were packaged with zero-insertion force connectors (SI).

Electrochemical Impedance Spectroscopy (EIS) and direct current (DC) leakage current measurements were performed between the pairs of fully insulated IDE and PEL traces while the samples were immersed in PBS at 37 $^{\circ}\text{C}$. Bending tests were performed in PBS at room temperature and involved bending the devices at various radii and measuring changes in electrical resistance of the resistor element on the array. Both electrical and mechanical characterizations were used to confirm the functionality and establish the basic properties of the device structures. The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Results and discussion

Impedance spectroscopy

EIS results showed consistent impedance spectra in PBS at 37 $^{\circ}\text{C}$ (Fig. 2). Both IDE and PEL measurements resulted in the same impedance curve at frequencies above 1 Hz, despite the different length and spacing of conducting traces. To validate these results, the samples were disconnected and EIS of the disconnected cables inside a Faraday Cage in an oven at 37 $^{\circ}\text{C}$ was measured to assess any contribution from cabling and establish the capability of our setup. Data from the samples were found to be close to the measurement limit, as seen in Fig. 2, and the mean impedance values at 1 kHz showed no significant difference between

PELs and IDEs ($P=0.52$) based on a two-sample t test ($1.97 \text{ G}\Omega \pm 208.04 \text{ M}\Omega$ and $2.06 \text{ G}\Omega \pm 55.89 \text{ M}\Omega$, respectively), confirming that the input impedance of the measurement setup dominates at this frequency. However, below 1 Hz frequency, the IDE samples are measurable, as seen by the impedance becoming resistive (frequency-independent), while the impedance of PELs remains capacitive, having a significant difference ($P < 0.001$). This is expected because IDE structures are apt to higher intrinsic leakages than PELs due to the smaller separation between their traces and the larger length of their traces. IDEs are also more likely to have defect sites in their insulation layers than PELs simply due to the larger area they occupy. While the setup is limited in measuring the impedance of the intact IDE and PEL structures, it is capable of monitoring sample deterioration during simulated aging experiments by detecting impedance drops due to increased current leakages.

DC leakage currents

DC leakage currents were assessed by chronoamperometry (S4.1) and were found to be mostly below 1 nA, which for this work we consider the insulation failure limit. PELs showed a mean leakage current value of $222 (\pm 81.9) \text{ pA}$ that was significantly lower ($P=0.002$) than that of the IDEs at $732 (\pm 150) \text{ pA}$ (Fig. 3). Type 1 device IDEs that did not have any additional inter-layer insulation exhibited the highest leakage currents on average.

Bending tests

The mean resistance change (ΔR) compared to their initial value (R_0) of the resistor lines of each device structure remained noticeably constant at the measured bending

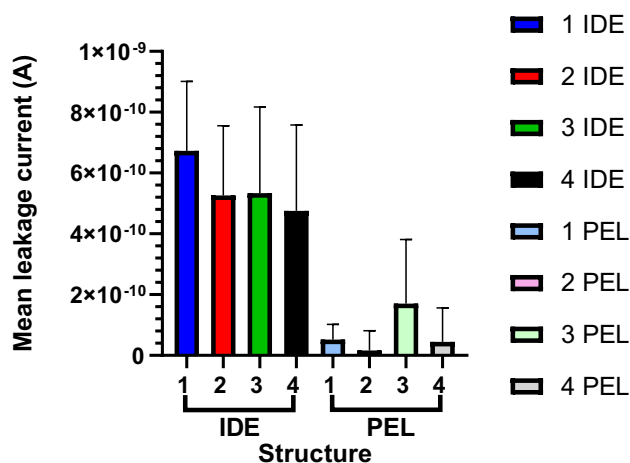


Fig. 3 Mean and SEM DC leakage current measured against time for the softening polymer structures when applying a 5 V step for 150 s ($n=5$) in PBS at 37°C

curvatures (mean $\Delta R/R_0 = 1.001777 \pm 0.0128$), indicating that the metal traces remained intact during this flexural challenge. We observed an increase in resistance change on one of the 3 measured samples of type 4 structure at a curvature of 0.33 mm^{-1} and we speculate that the metal trace for that specific device was being affected (Fig. 4). The same device showed an increased ΔR for the 0.4 mm^{-1} curvature which implicates the metal trace damage was permanent (mean $\Delta R/R_0 = 0.999581 \pm 0.000746$ of all types excluding affecter type 4 sample). However, the other two type-4 tested devices remained unaffected by the bending curvature. The results demonstrate that the fabricated structures are capable to bend to a 2.5 mm radius of curvature in PBS at room temperature and deliver electrical measurements without suffering from metal traces failure.

Conclusions

Whereas SP materials are attractive substrates for implantable microelectrodes, their inherent electrical properties mandate the use of an additional inter-layer encapsulation material around embedded metal traces. Here, we demonstrate the successful microfabrication of SP-based structures with a-SiC and polyimide encapsulation layers. Various strategies of encapsulation patterning were tested, and all fabricated structures were found to provide appropriate electrical insulation of the embedded metal traces when immersed in saline solution. Moreover, all samples were capable of bending without breakage around a 2.5 mm radius, which is expected to be sufficient for neural interface applications such as electrocorticogram arrays and cuffs for large nerves. Although no significant differences were observed between the types of structures investigated, it is expected that the lifetime of these devices will vary in simulated physiological conditions. We intend to further study these devices to determine

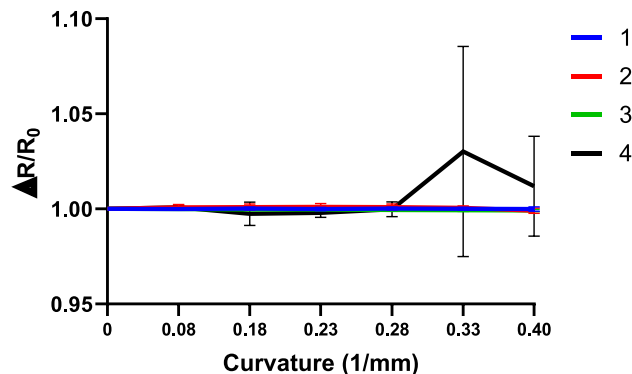


Fig. 4 Mean resistance change vs bending curvature of resistor lines of the four types of softening structures ($n=3$)

their stability in accelerated aging experiments and thereby identify optimum structures for chronic implantations.

Supplementary Information The online version contains supplementary material available at <https://doi.org/10.1557/s43580-021-00159-1>.

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Declarations

Conflict of interest The authors have no conflict of interest to declare.

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