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Thin Film Characterization on Cu/SnAg Solder Interface for 3D Packaging Technologies

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ABSTRACT

Copper is a commonly used interconnect metal in microelectronic interconnects due to its exceptional electrical and thermal properties. Particularly in applications of the 2.5 and 3D integration, Cu is utilized in through-silicon-vias (TSVs) and flip chip interconnects between microelectronic chips for providing miniaturization, lower power and higher performance than current 2D packaging approaches. SnAg capped Cu pillars are a common high-density interconnect technology for flip chip bonding. For these interconnects, specific properties of the Cu surface, such as roughness and cleanliness, are an important factor in the process to ensure quality solder bumps. During electroplating, tight processing parameters must be met so that defects are avoided, and high bump uniformity is achieved. An understanding of the interactions at the solder and Cu pillar interface is needed, based on the electroplating parameters, to determine the best method for populating solder on the wafer surface. In this study, surface treatment techniques such as oxygen plasma cleaning were performed on the Cu surfaces and the SnAg plating chemistry for depositing the solder were evaluated through hull cell testing to qualitatively determine the range of current densities to investigate. It was observed that current density while plating played a large role in solder bump deposition morphology. At the higher current densities greater than 60 mA/cm^2, bump height non-uniformity and dendritic growth are observed and at lower current densities, less than or equal to 60 mA/cm^2, uniform, continuous bump height occurred.

INTRODUCTION

Mutli-chip stacking and heterogeneous integration (HI) has the ability to improve performance and reduce size, weight, and power (SWaP) for microelectronics packaging architectures as compared to more traditional 2-D packaging approaches. In these 2.5 and 3-dimentional (3D) integration schemes, copper metallization is utilized for through-silicon-vias (TSVs) and flip chip bonding [1]. Flip chip bonding techniques such as IBM's Controlled collapse chip connection (C4) are used in the microelectronics packaging industry to connect chips by means of electrically conductive solder bumps between the two chip surfaces allowing miniaturization and better performance [2]. C4 approaches have limits in interconnect density because as the pitch between interconnects scales to lower than ~100 µm, the bond line thickness between the two chips similarly scales to a point at which it is prohibitively difficult to completely fill the bond line gap with underfill epoxy. To enable increase in interconnect density (decrease in interconnect pitch) an alternative approach has been developed known as chip connection (C2) in which Cu pillars are capped with SnAg solder [3]. The Cu pillar height defines the bond line thickness and the SnAg solder bump enable reflowed solder connection between the two chips. SnAg solder bumps are deposited on copper pillars by electroplating for improved control of bump pitch, higher processing throughput and process control [4]. Surface properties of Cu interconnects play an important role to ensure quality solder bumps. Consequently, a clear understanding of the interactions at the SnAg and Cu interface is required to optimize bump uniformity which is controlled by the electroplating parameters.

Electroplating is a method for depositing a thin layer of uniform metal cations onto an electrode using electrical current. An advantage of electroplating solder contacts for C4 and C2 packaging is the precise control of thickness and uniform morphology in the growth of the solder bumps, by closely adjusting the electroplating parameters [5]. Additionally, electroplating solder bumps can greatly reduce the amount of time required in industrial high-volume applications to populate a fully patterned wafer as compared to solder jetting which is a commonly used technique in microelectronics packaging processes. Solder jetting requires machinery that uses a laser to melt micro-sized solder balls onto aligned wafer contacts. The speed of the instrument is slow, with an approximate deposition rate of 3 solder balls per second, and a limited solder ball size restricts the advancements of this technique towards 3D packaging.

A schematic of a standard C4 solder bump integration used in microelectronics manufacturing is shown in Figure 1. The solder is deposited on top of the under-bump metallurgy (UBM) which serves to promote adhesion between the solder and the bond pad as well as prevent diffusion of the solder into the underlying interconnects. Reduction in bump pitch increases interconnect density per area for a die and enables improved power and ground handling in integrated circuits [6]. While Cu to Cu interconnects allow for higher power output, they require much smaller pitches and higher temperature processing during thermal compression bonding [7]. Using SnAg solder allows for relatively lower melting temperature during the flip chip bond for advantages in managing thermal budgets.

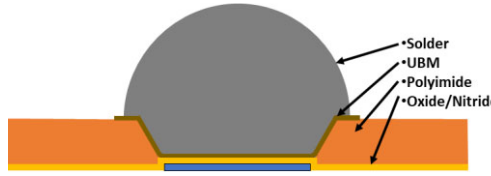

Figure 1: Standard C4 solder bump integration.

EXPERIMENT

Materials

6-inch silicon wafers with patterned Cu seed contacts were obtained from Sandia National Labs. DOW Solderon BP TS 6000 Tin/Silver Bump Plating Bath was used for the SnAg alloy plating bath consisting of a composition containing 97-3 atomic percent Sn-Ag. Sn was chosen as an alternative to Pb solder to reduce environmental impacts of lead, and silver was used in the Sn-alloy because tin needs minor alloying to prevent tin whisker formation and provide better mechanical properties [8].

Methods

A blanket film of 1000/3000/1000 angstrom Ti/Cu/Ti film was deposited by electron beam evaporation onto a top passivation layer which passivation cuts to access the bond pads. The first Ti film is used as an adhesion layer to promote adhesion of the Cu to the Al bond pad. The Cu layer is the plating seed metal and the top Ti layer is a protective film to prevent oxidation of the Cu. The top protective Ti layer is removed immediately prior to plating. Wafers were then put into an integrated photoresist spin coat and exposure track for patterning of the 90-micron diameter contacts, with a photoresist height of 50-microns. After lithography, wafer surfaces were treated by a 30 second oxygen plasma dry etch to remove any surface contamination from the photoresist. Figure 2 shows the processing steps to create a wafer ready for flip chip bonding, starting from the patterned wafer to the final reflow process.

1. Etch the top Ti layer using a hydrofluoric acid dip to expose the Cu seed metal.
2. Activate the Cu surface with 5% sulfuric acid to remove any potential Cu oxide formed by the first rinsing with DI water.
3. Electroplate SnAg onto the Cu contacts by dipping the testing wafer into the SnAg alloy electrolyte bath. A Biologic potentiostat was used as the power source during electroplating.
4. Remove photoresist with an acetone rinse.
5. Etch remaining seed metal to expose top passivation using 30% ammonium hydroxide + sodium chlorite etchant solution.
6. Reflow solder bumps to eutectic point in industrial reflow oven to partially melt into solder spheres for flip chip bonding.

During the plating process, a pogo pin contact was used for electrical stability. This type of contact ensures stable current flow and direct contact with the seed Cu on the patterned wafer during deposition. Scanning electron microscopy (SEM) was used for visual inspection of electroplated solder bumps after deposition. Optical profilometry was performed using a confocal microscope to qualitatively confirm bump height and morphology.

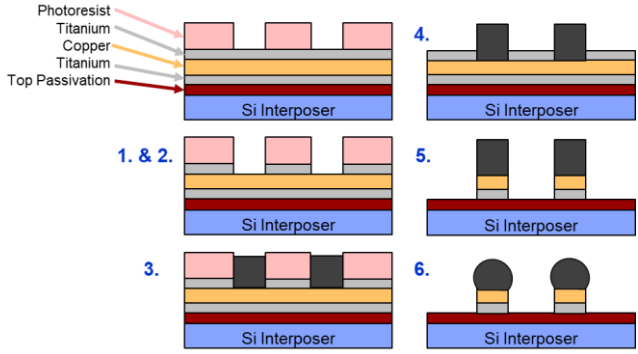

Figure 2: Electroplating processing steps to prepare wafers for flip chip bonding. The first steps involve etching the top Ti layer to expose Cu contacts and removing Cu surface oxides (1&2). Next, SnAg solder is plated (3) and the photoresist is removed (4). Remaining seed metal is etched (5) and the solder bumps are reflowed (6) before they are ready for flip chip bonding.

Hull cell test

A hull cell test allows for evaluating the optimum range of current density for uniform deposition. Prior to electroplating, a 267 ml hull cell test experiment was performed using a copper plate as the cathode in the SnAg plating bath to qualitatively determine the condition of the electrolyte solution. The temperature was controlled using a standard hot plate with magnetic stir bar agitation. A constant bias is applied using a Biologic potentiostat power supply with a total current of 2 amps, for a duration of 30 seconds. The angled design of the hull cell allows for a varying range of current densities to deposit as a function of linear position along the cathode. A current density below 60 mA/cm^2 was found to be optimal for uniform plating, whereas a plating density of 80-100 mA/cm^2 shows a rougher, discontinuous film surface, Figure 3.

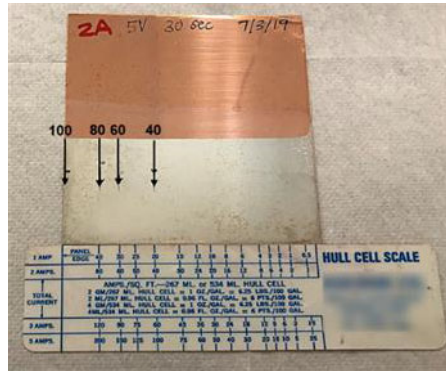

Figure 3: Cu plate used in hull cell experiment shows a current density below 60 mA/cm^2 is optimal for uniform plating.

RESULTS

A current density range of 60-100 mA/cm^2 was recommended according to the technical data sheet for the DOW Solderon BP TS 6000 Tin/Silver Bump Plating Bath for uniform plating height. Each 6-inch patterned wafer was cleaved into smaller testing pieces for better control of plating parameters. Current densities of 30, 60, 80, 100, and 200 mA/cm^2 were used to determine the variation in plating quality. It was determined that at higher current densities, greater than 60 mA/cm^2, solder bump growth was nonuniform and difficult to control. At current densities of 60 and 30 mA/cm^2, uniform bump height was achieved.

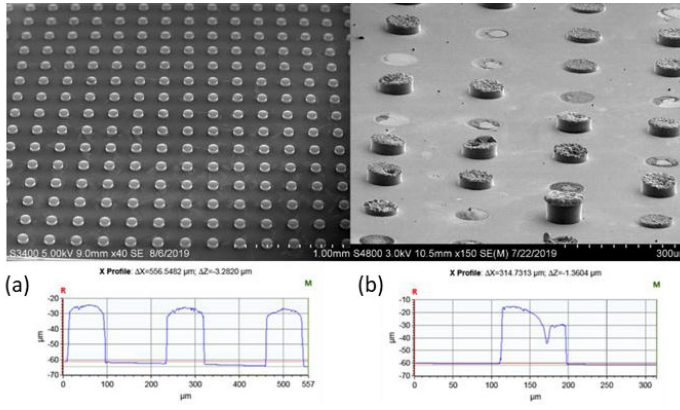

Figure 4: SEM images of the solder bumps with (a) uniform plating using a current density of 30 mA/cm^2 (40X magnification) and (b) nonuniform plating using a current density of 100 mA/cm^2 (150X magnification) with representative cross sections obtained by optical profilometry.

At low current (30 and 60 mA/cm^2), uniform plating was observed but as the current densities became too high (greater than 60 mA/cm^2), surface morphology was uncontrollable. Figure 4 shows the comparison of low and high current densities and their effects on uniform solder bump development. It can be seen in Figure 4.a that when a low current density of 30 mA/cm^2 is used, a uniform plating was achieved, yet when a current density of 100 mA/cm^2 is used, non-uniform solder bumps are observed as in Figure 4.b. Optical profilometry cross sections of the nonuniform bumps in Figure 4b illustrate cavity like hole in the center of the bump in addition to over plating bumps, called mushrooms, as well as the under plated bumps where the center of the bump has bare Cu and no bump formation.

DISSCUSION

Plating was performed to investigate solder surface morphology, deposition rates, repeatability, and bump uniformity. Uniform solder bump formation occurred at lower current density ranges of 60 and 30 mA/cm^2. This threshold condition was determined qualitatively using a hull cell test to determine the deposited SnAg film quality on a blank Cu plate. At current densities of 80, 100 and 200 mA/cm^2 nonuniform, discontinuous and dendritic bump formation occurred. Figure 5 shows dendritic solder bump formation that was observed at a current density of 100 mA/cm^2 implemented during the electroplating process. These dendrites formed inconsistently across the Cu contacts amidst other nonuniform plated morphologies mentioned before such as, mushrooms and underplating.

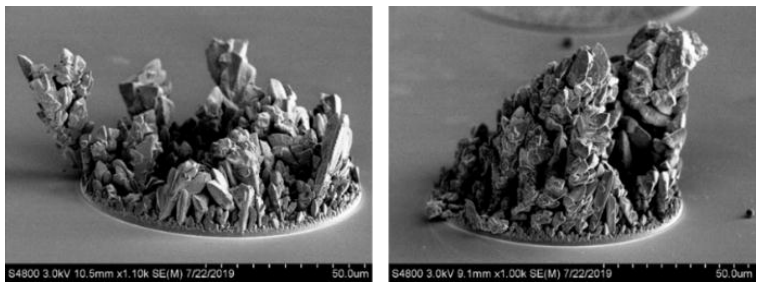

Figure 5: SnAg solder dendrite formation observed at a current density of 100 mA/cm2.

Kim 2003 [9] observed similar results while plating near-eutectic SnAg solders for wafer level packaging. Kim's study found a drastic change in morphology at increasing current density. The phenomenon was proven to be the result of the limited mass transfer of silver ions at low potentials. Further analysis of the Cu/SnAg bump interface is needed to understand the mechanisms for these dendritic formations. Micro and nano-scale Cu surface examinations could indicate the importance of Cu surface nature on Cu/SnAg interface quality. Further evaluations based on Cu surface topography and electrochemical analyses indicating the passivation behaviour of Cu surface should be performed to evaluate the rate of surface passivation on the interface and film growth quality [10].

CONCLUSIONS

Current densities ranging from 30-60 mA/cm^2 were favored for uniform solder deposition, bump height and optimal plating parameters. A hull cell test was performed prior to SnAg solder deposition to quickly identify a range of suitable conditions of the plating bath and to improve current density plating parameters. SnAg solder bumps were electroplated onto Cu pads at current densities ranging from 30-200 mA/cm^2. At higher current densities, greater than 60 mA/cm^2, bump height non-uniformity and dendritic growth were observed. Continued research is planned to investigate influence from the Cu surface to fully understand the role higher current densities play on the uneven surface quality of some solder bump formations and the effects on the Cu/SnAg interface.

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