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Characterization of Graphene Gate Electrodes for Metal-Oxide-Semiconductor Devices

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ABSTRACT

We fabricate and characterize metal-oxide-semiconductor (MOS) devices with graphene as the gate electrode, 5 or 10 nm thick silicon dioxide as the insulator, and silicon as the semiconductor substrate. We find that Fowler-Nordheim tunneling dominates the gate current for the 10 nm oxide device. We also study the temperature dependence of the tunneling current in these devices in the range 77 to 300 K and extract the effective tunneling barrier height as a function of temperature for the 10 nm oxide device. Furthermore, by performing high frequency capacitance-voltage measurements, we observe a local capacitance minimum under accumulation, particularly for the 5 nm oxide device. By fitting the data using numerical simulations based on the modified density of states of graphene in the presence of charged impurities, we show that this local minimum results from the quantum capacitance of graphene. These results provide important insights for the heterogeneous integration of graphene into conventional silicon technology.

INTRODUCTION

Graphene has attracted significant research interest for many applications in electronics, due to its excellent electrical conductivity, high optical transparency, mechanical flexibility, high thermal stability, and two-dimensional structure. However, the potential of graphene as a channel material replacing silicon is limited due to the absence of a bandgap. On the other hand, graphene is an excellent candidate as a transparent, conductive, and flexible electrode for silicon-based electronic and optoelectronic devices, including solar cells, gas sensors, and photodetectors.

Unlike conventional metals, whose Fermi level is typically pinned at the surface, the Fermi level and hence workfunction of graphene can be tailored by electrostatic gating, chemical or contact doping, surface engineering, or by varying the number of graphene layers. As a result, graphene is also a promising candidate as a replacement for the gate electrode in metal-oxide-semiconductor (MOS) devices. In recent work, graphene has been used as the gate electrode of a nonvolatile charge-trap Flash memory device to replace TaN metal on top of a high-κ dielectric [1]. In another recent work, multi-layer graphene was incorporated between TiN metal gate and SiO_2 in a MOS capacitor structure [2]. It was demonstrated that graphene electrodes improve the device performance in both cases. However, a detailed study of the electrical properties of graphene/SiO_2/Si MOS structures is currently lacking. In particular, a study of the gate tunneling

current and of the effect of the graphene quantum capacitance on the MOS capacitance-voltage characteristics has not been performed. Such an investigation of MOS devices with graphene gate electrodes would be of great importance for assessing the potential of integrating graphene into mainstream silicon technology.

In this work, we have fabricated and studied the temperature dependent *I-V* characteristics and room temperature *C-V* characteristics of MOS devices with graphene as the metal electrode, silicon dioxide with thicknesses of 5 or 10 nm as the dielectric, and *p*-type silicon as the semiconductor. Our results provide fundamental information on the electronic properties of MOS devices with graphene gate electrodes, which is important for the heterogeneous integration of graphene into silicon technology.

EXPERIMENTAL DETAILS

MOS devices were fabricated with oxide thicknesses of 5 or 10 nm. The starting substrates were ~3×10^{16} cm^{-3} doped *p*-type Si with 300 nm thermally grown oxide on top. First, active area windows were opened in the oxide layer by photolithography and buffered oxide etch (BOE). Subsequently, a gate oxide layer with a thickness of 5 or 10 nm was thermally grown on the active areas. Graphene was grown on a copper foil in a low pressure chemical vapor deposition system at a temperature of 1000ºC [3,4]. After graphene growth, poly(methyl methacrylate) (PMMA) was deposited on top of graphene, followed by the etching of copper foil in $FeCl_3$. The graphene layer was then transferred onto the Si substrates and the PMMA layer was removed. After the transfer step, graphene was patterned by O_2 plasma etching. The portion of the graphene layer that is etched lies well outside of the active device area, and hence the etching step should not create any oxygen traps in the MOS gate oxide layer. Finally, Ti/Au (5 nm/50 nm) metallic contact rings were patterned on graphene lying on the field oxide for electrical probing. Figure 1 shows the schematic of the graphene/SiO_2/Si MOS device.

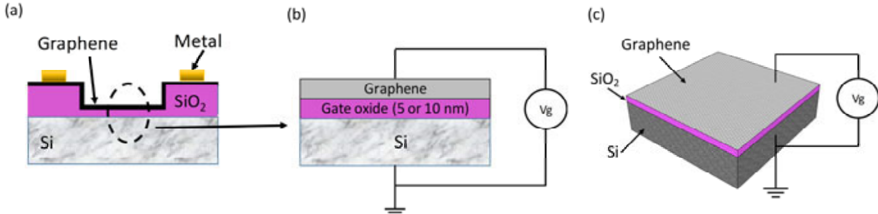

Figure 1. The graphene/SiO_2/*p*-type Si MOS device showing the (a) cross-sectional schematic, (b) zoom-in of the active device region indicating the applied gate voltage V_g, and (c) 3D schematic of the active device region.

RESULTS AND DISCUSSION

Figures 2(a) and (b) show the *I-V* characteristics of the graphene/SiO_2/Si MOS devices with 5 and 10 nm oxide, respectively, at eight different temperatures ranging from 77 K to 300 K, all under negative gate bias. Gate leakage currents of MOS devices are typically governed by Fowler-Nordheim (F-N) tunneling, which describes the tunneling of electrons through a triangular potential barrier, resulting in a current I_{FN} given by [5,6]

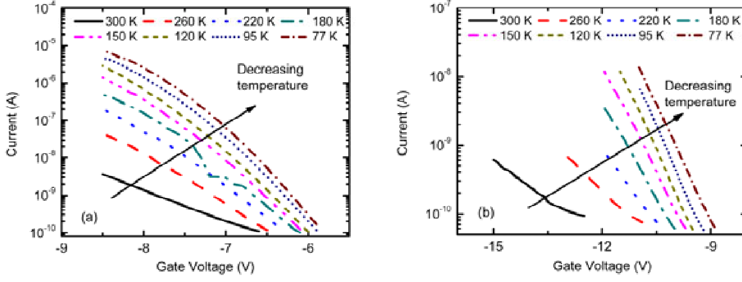

Figure 2. *I-V* characteristics at different temperatures for the graphene/SiO_2/Si MOS device with (a) 5 nm oxide and 200 µm x 200 µm area and (b) 10 nm oxide and 100 µm x 100 µm area.

$$I_{FN} = A_G A E_{ox}^2 \exp\left(-B / E_{ox}\right), \tag{1}$$

where A_G is the device area, E_{ox} is the electric field in the oxide, and A and B are the pre-exponential and exponential F-N coefficients, respectively, defined as [6] $A = q^3 (m / m_{ox}) / 8\pi h \Phi_b$ and $B = 8\pi \sqrt{2 m_{ox} \Phi_b^3} / 3qh$, where q is the electron charge, m is the free electron mass, m_{ox} is the effective electron mass in the oxide, h is the Planck constant, and Φ_b is the effective barrier height. The plot of $\ln(J_{FN} / E_{ox}^2)$ vs. $1/E_{ox}$, where $J_{FN} = I_{FN} / A_G$ is the current density, is known as the F-N plot and yields a straight line. The coefficients A and B can be extracted from the y-intercept and slope of the F-N plot, respectively.

In our case, since the applied gate voltage is negative, the F-N current is due to the tunneling of electrons from the graphene gate electrode into the oxide. F-N tunneling of holes from the valence band of silicon into the valence band of oxide could be neglected due to a hole barrier height which is significantly higher. Furthermore, since the Fowler-Nordheim tunneling current decreases exponentially with increasing oxide thickness, the contribution to the tunneling current from the metal/graphene/SiO_2/Si structure lying on the field oxide is negligible.

Figures 3(a) and (b) show the F–N plots of 5 and 10 nm oxide devices, respectively, at eight different temperatures. It can be seen from Fig. 3(b) that, for the 10 nm device, the F-N plots are linear at all temperatures, whereas their slopes decrease as temperature increases from 77 K to 300 K. The 5 nm device, on the other hand, begins to deviate from straight line fits at high temperatures and low electric fields, indicating that direct tunneling also starts to play a role. Any deviation at low electric fields due to direct tunneling does not affect the F-N data analysis, which is based only on the linear portion of the plots.

The good linearity of the F-N plots for the 10 nm device indicates that Eq. (1) can still be used to empirically describe the F-N current at all temperatures with temperature dependent effective F-N coefficients $A(T)$ and $B(T)$ [7,8]. The values of the effective barrier height Φ_b^{eff} as a function of temperature can be calculated from the extracted values of B. The temperature dependence of B and Φ_b^{eff} are shown in Figs. 4(a) and (b), respectively. We have extracted $\Phi_b^{eff}(T)$ from $B(T)$ as commonly done, since this is more reliable compared to extraction from

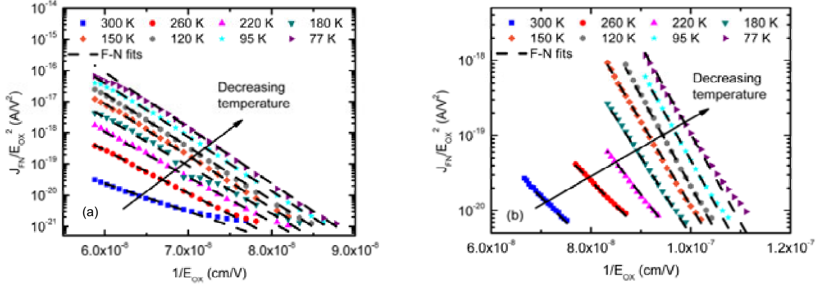

Figure 3. F-N plots at different temperatures ranging from 77 K to 300 K for the graphene/SiO_2/Si MOS device with (a) 5 nm oxide and 200 µm x 200 µm area and (b) 10 nm oxide and 100 µm x 100 µm area, calculated from the data shown in Figs. 2(a) and (b), respectively. The linear F-N fits are shown by the dashed lines.

$A(T)$, as discussed in the literature [7,8]. Here, we assumed a temperature independent effective mass of $m_{ox} = 0.5m$ [7-9]. It can be seen from the figure that Φ_b^{eff} decreases from ~3.25 eV to 2.25 eV as temperature increases from 77 to 300 K. There are two factors which could contribute to the decrease of Φ_b^{eff} with increasing temperature. The first one is the direct effect of temperature through the Fermi-Dirac distribution function. The second factor, which is indirect, is that the actual graphene/SiO_2 barrier height itself could be temperature dependent. This decrease of Φ_b^{eff} with increasing temperature agrees with the trend observed in previous experiments on the temperature dependence of the F-N current in conventional MOS devices with polysilicon or metal gate electrodes [7,8].

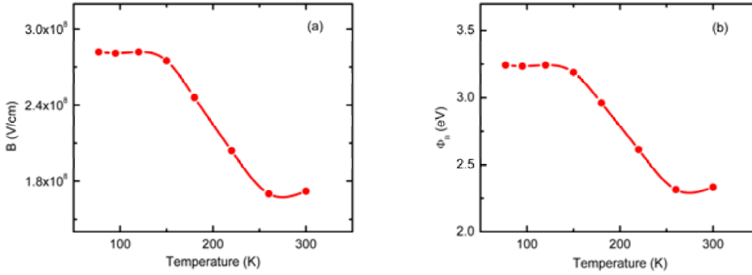

Figure 4. (a) B and (b) the effective barrier height as a function of temperature for the device with 10 nm oxide and 100 µm x 100 µm area, extracted from the F-N fits shown in Fig. 3(b).

High-frequency C-V measurements were also performed on the graphene/SiO_2/Si MOS devices with 5 and 10 nm oxide at a frequency of 100 kHz, as shown in Fig. 5(a). A capacitance dip under accumulation is observed, particularly for the 5 nm oxide device. This capacitance dip is due to the contribution of the quantum capacitance of graphene [10-17]. The quantum capacitance of graphene in the presence of charged impurities is given by [16-18]

$$C_Q(V_{ch}) = \frac{\partial Q}{\partial V_{ch}} = q^2 \int_{-\infty}^{\infty} D_{gr}^*(E)\left(-\frac{\partial f(E,E_F)}{\partial E}\right)dE\,, \quad (2)$$

where Q is the net charge per area in the graphene sheet, V_{ch} is the graphene electrostatic potential given by $V_{ch} = -E_F / q$, where E_F is the graphene Fermi level, $D_{gr}^*(E)$ is the modified density of states (DOS) of graphene per unit area in the presence of charge impurities given by $D_{gr}^*(E) = \frac{2}{\pi\hbar^2\upsilon_F^2}\left[E\mathrm{erf}\left(\frac{E}{\sqrt{2}s}\right) + \sqrt{\frac{2}{\pi}}s\exp\left(-\frac{E^2}{2s^2}\right)\right]$, where $\hbar$ is the reduced Planck constant, υ_F is the Fermi velocity in graphene, erf is the error function, and s is an energy parameter indicating the strength of the potential energy fluctuations, and $f(E,E_F)$ is the Fermi-Dirac distribution function. The reference of energy and potential is taken as the Dirac point.

In the experiments, the measured quantity is the total gate capacitance C_g as a function of gate voltage V_g. C_g is given by $C_g^{-1} = C_{ox}^{-1} + C_Q^{-1}$, which is the series combination of C_Q and the oxide capacitance per area C_{ox}, defined as $C_{ox} = \varepsilon_{ox} / t_{ox}$, where ε_{ox} is the permittivity of oxide and t_{ox} is the oxide thickness. As a result, the contribution from the quantum capacitance of graphene is observable only for thin oxides, where C_{ox} is large. Furthermore, V_g is related to V_{ch} by

$$V_g - V_{Dirac} = \left[V_{ch} + (1/C_{ox})\int_0^{V_{ch}} C_Q(V_{ch}^{'})dV_{ch}^{'}\right] \times \left|1 + i\omega C_g R_s\right|, \quad (3)$$

where V_{Dirac} is the gate voltage at the Dirac point, i is the imaginary unit, ω is the angular frequency of the small-signal gate voltage, and R_s is the series resistance arising from the sum of the contact resistances and the resistances of the metal ring, the graphene sheet, and the silicon bulk.

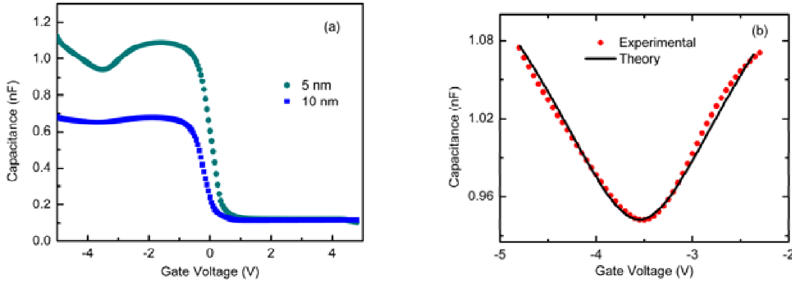

Figure 5. (a) High frequency (100 kHz) *C-V* characteristics at room temperature of graphene/SiO_2/Si MOS devices with oxide thicknesses of 5 and 10 nm. (b) The zoom-in of the experimental capacitance dip observed under accumulation for the 5 nm oxide device, as well as the theoretical best-fit calculated numerically based on the quantum capacitance of graphene in the presence of potential fluctuations induced by charged impurities.

Figure 5(b) shows the zoom-in of the experimental capacitance dip observed for the 5 nm oxide device, as well as the theoretical best-fit calculated numerically using Eqs. (2) and (3) with s = 38 meV and R_s = 10.5 kΩ used as the fitting parameters. The value of s obtained is in agreement with the values extracted from other experiments [14,17,19].

CONCLUSIONS

In conclusion, we fabricated and characterized MOS devices with graphene gate electrodes and oxide thicknesses of 5 or 10 nm. We demonstrated that Fowler-Nordheim tunneling dominates the gate current for the 10 nm oxide device and extracted the effective barrier height as a function of temperature. Furthermore, by performing *C-V* characterization, we observed a local minimum under accumulation, particularly for the 5 nm oxide device, which is due to the contribution of the quantum capacitance of graphene. We have fit this *C-V* data using numerical simulations. Our results provide important insights into the potential of graphene as a gate electrode in future MOS technology.

REFERENCES

[1] J. K. Park, S. M. Song, J. H. Mun, and B. J. Cho, Nano Lett. **11**, 5383 (2011).
[2] A. Misra, M. Waikar, A. Gour, H. Kalita, M. Khare, M. Aslam, and A. Kottantharayil, Appl. Phys. Lett. **100**, 233506 (2012).
[3] Y. An, A. Behnam, E. Pop, and A. Ural, Appl. Phys. Lett. **102**, 013110 (2013).
[4] Y. An, A. Behnam, E. Pop, G. Bosman, and A. Ural, J. Appl. Phys. **118**, 114307 (2015).
[5] S. M. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, 1981).
[6] D. K. Schroder, *Semiconductor Material and Device Characterization* (Wiley-Interscience, 1998).
[7] G. Salace, A. Hadjadj, C. Petit, and M. Jourdain, J. Appl. Phys. **85**, 7768 (1999).
[8] G. Pananakakis, G. Ghibaudo, R. Kies, and C. Papadas, J. Appl. Phys. **78**, 2635 (1995).
[9] Z. A. Weinberg, J. Appl. Phys. **53**, 5052 (1982).
[10] T. Fang, A. Konar, H. Xing, and D. Jena, Appl. Phys. Lett. **91**, 092109 (2007).
[11] D. L. John, L. C. Castro, and D. L. Pulfrey, J. Appl. Phys. **96**, 5180 (2004).
[12] F. Giannazzo, S. Sonde, V. Raineri, and E. Rimini, Nano Lett. **9**, 23 (2009).
[13] J. Xia, F. Chen, J. Li, and N. Tao, Nat. Nanotechnol. **4**, 505 (2009).
[14] S. Droscher, P. Roulleau, F. Molitor, P. Studerus, C. Stampfer, K. Ensslin, and T. Ihn, Appl. Phys. Lett. **96**, 152104 (2010).
[15] H. Xu, Z. Zhang, and L.-M. Peng, Appl. Phys. Lett. **98**, 133122 (2011).
[16] L. Wang, W. Wang, G. Xu, Z. Ji, N. Lu, L. Li, and M. Liu, Appl. Phys. Lett. **108**, 013503 (2016).
[17] G. S. Kliros, in *Graphene Science Handbook: Size-Dependent Properties*, edited by M. Aliofkhazraei, N. Ali, W. I. Milne, C. S. Ozkan, S. Mitura, and J. L. Gervasoni (CRC Press, 2016).
[18] S. Datta, *Quantum Transport: Atom to Transistor* (Cambridge University Press, 2005).
[19] Q. Li, E. H. Hwang, and S. Das Sarma, Phys. Rev. B **84**, 115442 (2011).