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DOI: 10.1557/adv.2017.490

Characterization of Few layer Tungsten diselenide based FET under Thermal Excitation

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Abstract:

Two-dimensional (2D) materials are very promising with respect to their integration into optoelectronic devices. Monolayer tungsten diselenide (WSe_2) is a direct-gap semiconductor with a bandgap of ~1.6eV, and is therefore a complement to other two-dimensional materials such as graphene, a gapless semimetal, and boron nitride, an insulator. The direct bandgap distinguishes monolayer WSe_2 from its bulk and bilayer counterparts, which are both indirect gap materials with smaller bandgaps. This sizable direct bandgap in a two-dimensional layered material enables a host of new optical and electronic devices. In this work, a comprehensive analysis of the effect of optical excitation on the transport properties in few-layer WSe_2 is studied. Monolayer WSe_2 flakes from natural WSe_2 crystals were transferred onto Si/SiO_2 (270nm) substrates by mechanical exfoliation. The flakes were observed under an optical microscope. A FET based on mechanically exfoliated WSe_2 was fabricated using photolithography with Molybdenum as metal contact and Silicon as back gate and the electronic properties were measured in a wide range of temperatures. The mobility of our device was found to be 0.2 cm^2/V-S at room temperature. The schottky barrier height was found to decrease from 80 meV to 25 meV as the gate voltage increases.

Introduction:

As one of the most promising two-dimensional (2D) materials, graphene, one-atom-thick single layer of carbon atoms packed with honeycomb lattice, has shown exceptional physical, chemical, optical and mechanical properties [1-3]. However, the gapless band structure limits the potential of graphene for digital electronic devices [4,5]. Recently, transition metal dichalcogenides (TMDCs) have attracted great for next-generation nanoelectronic devices due to their intrinsic band gap property and excellent electrical characteristics including their high mobility (~100 cm2/V·s), excellent current on/off ratio (~10^7), and low sub-threshold slope (SS, ~ 70 mV/decade) [1-4]. Furthermore, temperature effects on TMDC materials have been studied by many groups. Among many studies of temperature effects on TMDC layers [6-8], there have been predominant research activities noticeably toward single or/and multi-layer MoS_2 field effect transistors (FETs) with typical n-type characteristics. For example, the single-layer MoS_2 has unique quantum luminescence efficiency [9, 10] and exhibits a high channel mobility (~ 200 cm^2/V-S) and current ON/OFF ratio (10^8) when it was used as the channel material in a field-effect transistor (FET) [11]. However, WSe_2 FETs with typical p-type properties can be very attractive for the applications of nanoscale devices. For example, bulk WSe_2 is a p-type semiconductor with an indirect band gap of ~ 1.2 eV, whereas its monolayer exhibits a direct band gap of ~1.65 eV [12, 13]. The direct band gap of atomically thin TMDs can offer exciting opportunities for potential applications in both digital electronic and optoelectronic devices [14-

18]. For example, it has been recently reported that exfoliated monolayer WSe_2 can be used to create a high performance p-type field-effect transistor (FET) [19].

In this paper, we fabricate few-layer WSe_2 based FET and then study its temperature electrical properties. We analyze the effect of temperature on mobility, subthreshold swing, threshold voltage as well as the influence of temperature on the photo switching behavior of the device.

Experimental:

The FET was fabricated using few-layer WSe_2 as channel and pre-patterned sputtered Mo-contacts are used to contact the nanomembranes underneath to suspend the WSe_2 (Fig. 1a). The metal contacts were fabricated from a photolithography mask designed to allow the suspension of the WSe_2 on top of the contacts. Firstly, a 270 nm SiO_2/Si substrate is used for the transfer of WSe_2 to yield a high optical contrast between the substrate and the WSe_2 nanomembrane; the substrate is cleaned using piranha solution to reduce surface contaminants prior to the transfer. Secondly, standard photolithography process was executed with AZ5214E-IR photoresist to define the contact regions, after which point 100 nm of sputtered Mo was deposited at 200 Watts, 3 mTorr for 20 minutes. After deposition, the Mo was lifted-off with acetone and the surface was further cleaned using stripper (AZ Kwik Strip Remover). The WSe_2 nanomembrane was then mechanically exfoliated from the bulk crystal (2D Semiconductors) using low-tac blue tape (Semiconductor Equipment Corp.) aligned, and transferred to Si substrates using adaptations from the viscoelastic stamping process, [20] using an in house Karl Suss MJB3 mask aligner, where the substrate with Mo contacts was held on the wafer chuck, and the Gel-Film with the WSe_2 nanomembranes was then attached to a clear glass plate (4-inch x 4-inch) and mounted onto the mask aligner. The opto-electronic measurements were conducted using a state-of-the-art Lakeshore Probe Station CRX-4K and an ultra-low noise Semiconductor Parameter Analyzer (Keysight B1500A).

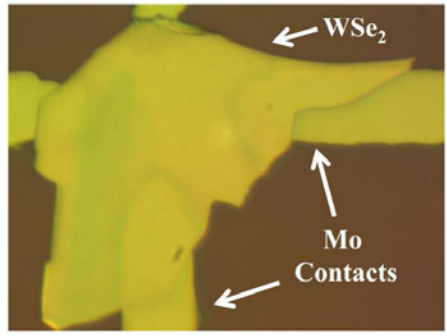

Fig 1: Optical image of the few-layer WSe_2 FET on Si/SiO_2 Substrate with Mo acting as a top gate and Si as a back gate.

Results and Discussion:

The Schottky barriers between the semiconducting channel and the metallic electrodes, which result from the difference between the electron affinity of the semiconductor and the work function of the metal, are expected to play a major role in any conventional photodetector. Hence, we calculated theoretically the schottky barriers for different metals when they form contacts with WSe_2 (Fig. 2). We found Molybdenum as a suitable metal which can be used for ambipolar conduction in the device as it forms similar barrier height w.r.t the conduction band (0.7 eV) and valence band (0.9 eV) of WSe_2. This is clear from Fig. 3 where the transfer characteristics of the device at room temperature are shown. Our few-layered WSe_2 FET shows ambipolar conduction, i.e. yielding a sizeable current for both positive and negative gate voltage. When the temperature is lowered down to 5 K (Fig. 4), the current is found to increase due to very less scattering at that low temperature. This behavior is attributable to disorder-induced carrier localization in the channel as extensively studied in SiO_2/Si MOSFETs.

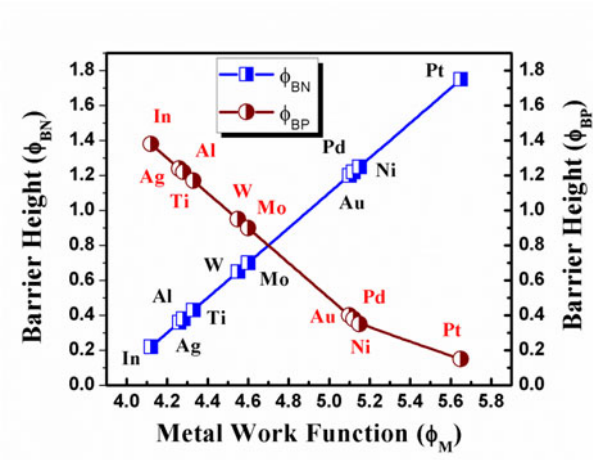

Fig 2: The Barrier Height formed by different metal in contact with WSe_2.

The field-effect mobility of this few-layer WSe_2 device can be estimated based on the equation:

$$\mu = \frac{Ld}{W\varepsilon_o\varepsilon_r V_{DS}} \times \frac{dI_D}{dV_G} \quad (1)$$

where the channel length L is 25 μm, the channel width W is 20 μm, ε_o is 8.854×10^{12} F/m, ε_r for SiO_2 is 3.9, and d is the thickness of SiO_2 (270 nm). The calculated mobility of our device is ca. 0.2 cm^2/V-S. Considering that phonon scattering is enhanced with increasing temperature,

and leads to the degradation in the mobility [21]. Additionally, the reason for low value of mobility is likely that the trap/impurity states exist at the SiO_2 surface in the bottom gate FETs, and the scattering from these charged impurities degrades the device mobility [22]. Reduction of the surface traps/impurities in the bottom gate dielectric is expected to improve the mobility of such a single-layer WSe_2 based bottom-gate FET devices. At high carrier densities, and in samples with reduced disorder, the localization length can exceed the sample size. In this weakly localized state, the 2D system can exhibit an apparent metallic behavior, explained in terms of the temperature dependent screening of fixed charged impurities. For high sample disorder, or at low carrier densities, the system becomes strongly localized, and the temperature dependence of conductivity displays the expected insulating behavior. At high carrier densities, and in samples with reduced disorder, the localization length can exceed the sample size. In this weakly localized state, the 2D system can exhibit an apparent metallic behavior, explained in terms of the temperature dependent screening of fixed charged impurities. For high sample disorder, or at low carrier densities, the system becomes strongly localized, and the temperature dependence of conductivity displays the expected insulating behavior. This crossover from a metallic weakly localized regime at high carrier densities to an insulating strongly localized regime at low carrier densities has been used to explain the MIT in 2D semiconductors [23, 24].

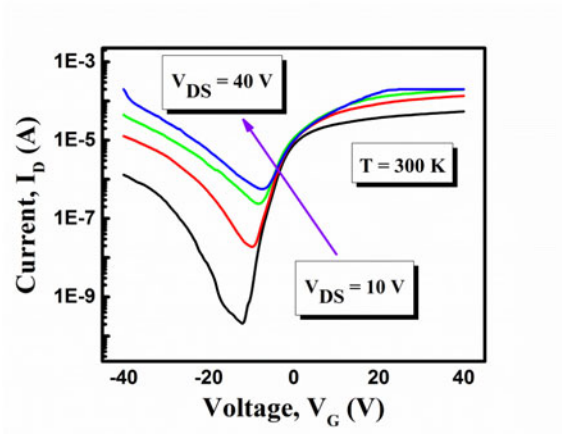

Fig 3: Source to drain current I_{ds} as a function of the back gate voltage V_G and for several values of drain-source excitation voltage V_{DS} at T = 300 K.

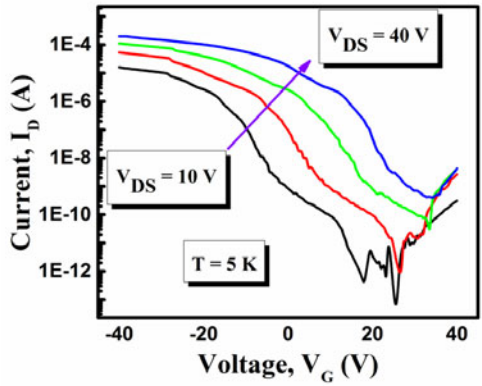

Fig 4: Source to drain current Ids as a function of the back gate voltage V_G and for several values of drain-source excitation voltage V_{DS} at T = 5 K.

We also calculated the temperature dependency on electrical parameters extracted from transfer curves of multilayer WSe_2 FETs. The current on/off ratio was defined as I_{on} (I_D at V_G = -30 V) / I_{off} (I_D at V_G = 30 V). The Subthreshold Swing (SS) was defined as the following equation:

$$SS = \left[\frac{d \log(I_D)}{dV_G} \right]^{-1} \quad (2)$$

The current on/off ratio were deteriorated as the temperature increases from 5 K to 300 K. Furthermore, the off-current increased with temperature increase The SS increased with temperature increase. In the MOSFET theory, the SS value is proportional to temperature.

As discussed above, the metallic electrical contacts were claimed to play a major role in the photoconducting response of FETs based on TMDs, therefore we proceed to analyze the quality of our Mo contacts and evaluate the size of the schottky barriers. The barrier height was found to decrease from 80 meV to 25 meV as the gate voltage was increased from -10 V to 0 V. The decreasing value of ϕ_B with increasing V_G might result from defects and impurities around the contact area which would pin the Fermi level at an arbitrary position relative to the conduction and valence bands. Or it might result from thermally assisted tunneling through a quite thin schottky barrier.

In conclusion we can say that in this work the temperature effect of I-V has been investigated in few-layer WSe_2 FETs systematically. We observed a notable degradation of I-V with temperature increase due to the decrease in mobility. The current on/off ratio and the subthreshold voltage swing were also calculated and their variations with temperature were

analyzed. The schottky barrier height was also calculated from the transfer characteristics and it was found to decrease with increasing gate voltage.

Acknowledgements

We are grateful to the Air Force Office of Scientific Research (grant number FA9550-15-1-0200) who provided support to pursue this work.

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