MRS Advances © 2016 Materials Research Society
DOI: 10.1557/adv.2016.95

Integrating 2D electron gas oxide heterostructures on silicon using rare-earth titanates

Eric N. Jin*[†1], Lior Kornblum[†1], Charles H. Ahn[1,2], and Frederick J. Walker[1]

[1]Center for Research on Interface Structures and Phenomena and Department of Applied Physics, Yale University, New Haven, Connecticut 06511, USA
[2]Department of Mechanical Engineering and Materials Science, Yale University, New Haven, Connecticut 06511, USA

*Corresponding author: eric.jin@yale.edu
[†]Eric N. Jin and Lior Kornblum contributed equally to this work.

ABSTRACT

Integrating oxide heterostructures on silicon has the potential to leverage the multifunctionalities of oxide systems into semiconductor device technology. We present the growth and characterization of two-dimensional electron gas (2DEG) oxide systems $LaTiO_3/SrTiO_3$ (LTO/STO) and $GdTiO_3/SrTiO_3$ (GTO/STO) on Si(001). We show interface-based conductivity in the oxide films and measure high electron densities ranging from ~9×10^{13} cm^{-2} $interface^{-1}$ in GTO/STO/Si to ~9×10^{14} cm^{-2} $interface^{-1}$ in LTO/STO/Si. We attribute the higher measured carrier density in the LTO/STO films to a higher concentration of interface-bound oxygen vacancies arising from a lower oxygen partial pressure during growth. These vacancies donate conduction electrons and result in an increased measured carrier density. The integration of such 2DEG oxide systems with silicon provides a bridge between the diverse electronic properties of oxide systems and the established semiconductor platform and points toward new devices and functionalities.

INTRODUCTION

2-dimensional electron gas (2DEG) systems in oxide heterostructures have been intensively studied, following the initial discovery by Ohtomo and Hwang [1] in the $LaAlO_3/SrTiO_3$ (LAO/STO) system. Similar interface 2DEGs have been subsequently reported in other oxide systems, including rare-earth titanates ($RTiO_3$, *R*TO, where *R* is typically a trivalent rare earth atom) on STO. These all-titanate interface oxide systems have been shown to support higher carrier densities than the LAO/STO system, and include $GdTiO_3$, $LaTiO_3$, $SmTiO_3$, and $NdTiO_3$ [2-8]. *R*TO/STO systems further feature a relatively simple interface structure, as the Ti-O sublattice is continuous across the interface. This feature was suggested as the origin of the higher measured carrier densities in GTO/STO versus LAO/STO [9].

Many oxide 2DEG systems have been demonstrated on ceramic substrates such as STO or $(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$ (LSAT). Developments in growth techniques such as molecular beam epitaxy allow the growth of single crystalline epitaxial STO on Si [10,11]. We apply this STO/Si as a template for integrating the novel phenomena realized in oxide systems with silicon technology. We have recently shown that oxide 2DEG structures can be grown on silicon substrates with both the LTO/STO and GTO/STO materials systems [12-14]. Integration of functional oxides on semiconductors is attractive as it increases potential toward scalable,

silicon-based technology [15]. Moreover, silicon offers a higher thermal conductivity compared to that of typical ceramic substrates such as STO or LSAT, which allows for better heat dissipation, and is appealing for applications requiring a higher power than achievable on ceramic substrates.

In this work, we compare the electronic transport of LTO/STO and GTO/STO structures grown on silicon using molecular beam epitaxy. In order to stabilize the perovskite LTO phase, we reduce the oxygen background pressure during growth of the LTO layers compared to that of the GTO layers. We show that the conduction in both these structures originates at the interfaces of the oxide layers, and we measure a high sheet charge density. One consequence of the lower oxygen pressure for the LTO films is an increase of carrier concentration for LTO/STO/Si compared to that of GTO/STO/Si.

EXPERIMENT

LTO/STO and GTO/STO heterostructures are grown on Si(001) in a custom-built reactive molecular beam epitaxy chamber supporting a base pressure of $<2 \times 10^{-10}$ Torr. All structures are deposited on an initial template layer of 4.5 unit cells (u.c.) of STO/Si [12,13]. Growth is monitored using in-situ reflection high-energy electron diffraction (RHEED) operated at 10 kV. The oxide films are deposited on 2" (001) undoped float-zone Si wafers (>3,000 Ω-cm, Virginia Semiconductor), chosen to reduce substrate conduction in electrical transport measurements. Various thicknesses of LTO and GTO are grown on STO and capped with 15 u.c. STO. The LTO layers are grown at an oxygen pressure of 1×10^{-7} Torr to avoid formation of a pyrochlore phase [16], while GTO layers are grown in an oxygen pressure of 5×10^{-7} Torr, which is identical to the growth pressure of STO. All films are grown at a substrate temperature of 600 °C.

Structural analysis performed by RHEED, x-ray diffraction, and scanning transmission electron microscopy is reported elsewhere [12-14], confirming high quality single crystalline films for both the GTO/STO and LTO/STO deposited on Si. For electrical transport measurements, the 2" wafers are cleaved into approximately 5 x 5 mm^2 samples. After the corners are scratched with a diamond scribe, ~60 nm Au contacts are sputtered, followed by Si-Al wire bonding in the van der Pauw geometry. Measurements are carried out in a Physical Properties Measurement System (Quantum Design) in a magnetic field swept at a range of ±3 T or higher.

RESULTS AND DISCUSSION

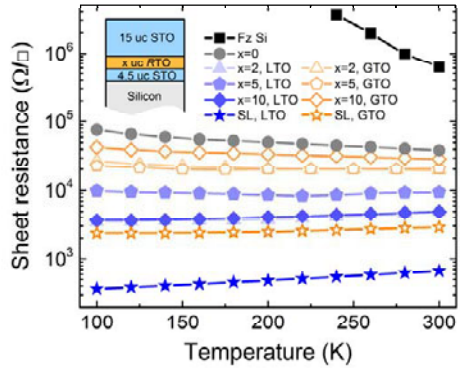

Fig. 1: Sheet resistance as a function of temperature for *R*TO/STO/Si structures (*R* = L and G, indicating LTO and GTO, respectively). All sample structures have a 4.5 u.c. STO layer on Si, and a 15 u.c. STO layer cap for all but the superlattice structures ("SL"). 2, 5, and 10 u.c. of *R*TO are deposited in the sandwich structure, as shown schematically in the top left inset, with "x" denoting the RTO layer thickness. The LTO samples are denoted by filled blue shapes, and the GTO samples are denoted by open orange shapes. The lines are a guide for the eye. Superlattice structures for both LTO and GTO are also shown (stars). For comparison, two control samples of a 19.5 u.c. STO/Si sample ("x=0") and a bare Si sample ("Fz Si") are also plotted.

Sheet resistance as a function of temperature and *R*TO layer thickness is plotted in Fig. 1 for both LTO/STO/Si and GTO/STO/Si structures, where "x" denotes the *R*TO total layer thickness in u.c. The undoped Si substrate by itself is shown for comparison. With x = 0 (i.e. no *R*TO film), the STO/Si film shows semiconducting behavior, which we attribute to residual oxygen vacancies in the oxide. As soon as just 2 u.c. of *R*TO is inserted, the samples show higher conductivity. The LTO films generally display a lower resistance than the equivalent GTO film structures, which we attribute to the lower oxygen pressures required during growth for epitaxial LTO. The reduced oxygen pressure during growth can further increase the number of oxygen vacancies in the STO, which contribute to conduction in the oxide. However, this conductance appears to be isolated to the oxide interfaces and not the bulk *R*TO, as the conductivity behavior appears qualitatively similar for 2, 5, and 10 u.c. *R*TO films. Furthermore, a superlattice structure is grown that has an identical total oxide film thickness (19.5 u.c.) but with 6 interfaces of alternating *R*TO/STO. The LTO superlattice has a structure of 4 u.c. STO on 4 u.c. LTO, repeated 3 times, and the GTO superlattice has a structure of 5 u.c. STO on 5 u.c. GTO, repeated 3 times. Both structures are grown on a template of 4.5 u.c. STO/Si. These superlattice structures show a substantially lower sheet resistance than the other samples. This observation further indicates that conduction is an *R*TO/STO interface effect.

To characterize the carrier density, Hall measurements are performed on a series of samples with varying numbers of interfaces. Carrier density is extracted by the equation R_H =

$R_{xy}/B = 1/(n_s q)$, where R_H is the Hall coefficient, R_{xy} is the transverse resistance, B is magnetic field, n_s is sheet carrier density, and q is the elementary charge. We observe a highly nonlinear R_{xy} vs B behavior at high temperature (>180 K for the LTO samples, and >100 K for the GTO samples) and linear behavior at low temperatures. The nonlinearity may arise from multiple channels of conduction in the heterostructures, with one channel being a very low density of electrons or holes in the bulk of the silicon and the second a much higher density of low mobility electrons in the oxide layers. Despite the carriers in the silicon having a significantly lower density than the 2DEG, the mobilities are typically 2–3 orders of magnitude higher, which results in the nonlinear Hall behavior. Thus, for analysis purposes, we use an intermediate temperature (140 K for LTO samples and 100 K for GTO) to extract carrier densities. We note that the temperature variation of the carrier densities at these temperatures is small.

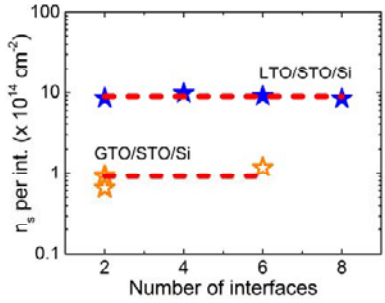

Fig. 2: Hall sheet carrier densities (per interface) measured in *R*TO/STO/Si structures with differing number of interfaces. LTO heterostructures (blue filled stars) have total film thicknesses of 29.5 u.c., and GTO heterostructures (orange unfilled stars) have total film thicknesses of 34.5 u.c. for 6 interfaces and 19.5 u.c. for 2 interfaces. The multiple data points for GTO at 2 interfaces include samples with 2 u.c. GTO and 5 u.c. GTO, showing little variation in measured carrier density. The red lines serve as guides to the eye and represent ~9×10^{14} cm^{-2} $interface^{-1}$ for LTO and ~9×10^{13} cm^{-2} $interface^{-1}$ for GTO.

The measured carrier densities of LTO/STO/Si and GTO/STO/Si are summarized in Fig. 2. The R_{xy}/B slope is negative for all samples measured, indicating electrons as the carrier type. The LTO samples are grown in a series of varying numbers of interfaces, ranging from 2 to 8 LTO/STO interfaces but with a constant total film thickness of 29.5 u.c. to separate the possible contribution of bulk-STO conduction. The GTO samples are grown with 2 and 6 interfaces. The average measured charge density per interface is ~9×10^{14} cm^{-2} for the LTO samples [12] and ~9×10^{13} cm^{-2} for the GTO samples [13]. The carrier density for both materials systems scales with the number of interfaces and further confirms interface conduction as the transport mechanism. We attribute the 10× higher carrier density measured in the LTO samples to the presence of interfacial oxygen vacancies at the LTO/STO interfaces, resulting from the lower growth pressures used. It has been shown in other 2DEG systems that oxygen vacancies can add carriers to the oxide and increase the measured 2DEG density [18]. Because GTO is grown at a higher growth pressure, we expect fewer vacancies, and the measured density is accordingly lower.

These numbers do differ somewhat from previous reports [3] of 3–3.5 × 10^{14} cm^{-2} and may be due to traps in the oxide or at the oxide-semiconductor interface. The electron mobility of the films can be calculated with the equation $R_s = 1/(n_s q \mu)$, where R_s is the sheet resistance and μ is mobility. The mobilities for both the LTO and GTO samples are similar, ranging from ~1–4 $cm^2V^{-1}s^{-1}$ at 140 K-100 K, and are comparable to LAO/STO systems grown on oxide substrates [17-19], while maintaining the advantages of a silicon platform.

CONCLUSIONS

In summary, we have characterized the electrical properties of high quality epitaxial films of LTO/STO and GTO/STO grown on Si(001) which exhibit a 2DEG at the interface of the oxide. The introduction of just 2 u.c. of *R*TO in STO/Si results in the formation of the 2DEG due to carrier transfer from the *R*TO layer. The measured carrier concentration scales with the number of *R*TO/STO interfaces, with ~9 × 10^{14} cm^{-2} $interface^{-1}$ for the LTO/STO/Si structures and ~9 × 10^{13} cm^{-2} $interface^{-1}$ for the GTO/STO/Si structures. The GTO samples are comparably more resistive and have lower carrier density due to a higher oxygen pressure used in growth, which results in a lower concentration of oxygen vacancies we associate with the LTO/STO interface. We conclude that oxide 2DEG heterostructures can be integrated with silicon and have potential in microelectronics technology.

ACKNOWLEDGMENTS

This work was funded by the Office of Naval Research Multidisciplinary University Research Initiative (ONR-MURI) to support the EXtreme Electron DEvices (EXEDE) program, along with support from the National Science Foundation through NSF DMR-1309868 and NSF MRSEC DMR-1119826. The authors thank M. D. Wint and T. McHugh for valuable technical assistance.

REFERENCES

1. A. Ohtomo and H. Y. Hwang, Nature **427**, 423–426 (2004).
2. K. Shibuya, T. Ohnishi, M. Kawasaki, H. Koinuma, and M. Lippmaa, Jpn. J. Appl. Phys., Part 2 **43**, L1178 (2004).
3. P. Moetakef, J. Y. Zhang, A. Kozhanov, B. Jalan, R. Seshadri, S. J. Allen, and S. Stemmer, Appl. Phys. Lett. **98**, 112110 (2011).
4. J. Y. Zhang, C. A. Jackson, R. Chen, S. Raghavan, P. Moetakef, L. Balents, and S. Stemmer, Phys. Rev. B **89**, 075140 (2014).
5. C. A. Jackson, J. Y. Zhang, C. R. Freeze, and S. Stemmer, Nat. Commun. **5**, 4258 (2014)
6. P. Xu, D. Phelan, J. S. Jeong, K. A. Mkhoyan, and B. Jalan, Appl. Phys. Lett. **104**, 082109 (2014).
7. S. S. A. Seo, W. S. Choi, H. N. Lee, L. Yu, K. W. Kim, C. Bernhard, and T. W. Noh, Phys. Rev. Lett. **99**, 266801 (2007).
8. Y. J. Chang, L. Moreschini, A. Bostwick, G. A. Gaines, Y. S. Kim, A. L. Walter, B. Freelon, A. Tebano, K. Horn, and E. Rotenberg, Phys. Rev. Lett. **111**, 126401 (2013).
9. A. Janotti, L. Bjaalie, L. Gordon, and C. G. Van de Walle, Phys. Rev. B **86**, 241108 (2012).

10. R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. **81**, 3014–3017 (1998).
11. J. W. Reiner, A. M. Kolpak, Y. Segal, K. F. Garrity, S. Ismail-Beigi, C. H. Ahn, and F. J. Walker, Adv. Mater. **22**, 2919 (2010).
12. E. N. Jin, L. Kornblum, D. P. Kumah, K. Zou, C. C. Broadbridge, J. H. Ngai, C. H. Ahn, and F. J. Walker, APL Mater. **2**, 116109 (2014).
13. L. Kornblum, E. N. Jin, D. P. Kumah, A. T. Ernst, C. C. Broadbridge, C. H. Ahn, and F. J. Walker, Appl. Phys. Lett. **106**(20), 201602 (2015).
14. L. Kornblum, E. N. Jin, O. Shoron, M. Boucherit, S. Rajan, C. H. Ahn, and F. J. Walker, J. Appl. Phys. **118**, 105301 (2015).
15. X. Gu, D. Lubyshev, J. Batzel, J. M. Fastenau, W. K. Liu, R. Pelzel, J. F. Magana, Q. Ma, L. P. Wang, P. Zhang, and V. R. Rao, J. Vac. Sci. Technol., B **27**, 1195–1199 (2009).
16. A. Ohtomo, D. A. Muller, J. L. Grazul, and H. Y. Hwang, Appl. Phys. Lett. **80**, 3922 (2002).
17. A. Annadi, Z. Huang, K. Gopinadhan, X. R. Wang, A. Srivastava, Z. Q. Liu, H. H. Ma, T. P. Sarkar, T. Venkatesan, and Ariando, Phys. Rev. B **87**, 201102 (2013).
18. Z. Q. Liu, C. J. Li, W. M. Lü, X. H. Huang, Z. Huang, S. W. Zeng, X. P. Qiu, L. S. Huang, A. Annadi, J. S. Chen, J. M. D. Coey, T. Venkatesan, and Ariando, Phys. Rev. X **3**, 021010 (2013).
19. A. Fête, C. Cancellieri, D. Li, D. Stornaiuolo, A. D. Caviglia, S. Gariglio, and J.-M. Triscone, Appl. Phys. Lett. **106**, 051604 (2015).