

II-VI Material Integration With Silicon for Detector and PV Applications

T.A. Gessert†, E. Colegrove*, B. Stafford*, R. Kodama†, Wei Gao*,
 H.R. Moutinho**, D. Kuciauskas**, R.C. Reedy**, T.M. Barnes**, and S. Sivananthan*

†EPIR Inc. Bolingbrook, IL 60440

*University of Illinois at Chicago, Physics Department, Chicago, IL 60612

**National Renewable Energy Laboratory, Golden, CO 80401

ABSTRACT

Heteroepitaxial growth of high-quality II-VI-alloy materials on Si substrates is a well-established commercial growth process for infrared (IR) detector devices. However, it has only recently been recognized that these same processes may have important applications for production of high-efficiency photovoltaic devices. This submission reviews the process developments that have enabled effective heteroepitaxy of II-VI alloy materials on lattice-mismatched Si for IR detectors as a foundation to describe recent efforts to apply these insights to the fabrication of multijunction Si/CdZnTe devices with ultimate conversion efficiencies >40%. Reviewed photovoltaic studies include multijunction Si/CdZnTe devices with conversion efficiency of ~17%, analysis of structural and optoelectrical quality of undoped CdTe epilayer films on Si, and the effect that a Te-rich growth environment has on the structural and optoelectronic quality of both undoped and As-doped heteroepitaxial CdTe.

INTRODUCTION

Large-area, low-cost, high-quality, II-VI semiconductor materials are needed for the next generation of IR-detector and solar-photovoltaic (PV) systems. Many present state-of-the-art infrared focal plane arrays (IRFPAs) are fabricated using molecular-beam epitaxy (MBE) of HgCdTe (MCT) absorbers onto CdZnTe (CZT) substrates. CZT is a logical substrate choice because Cd_{0.94}Zn_{0.06}Te can be lattice matched to the Hg_{0.80}Cd_{0.20}Te alloy used for long-wavelength IR (LWIR) detectors, while slight variations in Zn content can accommodate absorber materials for mid-wavelength and short-wavelength IR detectors (MWIR and SWIR, respectively). Unfortunately, there is a lack of large-area, high-quality CZT substrates due to their high production cost. Further, the difference in thermal expansion coefficients between CZT substrates and Si-based readout integrated circuits (ROICs) presents drawbacks for CZT substrates for next-generation IRFPAs applications, becoming a particular concern with increasing size and thermal-cycle requirements of the IRFPAs.

In contrast to CZT substrates, the use of silicon substrates for growth of MCT IRFPAs can provide advantages including substrate size, surface reproducibility, mechanical robustness during processing and thermal cycling, reduced cost, and fewer issues related to Cu diffusion. Taken together, MBE growth on silicon substrates makes it possible to fabricate IRFPAs with reduced cost and more dies per wafer. Although Si is not lattice-matched to MCT, a versatile accommodation template process has been developed at EPIR that enables the fabrication of low-cost, SWIR, MWIR, and LWIR IRFPAs on Si substrates. Specifically, high quality n-type MCT (~1.5x10¹⁵ cm⁻³) layers have been grown on CdTe/Si substrates that show exceptional compositional and thickness uniformity over 6-inch diameter substrates. The layers further

demonstrate low surface defect densities (e.g., voids $\sim 5 \times 10^2 \text{ cm}^{-2}$, micro-defects $\sim 5 \times 10^3 \text{ cm}^{-2}$) and low etch pit density ($\sim 3.5 \times 10^6 \text{ cm}^{-2}$). This material has been used to fabricate planar-device IRFPAs with several array formats (i.e., $320 \times 256 \times 30\text{-}\mu\text{m}$ pitch and $640 \times 512 \times 15\text{-}\mu\text{m}$ pitch) using arsenic implantation to achieve p-type doping. Noise characterization of $320 \times 256 \times 15\text{-}\mu\text{m}$ MWIR FPA devices revealed an impressive noise equivalent temperature difference (NETD) of 13.8 mK at 85 K for a 1 ms integration time with f#2 optics. The NETD operability is 99% at 120 K, with a mean dark current noise of $8.14 \times 10^{-13} \text{ A/pixel}$. High quality thermal imaging was obtained from these IRFPA up to an operating temperature of 150 K. Because of these advancements, the use of Si substrates for fabrication of IRFPAs is increasing.

The success of these IRFPA devices grown on Si also has significant alignment for the development of high-efficiency, multi-junction photovoltaic (PV) devices. Currently, the highest performing PV cells ($\sim 46\%$ efficiency) [1] are based on multijunction crystalline III-V materials. However, because the present generation of these devices must be grown on III-V substrates, their high cost limits deployment to very high-value applications - such as space power. In contrast, the EPIR's technology for growing crystalline II-VI-alloy materials on Si has the potential of producing not only much lower-cost PV devices compared to III-V devices (i.e., factor of ~ 5 cost reduction) [2] but because more ionic bonding makes II-VI materials less sensitive to defects, II-VI solar cells may ultimately yield higher efficiencies than III-V devices [3]. Because growth on Si also enables the use of kerfless Si-film material with thickness as low as 10 μm , mechanically robust devices with specific power of $>1000 \text{ W/kg}$ become possible. Although CdTe has a near-ideal band gap (E_g) for terrestrial single-junction solar cells (as demonstrated by the recent First Solar world record efficiency of 22.1% for a single-junction polycrystalline CdTe device), [4] the $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$ alloy ($0.45 < x < 0.5$, $E_g = \sim 1.7 \text{ eV}$) provides a near optimum band gap for a top-cell partner for a Si/CZT tandem-cell device. Furthermore, the available band gap of $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$ spans an energy range of ~ 1.46 to $\sim 2.24 \text{ eV}$, far above the accessible range for III-V top-junction materials. This is important because cells with three or more junctions are being considered in future multi-junction designs. Finally, while it is well known that CdTe is notoriously difficult to dope p-type, making fabrication of optimum homojunction devices difficult, p-type doping is significantly easier in the CZT alloy. [5]

In this paper, we discuss recent studies at the University of Illinois at Chicago (UIC) aimed at developing CdTe-alloy materials with a view to ultimately incorporate a CZT top cell into a CZT/Si tandem PV device with a near-term efficiency of $>30\%$, and longer-term performance $>40\%$. This work expands earlier proof-of-concept studies at EPIR Technologies that demonstrated multi-junction efficiency of $\sim 17\%$ [6]. Specifically, the paper combines studies of CdTe growth on Si, stoichiometry control during growth, and doping incorporation (As).

EXPERIMENTAL DETAILS

The CdTe heteroepitaxial layers are produced at the UIC Microphysics Laboratory with either a Riber Opus 5-inch MBE system (indicated as System W) or a Riber V100 9-inch system (indicated as System E). For both systems, 3-inch Si (211) wafers are used as the substrates. The CdTe/Si heteroepitaxy techniques have been developed over the past 25 years at UIC and EPIR [7,8] and include the use of a double-side polished (211) 3-inch-diameter Si wafers that are boron doped to 30–70 $\text{ohm}\cdot\text{cm}$. The wafers are cleaned *ex situ* using a modified RCA cleaning process, after which they are loaded into the respective MBE system. Systems are pumped to pressures $< 1 \times 10^{-9}$ Torr, where the wafers undergo a dehydration bake at $\sim 400^\circ\text{C}$, followed by a

thermal oxide strip at $>1000^{\circ}\text{C}$ (note that all MBE temperatures quoted are uncorrected thermocouple values). Deposition of CdTe layers on Si begins with the fabrication of a multilayer, lattice-accommodating “template.” Although the template-layer parameters can vary depending on intended application, the template produced for use with CdTe or CdZnTe PV materials included a sub-monolayer of As, followed by ~ 15 nm of ZnTe. The ZnTe layer is deposited using migration-enhanced epitaxy (MEE), where beam flux from elemental sources of Zn and Te (99.99999% purity) are alternated with a short time between atomic layers to allow surface migration to improve two-dimensional growth. In this template design, the As layer passivates dangling bonds at the Si, improving structural and adhesion integrity, whereas the ZnTe pseudomorphic layer maintains the (211)B orientation (i.e., the passivation layer is thinner than the critical thickness at which misfit dislocations occur). Following ZnTe deposition, the substrate temperature is reduced to the CdTe growth temperature of 325°C .

Although CdTe layers used for HgCdTe IR-detector devices are generally ~ 10 μm thick (and are called CdTe buffer layers), these initial studies for PV devices have included CdTe layers that were both thinner and thicker - to allow correlation of the optoelectronic properties of the CdTe layer with structural properties. CdTe films produced for what is referred to in this paper as the *initial study* were undoped and deposited a nominally stoichiometric CdTe effusion source. CdTe film produced for what is referred to as the *intermediate and recent studies* were produced using co-deposition from CdTe and Te effusion sources (99.99999%-purity), and a thermal cracker for As. These sources were controlled to produce a growth rate of ~ 1 $\mu\text{m hr}^{-1}$.

Films were analyzed using a combination of techniques. Analyses at UIC and EPIR immediately following deposition included film-thickness uniformity using mapping IR spectroscopy (~ 35 -point maps, Fourier transform infrared spectroscopy [FTIR]) in the wavenumber range of $400\text{--}6000$ cm^{-1} [using a Thermo Nicolet Nexus model 870 FTIR spectrometer with KBr beamsplitter and DTGS-TEC detector]. Surface-quality uniformity was performed using a combination of multi-point Nomarski optical imaging (5-points on wafer), and whole-wafer optical image capture of low-angle scattered white light. Crystalline uniformity was assessed using mapping X-ray diffraction double-crystal rocking curve (DCRC, with std. dev. calculated from ~ 35 -point wafer maps of the full width at half maximum [FWHM] of the CdTe $\langle 422 \rangle$ peak [Bruker AXS Diffraktometer D8 with a high-resolution X-ray diffraction system employing a Ge(200) four-bounce beam filter for the Cu K source]).

Analysis performed at NREL included electron backscatter diffraction (EBSD) to assess if the films demonstrated any polycrystalline artifacts (EDAX Pegasus system with Hikari EBSD detector, housed in a field-emission scanning electron microscope FEI Nova 630). Cross sections of “cleaved” films for EBSD analysis were ion-beam milled for 5–10 h using a JEOL ion-beam cross-section polisher operated at 4 kV. NREL analysis also included room-temperature 2-photon excitation time-resolved photoluminescence (2PE-TRPL) performed at an analysis wavelength of 820 nm, using an excitation wavelength of 1120 nm, a laser repetition rate of 1.1 MHz, and 0.3 ps laser pulses. [9] Because the two-photon absorption coefficient is much lower than a one-photon absorption coefficient, carriers are generated nearly uniformly throughout the film volume defined by the excitation beam size and the $\sim 6\text{--}18$ μm film thickness. Secondary ion mass spectrometry (SIMS) was performed either at NREL or at Evans Analytical Group. NREL SIMS was performed using a Cameca IMS-5F instrument. All SIMS data presented here have a minimum detection limit for As in the CdTe samples measured of $<1 \times 10^{15}$ cm^{-3} .

RESULTS AND DISCUSSION

Initial Investigations – Effect of Thickness on Stoichiometric CdTe MBE Growth

Because most historic studies on heteroepitaxy of II-VI materials on Si have been directed at development of MCT detectors, relatively few studies had focused on studying the structural and other material properties of the binary CdTe material. Figure 1 shows initial results where the structural quality of a CdTe heteroepitaxial layer was studied as a function of layer thickness. In this study, and consistent with earlier studies where the CdTe layer was used as a structural buffer for MCT devices, structural quality is seen to increase as the CdTe layer thickness increases from ~400 arcs at ~1 μm thickness, to ~60 arcsec at a thickness of ~10 μm . The CdTe structural quality of ~60 arcsec at ~10 μm is consistent with the best-quality heteroepitaxial layers used to produce commercial MCT detectors, but the DCRC FWHM remains higher than the highest quality *bulk-crystal* DCRC values - of ~20 arcsec. This previous work also indicated that opto-electronic quality of the films improves with structural quality, as assessed with TRPL. [10] Specifically, modeling the resulting minority carrier lifetime (τ) of the thicker heteroepitaxial layers suggests that τ should be sufficient for required high-efficiency device performance (i.e., note that the measured minority carrier lifetime from 2PE-TRPL from all of the the CdTe layers is reduced by surface recombination). [11]

At the time of these initial demonstrations, and although the DCRC analysis indicated high structural quality, uncertainty remained regarding the spatial extent of crystallinity for the CdTe epilayers. For this reason, plan-view EBSD analysis was undertaken to determine if any features representative of an extended multi-crystalline nature may be present in the epilayers. As shown in Figure 2, plan view EBSD analysis did not reveal multiple crystal orientations, while pole figure analysis confirmed a crystalline film with (211) orientation slightly off the normal, suggesting only that a slight misorientation with the substrate existed. Taken together, the structural and electrical analyses of these initial films suggested: (1) The structural quality of the films was somehow related to electrical quality, and (2) the structural and electrical quality of

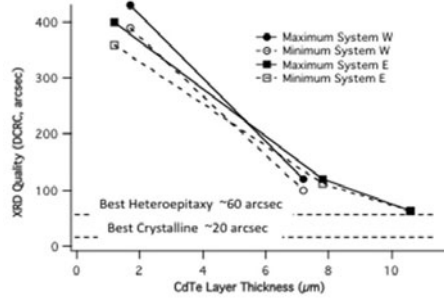


Fig. 1. DCRC crystal quality vs. FTIR-measured CdTe layer thickness for one early set of samples. The dotted and solid lines show the minimum and maximum FWHM, respectively. The dashed lines indicate the best heteroepitaxy (~60 arcsec) and best crystalline (~20 arcsec) values.

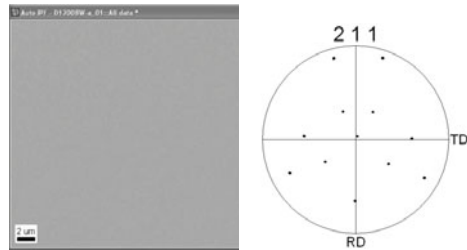


Fig. 2. Left – EBSD image of ~10- μm -thick CdTe layer on Si. Right – Pole figure confirming crystalline film with (211) orientation slightly off surface normal (spots enlarged for clarity).

the films were dependent on film thickness, at least for film thicknesses in the range of 1-10 μm . Therefore, it was believed subsequent sample sets may benefit from film thicknesses of at least 10 μm .

Intermediate Investigations – Effect of Te-Rich MBE Growth Conditions

With foundations established for heteroepitaxial Si/CdTe film growth from the initial study, a second set of films were produced to probe a widely held belief that the anion vacancy (i.e., Te vacancy, V_{Te}) could be a detrimentally important defect in CdTe and related-alloy material systems. [12] Based on guidance from the initial study, a sample set was designed to have film thickness of approximately 10-20 μm , but with an additional Te flux present during film growth. Table I provides details on these samples, indicating 0-33% additional Te flux for some samples.

TABLE I
Structural and Electro-Optical Analysis Of Undoped CdTe Layers
Grown Heteroepitaxially On (211) Si Substrates.

ID	Thickness (μm)	Te Flux (%)	DCRC (arcsec)	DCRC St.Dev. (arcsec)	2PE-TRPL (ns)
W13009	10.7 (Thin)	20	74	2.8	1.8
W13007	10.0 (Thin)	0	102	80.7	1.2
W13010	6.3 (Thin)	12	109	11.4	1.1
W13008	18.0 (Thick)	0	67	40.2	2.3
W13028	14.8 (Thick)	33	73	2.5	1.7
W13029	14.4 (Thick)	12	71	3.1	1.7

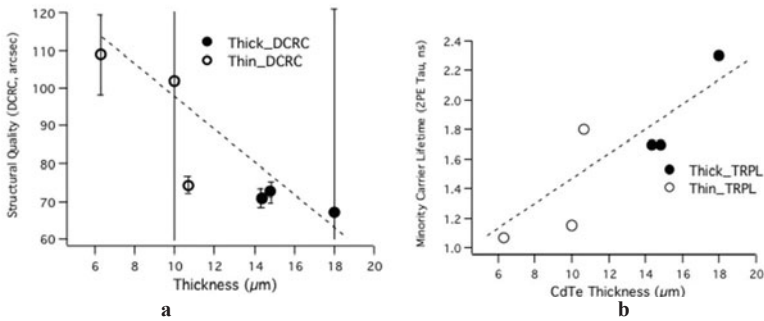


Fig. 3. Results of intermediate sample set produced were both sample thickness and Te overpressure were varied to explore the interrelationship of these parameters on (A) structural quality (DCRC FWHM) and (B) minority-carrier lifetime (τ , 2PE-TRPL). Note that in these figures, “thin” and “thick” samples are defined as less than, or greater than, $\sim 12 \mu\text{m}$, respectively.

Because earlier studies (see Fig. 1) had shown that CdTe film thickness can be strongly linked to material structural quality, Figure 3 shows the intermediate sample set's key quality parameters (i.e., DCRC FWHM and τ) plotted as a function of film thickness. Although some thickness correlation may be inferred from this figure, especially in τ (see Fig 3b), the structural quality revealed film thickness was not necessarily the only important growth parameter, especially for areal reproducibility of structural quality, as shown by the large std. dev. error bars in Fig. 3a. Considering this observation, the data in Fig. 3 was re-plotted as a function of Te overpressure - rather than as a function of thickness. As shown in Figure 4, this analysis revealed, if the Te overpressure exceeded $\sim 12\text{-}14\%$, both structural quality and τ improved significantly. This improvement was especially noteworthy for the films that were considered "thin" (i.e., less than $\sim 12\text{-}\mu\text{m}$ thick, as shown in Fig. 3 and Table I). In this regard, Fig. 4 suggests that both "thick" and "thin" films can benefit structural and electrical from Te-rich growth conditions. This observation is similar to historic observations of the PV absorber material CuInGaSe (CIGS), where present high-performance polycrystalline absorber materials are deposited in a Se-rich environment. However, in the case of CIGS, the Se overpressure is typically 500-700% (i.e., 5-7 times the arrival flux of the Cu + In + Ga). Although the amount of Te overpressure for CdTe shown here ($>12\%$) that leads to significant structural and electrical improvement is significantly less, one should note that this CdTe observation is for MBE growth at ultra-high vacuum conditions, while the CIGS observations relate primarily to co-evaporation under higher-pressure (i.e., high-vacuum) conditions. Although it is expected that at some Te overpressure a Te-on-Cd antisite defect will form (Te_{Cd}), and this defect has been suggested to be even more detrimental than the V_{Te} defect, [13] at this time sufficient studies have not been performed to determine if and at what Te overpressure the Te_{Cd} may become observable in either the structural or electrical properties of the film.

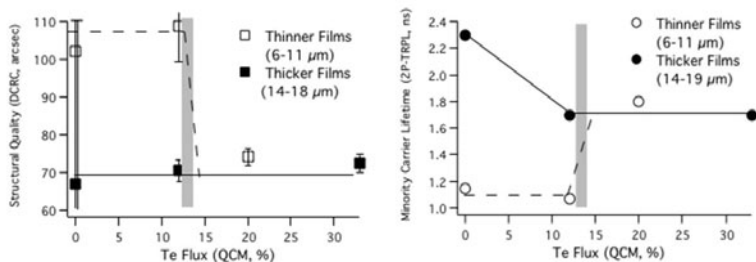


Fig. 4. Data shown in Fig. 3, but now plotted as a function of Te flux. Figure shows that there is a point at $\sim 12\%$ flux where both the structure and τ improve, regardless of CdTe film thickness.

The correlation of structural and optoelectronic analyses (DCRC and 2PE-TRPL) described above suggests that the Te overpressure improves both structural and optoelectronic quality, especially of thin CdTe films. However, it must be considered that both the DCRC and 2PE-TRPL analysis techniques probe relatively deeply into the bulk of the CdTe heteroepitaxial films; thus, details of the effect of Te overpressure, especially as a function of depth, remain

uncertain. To investigate this, EBSD cross sections were analyzed near the Si/CdTe interface for several undoped heteroepitaxial CdTe films. Although initial *plan-view EBSD* analysis confirmed that Te overpressure during growth improved structural quality, initial cross-sectional surfaces formed during the cleaving of the CdTe films to enable *cross-sectional EBSD* were too rough for optimum EBSD. For this reason, several of these samples were subjected to further sample preparation using cross-sectional ion-beam milling to reduce surface roughness and to suppress any cleave-induced structural artifacts.

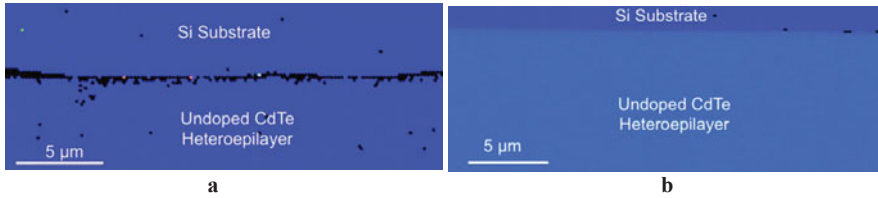


Fig. 5. Cross-sectional EBSD of Si/CdTe interface (a) without Te overpressure, and (b) with ~14% Te overpressure.

Figure 5a shows EBSD analysis of an ion-beam-milled cross-section of the initial ~5 μm of undoped CdTe grown heteroepitaxially on Si (note that the total undoped CdTe film thickness for this sample was ~11 μm). The figure shows that the EBSD software was able to correlate the resulting Kikuchi patterns to known crystalline orientations for the majority of the Si and CdTe layer. However, as indicated by the dark artifacts in the image, some regions of the bulk CdTe could not be correlated, especially near the interface between the CdTe film and Si substrate. Because the width of this interface region generally contains 3–5 EBSD pixels, it is likely this lack of correlation represents actual structural disruption at the CdTe and Si interface, rather than an EBSD analysis artifact. These observations in Fig. 5a are not unexpected, because the lattice difference between (211) Si and CdTe is significant. Specifically, although the As and ZnTe accommodation “template” layers are known to produce CdTe films with sufficiently high quality for IR detectors, the EBSD-measured misorientation between the surface normal directions for the Si and CdTe layers remains at ~3°–4°. Although detailed EBSD analysis of undoped CdTe films grown under Cd-rich conditions has not yet been performed, initial analysis of CdTe films that were doped lightly with Cd₃As₂ (i.e., As content at mid 10¹⁵ cm⁻³) shows very similar results to that shown in Fig. 5a. Initial high-resolution EBSD analysis of this disordered region has not yet revealed significant additional insight.

In contrast to Fig. 5a, Fig. 5b shows a surprising result. First, for similarly prepared Si/CdTe EBSD cross-sections, if the CdTe was deposited with a ~14% Te overpressure, EBSD analysis reveals significantly fewer regions in the CdTe film where the Kikuchi pattern could not be correlated (i.e., the crystal quality of the entire CdTe films appears higher than for film shown in Fig. 5a). Second, the interface region between the Si and CdTe reveals significantly less structural disruption. This is true even though the EBSD-measured misorientation in the samples produced with Te overpressure (Fig. 5b) is the same as for the sample shown in Fig. 5a (i.e., ~3°–4° for both samples). It should also be noted that the total thickness of the undoped film shown in Fig. 5b is significantly thinner than the film shown in Fig. 5a (i.e., ~5.5 μm vs. ~11 μm, respectively). Because the thinner film (Fig. 5b) demonstrates higher structural quality than the

thicker film (Fig. 5a), this supports the trends identified by DCRC analysis of Fig. 4—that Te overpressure facilitates higher as-grown structural quality, especially for CdTe heteroepitaxial films of $< \sim 10\text{-}\mu\text{m}$ thickness.

The observations that Te-rich growth conditions can yield improved as-grown structural and optoelectronic quality in heteroepitaxial CdTe films deposited onto Si might be viewed, to some extent, to be in contrast with recent reports that Cd-rich stoichiometries yield higher τ for bulk CdTe materials [13]. Several possibilities can be suggested to explain this seeming inconsistency. First, in the earlier work [13] DCRC analysis of the bulk materials was not used to assess structural quality as a function of stoichiometry. Therefore, the lower lifetime seen in the Te-rich samples of [13] may be related to the (possible) multiphase structure suggested by comparative X-ray analysis of the samples of the earlier bulk material set. Second, the heteroepitaxial thin *films* studied here are much thinner than the *bulk materials* studied earlier (as the term *film* implies). Therefore, the 2PE-TRPL analysis is likely to be more influenced by surface recombination for these *films* compared to the earlier *bulk* samples. In this case, one might further suspect that the reduced disorder noted with EBSD at the Si/CdTe *film* interface for the Te-rich samples may reduce surface (i.e., back interface) recombination. Thus, the related 2PE-TRPL analyses may be influenced by a higher-quality interface—rather than sensing only differences in the CdTe bulk. Finally, and as suggested earlier, although the amount of source and ambient contamination during MBE film synthesis is very low (at least compared to most CdTe film-synthesis processes), it should be considered that each MBE system is unique, and residual source/ambient contamination levels in the resultant films will depend on both long-term and recent system use. Therefore, it is possible that the observations reported here may depend on the particular MBE system. The likelihood of all these possibilities are presently being investigated.

Recent Investigations – Doping of MBE Grown CdTe with As

The results discussed so far in this submission have focused on undoped CdTe films heteroepitaxially grown on Si. Although DCRC and TRPL measurements can provide indications of structural and electrical quality for these undoped films, a $10\text{-}\mu\text{m}$ thick *undoped* CdTe heteroepitaxial films remain too resistive to assess critical electrical properties of carrier concentration and mobility using Hall measurements. While Cu is presently the primary acceptor dopant species in polycrystalline CdTe used for PV solar cells and commercial modules, [14] control of the Cu incorporation and electrical activation is difficult, [12] while excessive Cu incorporation can lead to problems with long term device stability. Although improving understanding of the historic Cu acceptor remains an important area of investigation, recent studies, focused on developing higher performance and more stable CdTe PV devices, are considering substitutional anion acceptor dopants (i.e., N, P, As, Sb) because of their expected low ionization energy [15] and thermal stability. For the recent studies described here, As was chosen as an initial anion substitutional acceptor dopant. Although the source of As dopant used during MBE deposition included both pure As from a cracker cell, and some studies with As from a Cd_3As_2 effusion source (thus producing also a Cd-rich growth condition), the data presented here discusses primarily As incorporated with the elemental cracker source during growth - both with, and without, Te-rich deposition conditions. Other recent publications discuss initial results of CdTe:As/Si heteroepitaxy using a Cd overpressure. [16]

Results of CdTe:As/Si films produced by MBE revealed trends consistent with previous studies [16,17] indicating that As could be incorporated into the growing CdTe film, but the

structural quality of the films was reduced for even small concentrations of As - for films that did not include a Te overpressure. Specifically, Figure 6b shows, DCRC FWHM values increases from its undoped value of ~ 60 arcsec (see Fig. 1) to ~ 100 arcsec when even 1.0% As flux is added to the CdTe growth flux (yielding $\sim 1 \times 10^{16} \text{ cm}^{-3}$ SIMS-measured As incorporation, see Fig. 6a) and increases further to ~ 200 arcsec with As incorporation as low as 1.5%. Higher As incorporation further degrades the film structure (>300 arcsec shown in Fig. 6b for As flux of $\sim 2\%$), with the structure becoming polycrystalline as the As incorporation becomes uncontrollably high ($\geq \text{mid } 10^{20} \text{ cm}^{-3}$). It has been suggested the onset of the polycrystalline film structure, and uncontrolled As incorporation, may due to the formation of an As-related secondary phase, such as As_2Te_3 [16,18,19] or Cd_3As_2 . In contrast, Fig.6 shows that adding $\geq \sim 14\%$ Te flux during film growth can yield a much wider process window for As incorporation, while retaining the structural quality. Specifically, by adding Te overpressure of $\geq \sim 14\%$, As flux can be increased to at least 5% while maintaining as-grown DCRC FWHM values of <150 arcsec. At these conditions, As incorporation can be controlled to provide incorporation of $\sim \text{mid } 10^{16} \text{ cm}^{-3}$. Although not reported here, appropriate activation of the As dopant [20] has led to net-acceptor concentrations of $\sim \text{low } 10^{16} \text{ cm}^{-3}$, suggesting activation efficiencies of $\sim 50\%$ at this early stage of the research.

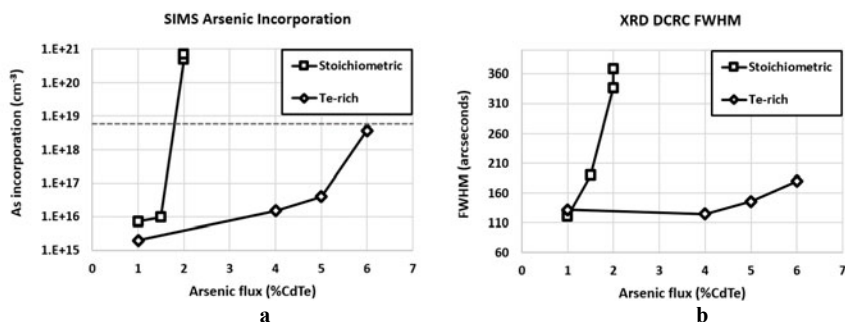


Fig. 6. (a) SIMS-measured As incorporation and (b) DCRC FWHM structural quality as a function of As flux for films grown with and without Te overpressure. The dotted line indicates the approximate onset of polycrystalline film structure in extent of As incorporation.

To investigate the origin of the structural quality reduction in CdTe with increasing As incorporation, cross-sectional EBSD analysis was performed on some of the As-doped samples. Figure 7 shows $\sim 6 \mu\text{m}$ of As-doped CdTe film (2% As flux) grown onto a $\sim 12 \mu\text{m}$ CdTe buffer layer. In this figure, and similar to Fig. 5, EBSD was able to correlate the resulting Kikuchi patterns to known crystalline orientations for the majority of the Si and undoped CdTe layer. However, EBSD was not able to correlate the As-containing region, suggesting a significant reduction in structural quality for this heavily As-containing CdTe layer (note that the SIMS-measured As content of this layer was $\sim 2\text{-}6 \times 10^{20} \text{ cm}^{-3}$). Because visual and DCRC FWHM analysis suggested that *lower* As incorporation often does not lead to the onset of polycrystalline films and excessive As concentration ($< \text{mid } 10^{18} \text{ cm}^{-3}$, see also Fig. 6 and [18,19]), films with a lower SIMS-measured concentration of As were next analyzed with cross-sectional EBSD to determine if EBSD may also reveal indications that can be correlated to the improved structural quality suggested in Fig. 6.

Figure 8 shows two samples that demonstrate lower SIMS-measured As concentrations compared to the sample shown in Fig. 7 (both samples in Fig. 8 have SIMS-measured As incorporation from mid 10^{15} to mid 10^{16} cm^{-3}). Fig. 8a shows a 9- μm thick CdTe:As layer (2% As flux, As content $\sim 4 \times 10^{15}$ cm^{-3} , no undoped buffer layer used in this sample) revealing, although some regions of the CdTe:As layer where the Kikuchi patterns could not be correlated to known crystal orientations, most of the CdTe:As layer could be correlated. In contrast, the cross-sectional EBSD shown in Fig. 8b for a sample grown with much higher As content (4% As flux, As content up to 5×10^{16} cm^{-3}), but with a 14% Te overpressure, shows essentially no regions where EBSD could not be correlated to known crystal orientations within the CdTe:As layer, no uncorrelated regions at the CdTe/CdTe:As interface, and further - showing almost no uncorrelated regions at or near the CdTe/Si interface. These results are very similar to the result shown in Fig. 5 for *undoped* CdTe, and strongly suggest that the Te overpressure can provide a significant benefit of allowing not only wider process latitude for As incorporation during growth without loss of structural and compositional control, but significant reduction in the formation of secondary phases both within the as-grown CdTe:As layer, and at the CdTe/Si or CdTe:As/Si boundary. [21]

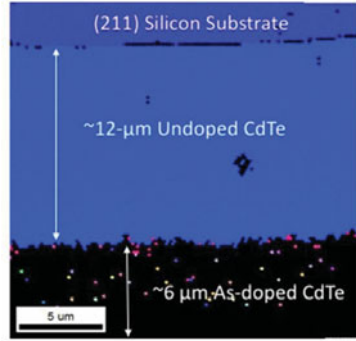


Fig. 7. (W13027) EBSD image of heavily As-doped CdTe sample grown without Te overpressure. SIMS-measured As concentration in the CdTe:As layer is $\sim 6 \times 10^{20}$ cm^{-3} .

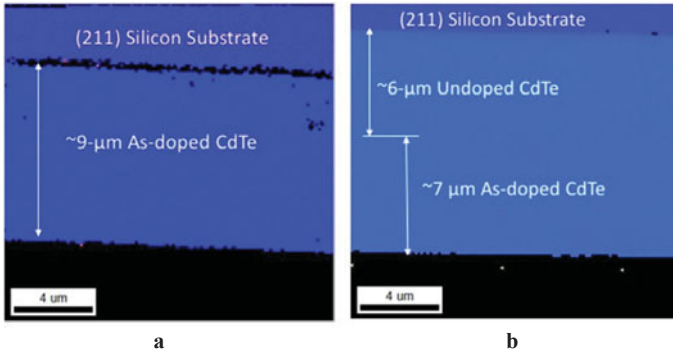


Fig. 8. Left (W13032:I3)- region of CdTe:As sample demonstrating a low As concentration (2% As flux, $\sim 4 \times 10^{15}$ cm^{-3} , 244 arcsec) and without Te overpressure. Note that no undoped buffer layer was used in this sample. Right - (W13042) CdTe:As sample deposited at high As flux (4% As flux, $0.5\text{-}5 \times 10^{16}$ cm^{-3} , 125 arcsec) but with Te overpressure (14%).

CONCLUSIONS

The fabrication of crystalline CdTe layers formed onto Si substrates represents an important option for the development of test structures to probe the limitations of related PV devices. This contribution reviews recent studies of CdTe/Si samples fabricated at UIC detailing the combined effects of thickness, growth stoichiometry, and As doping. Correlations between structural and opto-electronic quality shows that the use of stoichiometry control is likely to be a beneficial process-control parameter for reproducible growth of undoped and doped CdTe films that embody also optoelectronic quality needed to reduce bulk recombination to a level acceptable for high-efficiency CdTe or CdZnTe devices grown on Si.

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