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Low Temperature Metalorganic Chemical Vapor Deposition of Semiconductor Thin Films for Surface Passivation of Photovoltaic Devices

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ABSTRACT

Three II-VI wide bandgap compound semiconductors have been investigated for surface passivation of various photovoltaic devices. First part of this work focuses on the surface passivation of HgCdTe IR detectors using CdTe. A new metalorganic chemical vapor deposition (MOCVD) process has been developed that involves depositing CdTe films at much lower temperature (< 175°C) than the conventional processes used till now. Deposition rate as high as 420nm/h was obtained using this novel experimental setup. Favorable conformal coverage on high aspect ratio HgCdTe devices along with a significant minority carrier lifetime improvement was obtained. Another II-VI semiconductor, namely, CdS was investigated as a surface passivant for HgCdTe IR detectors. It was deposited by MOCVD as well as atomic layer deposition (ALD) and was studied for optimal conformal coverage on high aspect ratio structures. Surface passivation of p-type Si wafer has also been demonstrated using p-ZnTe grown by MOCVD, for possible application in solar cells. Preliminary work showed a remarkable improvement in the minority carrier lifetime of Si light absorbing layer after passivation with a thin layer of ZnTe.

INTRODUCTION

Photovoltaic devices are an essential part of every phase of life today. A photovoltaic device is an application of a semiconductor p-n junction which converts light into an electrical signal. Photons are absorbed by the semiconductor lattice creating electron-hole pairs. The generated minority carriers diffuse though the lattice and are separated by the p-n junction electric field producing an external voltage. This principle of light conversion is mostly utilized in solar cells and infrared (IR) detectors. Starting from electricity generation using solar cell panels to medical imaging using IR detectors, these devices find a wide variety of applications.

Over the years, structures of such devices and their fabrication processes have become increasingly intricate pushing the limits of their efficiencies. Such advancement in technology has been possible by developing advanced growth techniques like chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) coupled with effective surface and interface engineering [1]. Deposition of a thin insulating film, called a surface passivation layer has become one of the major aspects of fabrication of photovoltaic devices. It is used to enhance the electrical performance of the device as well as its chemical stability. Semiconductor surfaces are generally quite different from the bulk due to contamination during the fabrication process or

abrupt termination of crystalline periodicity at the surface which results in broken bonds. The surface properties often become the dominant contributor to the electrical properties of the device giving rise to high leakage currents [2]. A passivation film satisfies the dangling bonds and protects the surface from external exposure minimizing the effect of the surface on the electrical performance of the device.

Silicon (Si) technology has had the advantage of the ease of formation of a good quality oxide. Hence, the most frequently used passivation material for Si is silicon oxide (SiO_2) [3]. Other materials like silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) are also used. Over the past few decades, many compound semiconductors consisting of two or more elements have been synthesized and they have gained prominence due to their superior light receiving/emitting function, generation of microwaves, magnetic sensitivity and heat resistance. As researchers started exploring such compound semiconductors like gallium arsenide (GaAs), indium phosphide (InP), cadmium telluride (CdTe), mercury cadmium telluride (HgCdTe), etc., the need for investigating other materials for passivation arose. Since then, several wide bandgap semiconductors have gained prominence as effective passivation materials [4-6].

This research investigates the passivation capabilities of thee different wide bandgap II-VI semiconductor compounds. The deposition techniques used are metalorganic CVD (MOCVD) and also atomic layer deposition (ALD). Two of the semiconductors, namely, CdTe and cadmium sulfide (CdS), have been studied for surface passivation of HgCdTe photovoltaic IR detectors. A good passivation layer helps greatly in improving the device performance, as HgCdTe surface is extremely sensitive. It reduces recombination-generation centers as well as interface trap charges. This in turn increases the overall minority carrier lifetime and reduces the leakage current of the device. Nemirovsky and Bahir have extensively studied the dependence of device performance on surface passivation [7]. Since, HgCdTe is a narrow bandgap material, even a surface potential of ~100 meV can accumulate, deplete or invert the surface. Surface passivation helps in maintaining a near flat band condition at the surface, which reduces the overall dark current as well as tunneling current caused by accumulated or inverted surfaces [8]. Surface passivation has been proven to improve the thermal and chemical stability of the device as well. It protects the underlying HgCdTe from the high temperature post-processing steps. CdTe is the most widely used surface passivant for HgCdTe due to several factors. CdTe is nearly lattice-matched with HgCdTe, which helps reduce the number of dangling bonds significantly [8, 9]. Since it is a higher bandgap material than HgCdTe, it acts as a good minority carrier reflector, which in turn increases the effective minority carrier lifetime. But, the growth temperature of CdTe is above 350°C [10-13]. Exposing HgCdTe substrates to higher temperature might lead to the depletion of Hg from the surface as Hg is very weakly-bonded in the lattice. This work depicts the development of a novel experimental set-up to deposit CdTe at temperatures as low as 135°C.

The deposition of CdS using MOCVD and ALD has been studied as an alternative to CdTe. CdS has drawn attention as a passivant for HgCdTe due to its higher mechanical and dielectric strength over CdTe [14]. It is also quite insensitive to the atmosphere. Over the years, passivation of HgCdTe using anodic sulfidation has been studied [7, 14-16]. Though anodic sulfidation is a very convenient technique, it suffers from the drawback that the stoichiometric composition of the deposited CdS films is not preserved and there are traces of Hg [15]. Hence, MOCVD or ALD are preferred for deposition of CdS passivation layers as the stoichiometry of the deposited films can be controlled precisely. Another major advantage of depositing CdS passivation films

using these techniques is that Cd precursors readily react with hydrogen sulfide (H_2S) at room temperature to produce CdS.

The third compound semiconductor that has been explored is zinc telluride (ZnTe). It has been used as an active layer in a novel double heterostructure Si solar cell, along with providing surface passivation to the absorbing layer of Si. This design has been motivated by Si hetero-junction with intrinsic thin layer (HIT) solar cell developed by Sanyo. The first reported HIT solar cell had an efficiency of 18% [17] and since then over the last two decades, the efficiency has improved to 25.6%, with a 50% reduction in Si wafer thickness [18*]. A HIT solar cell utilizes a heterostructure between thin c-Si wafers (<100 μm) and very thin amorphous Si (a-Si) layers (~10 nm) [19]. The band-gap of a-Si is around 1.7 eV at 300 K, whereas that of c-Si is 1.12 eV. Due to the band offset, both hetero-interfaces act as minority carrier reflectors, which can reduce the recombination of minority carriers. Most of the volume of the HIT solar cell is essentially c-Si wafer. Since no high temperature processes like diffusion, oxidation, etc. are involved, HIT solar cells can be processed at a very low temperature of around 200^{o}C, which reduces the cost of solar modules. The alternate model proposed by Dr. Zhang of Arizona State University includes two II-VI semiconductor layers (n-type zinc selenide, ZnSe or zinc sulfide, ZnS and p-type ZnTe) on both sides of a thin c-Si wafer to form a double-heterostructure to replace the top and bottom multilayer structures (TCO/doped a-Si/intrinsic a-Si) of the HIT solar cell. The main motivation behind this alternate approach is cost-driven. The replacement of the TCO (like indium tin oxide – ITO) layers with II-VI materials reduces the cost of production. Besides, the optical loss in the a-Si layers is reduced as the II-VI layers have wider bandgaps. Amorphous Si is subjected to light-induced degradation after hydrogen passivation (a-Si:H), which reduces the cell conversion efficiency over the years [20]. The use of II-VI materials assures a long-term stability and overcomes the problem of cell degradation.

EXPERIMENTAL DETAILS

CdTe deposition using MOCVD

A horizontal, hot-wall MOCVD reactor has been custom-designed to deposit CdTe at temperatures as low as 135°C [21]. The reactor is operated at sub-atmospheric pressures (below 10 Torr). Dimethylcadmium (DMCd) and diisopropyltelluride (DIPTe) were used as the metalorganic sources for Cd and Te, respectively. A H_2 purifier set to 375˚C is used to provide ultra-high-purity (UHP) H_2 as the carrier gas. The hot-wall configuration consists of two clam-shell heaters. The front heater which is close to the main gas inlet is maintained at a temperature of 600˚C to help crack the metalorganic precursors as they enter the reactor chamber.

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The susceptor carrying the sample is placed near the back heater, the temperature of which is varied from 20˚C to 200˚C. Using this hot wall system, the sample temperature could be maintained between 135˚C and 170˚C, while ensuring the cracking of precursors. With the above

described set-up, good uniform films of CdTe have been obtained but there is ample scope of improvement in the rate of deposition. In order to increase the deposition rate of CdTe, a new graphite cracker cell with integrated diffusers has been designed and incorporated inside the hot wall reactor [22]. The graphite cracker cell encloses a hollow space within the two diffusers which comprise of the unit and it is placed near the front heater. Precursors carried by UHP H_2 enter the enclosed volume, and crack into elemental Cd and Te. They are then ejected though the small outlet-side holes. Figure 1(a) shows the schematic of the custom-built MOCVD reaction chamber and Fig. 1(b) shows the schematic of the same system with the incorporation of the graphite cracker cell. For optimization of the growth conditions, commercial GaAs (100) and Si (100) substrates were used due to limited availability of $Hg_{1-x}Cd_xTe$ samples. The $Hg_{1-x}Cd_xTe$ samples that were used for the experiments had an x value of 0.3. Prior to deposition, these samples were subjected to an organic cleaning in methanol, followed by etching in 0.4% Br:ethylene glycol and subsequently dilute HCl.

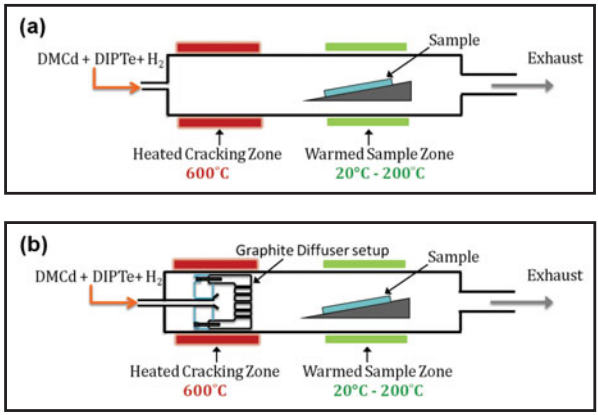

Figure 1. Schematic of the custom-built hot-wall MOCVD reactor (a) showing the heated cracking zone and the warmed sample zone, and (b) showing the incorporation of the graphite cracker cell inside the same reactor for efficient thermal cracking of precursors.

CdS deposition using MOCVD and ALD

The same hot-wall MOCVD reactor has been used to deposit CdS. It can be operated as an ALD system as well. It has a fast switching manifold design with pneumatic bellow-sealed valves for precise control of gas flow. It can deliver the ALD reactant gases to the reaction chamber separately without intermixing. The precursors carried by the carrier gas mix up in the manifold just before being injected into the horizontal reactor chamber. DMCd and hydrogen sulfide (H_2S) gas were used as the precursors for the deposition of CdS. UHP H_2 was used as the carrier gas. Commercial GaAs (100), Si (110) trench structures and glass were used as the substrates for all experiments. Si (110) wafers patterned with deep trenches of high aspect ratios were used to test for the conformal coverage of the deposited CdS films. Trench structures with

aspect ratios of 2.5 and 13 were used. MOCVD runs were carried out at room temperature, whereas ALD runs were performed at 85°C. The pressure of the reactor for all experiments was maintained at 5 Torr. The optimized DMCd and H_2S pulses were of 3 s duration each, whereas the purge durations for both were maintained at 6 s.

ZnTe deposition using MOCVD

A vertical cold-wall MOCVD reactor was used for the growth of p-type ZnTe. The susceptor having a 3" wafer holding capability is mounted on a rotating heater. Diethylzinc (DEZn) and DIPTe were used as the precursors for Zn and Te respectively. Arsenic (As) was used as the p-type dopant. Two different sources for As was used, namely, tris(dimethylamino)arsine (TDMAAs) and Arsine (AsH_3). UHP H_2 was used as the carrier gas. ZnTe was deposited on Si wafers of different orientations, Si (100), Si (111), Si (211). The reactor temperature was maintained at 450°C, the pressure of the chamber being 100 Torr. All Si samples were subjected to an organic clean followed by a dilute hydrofluoric acid (HF) etch to remove the native oxide.

RESULTS AND DISCUSSIONS

CdTe deposition using MOCVD

CdTe films deposited with and without the graphite cracker cell were compared for their rate of deposition and surface morphology using scanning electron microscopy (SEM). The incorporation of the new graphite cracker cell set up increased CdTe deposition rates highly. The advantage of this higher growth rate of CdTe passivation layer is that it shortens the total deposition time for a required thickness, which will further reduce the exposure time of the HgCdTe sample to a higher temperature. Without the cracker cell, H_2 flow of 0.6 slm was used to obtain good uniform films over an area of 3cm×3cm. The observed deposition rate at 135°C was around 40-50 nm/h. The incorporation of the new graphite cracker cell set up increased CdTe deposition rates highly. The advantage of this higher growth rate of CdTe passivation layer is that it shortens the total deposition time for a required thickness, which will further reduce the exposure time of the HgCdTe sample to a higher temperature. At a H_2 flow of 3 slm, the deposition rate increased to more than 420 nm/h at 145°C. This was a big achievement in terms of increasing the deposition rate. Figure 2(a) and (b) display SEM cross-sectional images showing the increase in deposition rate of CdTe with the implementation of the graphite cracker cell. The surface morphology of the deposited CdTe films showed grainy deposition, and the films were confirmed to be polycrystalline using x-ray diffraction.

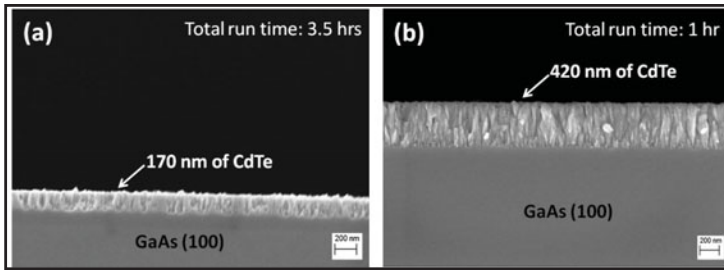

Figure 2. SEM cross-sectional images to show the thickness of CdTe films deposited (a) without the use of the graphite cracker cell at 135°C (deposition rate 50nm/h), and (b) with the implementation of graphite cracker cell at 145°C (deposition rate 420nm/h). This shows the remarkable improvement in the deposition rate of CdTe with the thermal cracking enhancement.

To test for the conformal coverage high aspect ratio, mesa-etched HgCdTe samples were used. Though not fully conformal, adequate deposition was obtained on the bottom and side walls of the mesa-etched structures on HgCdTe samples. The thickness of CdTe film deposited in 1.25 h (using H_2 flow of 3 slm) on the top of the trench structure was ~550 nm whereas the thickness on the side walls and bottom of the trench was ~380 nm. Figure 3 shows the conformal coverage obtained on a mesa-etched HgCdTe sample.

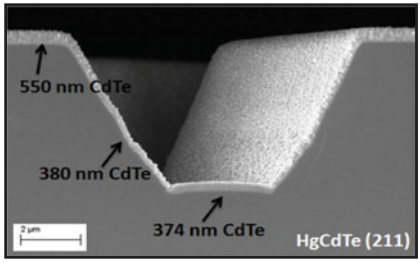

Figure 3. SEM cross-sectional image showing favorable conformal coverage of CdTe obtained on HgCdTe mesa-etched diode structures.

Focussed ion beam (FIB) imaging was used to image the interface between CdTe and HgCdTe. The interface between the two layers, as well as the surface of CdTe layer looks quite uniform and smooth, as seen in Fig. 4. The topmost platinum (Pt) layer has been deposited on the surface exposed to the ion beam to reduce the FIB induced surface artifacts caused by incident gallium ions (Ga+). The thickness of the Pt layer is around 1 μm. The image shows the presence of some pinholes which is a characteristic problem of CdTe. This problem is not seen in CdS.

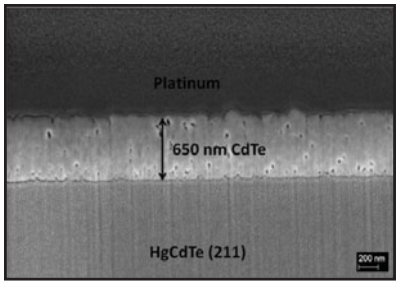

Figure 4. SEM cross-sectional image showing favorable conformal coverage of CdTe obtained on HgCdTe mesa-etched diode structures.

Another very important characterization technique used was microwave photoconductive decay measurement to measure the minority carrier lifetime of the passivated HgCdTe substrates. A custom-built MPCD lifetime measurement system was used for this purpose [23]. MPCD measurement technique is based on the principle that the semiconductor sample conductivity is directly proportional to the microwave reflection. A microwave signal at 35 GHz is incident on the semiconductor sample and gets reflected from the metal plate lying underneath the sample. A GaAs laser emitting at 890 nm, with pulse duration of 150 ns shines upon the semiconductor sample. This increases the conductivity of the sample, which in turn increases the microwave reflectivity. Once the excess carriers recombine the reflectivity signal decays down to the original value. This photoconductive decay is recorded by an oscilloscope and is used to extract the minority carrier lifetimes. Minority carrier lifetime improvements were obtained on samples passivated with CdTe deposited with and without the graphite cracker cell. There was a significant improvement in lifetime on the HgCdTe sample passivated with CdTe at 135˚C without implementation of graphite cracker cell. The lifetime increased from 0.9 μs (sample without passivation) to 4.28 μs (for sample passivated at 135˚C). Though at an elevated temperature of 170˚C there was hardly any improvement in lifetime. This could be due to the depletion of mercury from the surface. With the use of the thermal cracking enhancer graphite cell, there was a noticeable improvement in lifetime at 145˚C. An additional annealing step at 250˚C for 20 mins in the presence of H_2 further improved the minority carrier lifetime. Figure 5 demonstrates the photoconductive decay measurements conducted on HgCdTe samples passivated with CdTe. Table I summarizes the extracted lifetime obtained from the displayed photoconductive slopes.

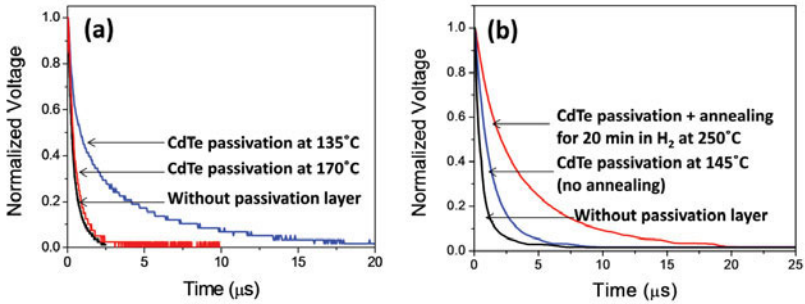

Figure 5. Photoconductive decay measurements using MPCD system on HgCdTe samples passivated with CdTe (a) without the graphite cracker cell at 135°C, and (b) using the graphite cracker cell at 145°C.

Table I. Minority carrier lifetimes on HgCdTe samples passivated with CdTe, extracted from the photoconductive decay slopes.

Sample Description	Lifetime (μs)
HgCdTe substrate without passivation layer in Fig. 5 (a)	0.92
HgCdTe substrate passivated with CdTe at **170˚C**	1.07
HgCdTe substrate passivated with CdTe at **135˚C**	4.28
HgCdTe substrate without passivation layer in Fig. 5 (b)	2.8
HgCdTe substrate passivated with CdTe at **145˚C** using graphite cracker cell	3.9
Above sample annealed at **250˚C** for 20 mins in the presence of H_2	9.1

CdS Deposition using MOCVD and ALD

CdS films deposited using MOCVD and ALD have been characterized for deposition rates, surface morphology and conformal coverage using SEM. 1 h ALD deposition at 85°C resulted in a film thickness of around 70 nm. This implies that the deposition rate was almost one monolayer per cycle. CdS films deposited using MOCVD had a much higher deposition rate of ~280 nm/h at room temperature. The surface morphology of deposited CdS films revealed grainy surfaces. The grain sizes of the ALD films were comparatively smaller than those of the CVD-deposited films. The films deposited were very uniform. Film thickness varied by ~10 nm across a sample area of 2cm×2cm for CVD deposition. Films deposited using ALD were more uniform with a minor variation of less than 5nm over an area of 2cm×2cm. Conformal coverage obtained on Si trench structures by ALD and CVD were comparable. The uniformity of the deposited CdS films as well as the conformal coverage can be seen in Fig. 6.

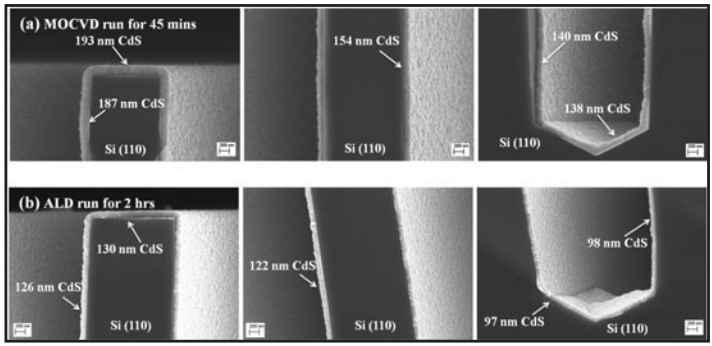

Figure 6. CdS films deposited on Si (110) trench structures showing excellent conformal coverage using (a) MOCVD for 45 mins at room temperature (~71%), and (b) ALD for 2 h at 85°C (~75%).

CdS films deposited by ALD and CVD on glass substrates were used for measuring the current vs. voltage characteristics. The glass substrate was scribed with a diamond scriber to form isolated devices of different lengths. Six devices were isolated on two glass samples – one with CdS film deposited using MOCVD and the other using ALD. Indium pieces were used to form ohmic contacts on two opposite edges of each device. The thickness of ALD-deposited CdS film was 175 nm, and that of the CVD-deposited film was 280 nm. All three devices on the sample having CdS deposited on glass substrate using MOCVD with different lengths and areas gave consistent results for resistivity measurements. The resistivity measured was around 200 Ω-cm, whereas, the resistivity measured on the devices on ALD-deposited CdS films was two orders higher - ~3×10^4 Ω-cm. Hence, ALD-deposited CdS films showed much better passivating quality. Figure 7 presents the I-V curve measured on two samples having CdS deposition using ALD and CVD.

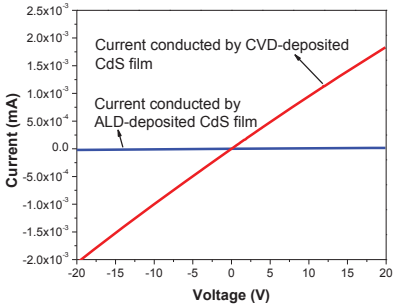

Figure 7. I-V characteristics obtained on ALD and CVD deposited CdS films on semi-insulating GaAs (100). Resistivity measured on the CVD deposited film (~ 200 Ω-cm) is two orders lower than that of ALD deposited film (3×10^4 Ω-cm).

ZnTe deposition using MOCVD

X-ray diffraction was used to determine the crystalline quality of the grown p-ZnTe films. It was found out that ZnTe films deposited at 450°C were single-crystalline. Figure 8 (a) gives a plot of the acquired XRD spectrum, showing the different ZnTe characteristic peaks on Si (111). A phi-scan with chi set to 70.5° ({111} planes are 70.5° inclined to the wafer surface) was done and no twinning was observed. This scan is displayed in Fig. 8 (b). Hall measurements were also performed on the p-ZnTe layers to determine the carrier concentration and resistivity of the thin films. ZnTe was grown on semi-insulating GaAs (100) for this purpose. A high carrier concentration of 3×10^{8} cm^{-3} was obtained using As as the dopant. A very low resistivity of 0.33 Ω-cm was recorded. This has been reported earlier by our research team as part of a different project [24].

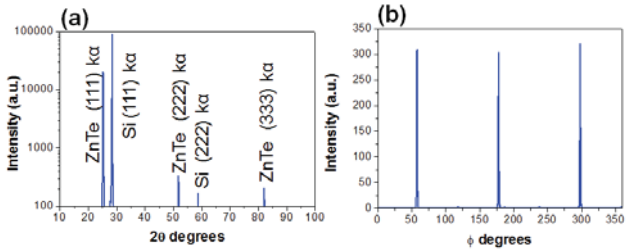

Figure 8. XRD spectrum acquired on ZnTe films grown on Si (111) wafer, showing ZnTe to be single-crystalline (a) θ-2θ scan, (b) phi scan with chi set to 70.5°.

Minority carrier lifetime measurements have been performed on Si wafers of different orientations with a thin ZnTe film grown on it. It has been observed that minority carrier lifetime of Si showed significant improvement after the growth of ZnTe thin film, hence proving the potential of ZnTe as a good surface passivant. Photoconductive decay plots on Si (100), Si (111), and Si (211) wafers are displayed in Fig. 9. The minority carrier lifetimes have been extracted from the decay plots and summarized in Table II.

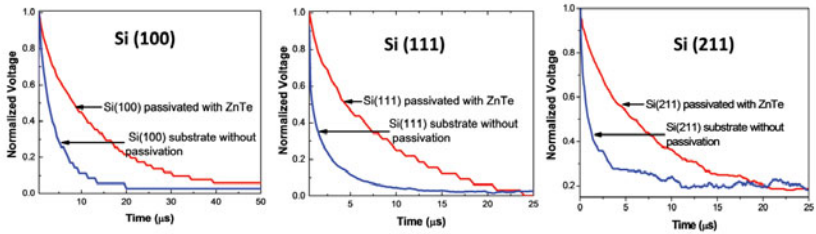

Figure 9. Photoconductive decay measurements on Si substrates having different orientations, and passivated with p-type ZnTe.

Table II. Extracted minority carrier lifetime from the photoconductive decay plots of Si wafers passivated with ZnTe.

Sample Description	Measured Lifetime (μs)
p-Si(100) Substrate	5
p-ZnTe/p-Si(100)	16
p-Si(111) Substrate	3.33
p-ZnTe/p-Si(111)	15
p-Si(211) Substrate	1.25
p-ZnTe/p-Si(211)	12.1

CONCLUSION

In summary, significant progress has been made in the research area of passivation of HgCdTe IR detectors using CdTe. A successful MOCVD design modification has been implemented to develop a process for the deposition of CdTe at a low temperature (below 150°C). Though uniform CdTe films were obtained initially, the deposition rates were quite low (~50 nm/h). With further modification of the MOCVD system, deposition rates were increased to ~420 nm/h. Significant improvement in minority carrier lifetime of HgCdTe passivated with CdTe was observed. A comparative study of CdS deposition using MOCVD and ALD revealed that while deposition rate using MOCVD was much higher than that using ALD, ALD is the preferred method for CdS deposition owing to the higher resistivity of ALD deposited CdS films. Also, ALD results in a much more uniform film over a larger area. MOCVD growth of ZnTe conducted on several orientations of Si wafers demonstrated improvement in lifetime of the underlying Si substrate. X-ray diffraction confirmed the thin films to be single-crystalline. A very low resistive film (0.33 Ω-cm) with a high carrier concentration of 3×10^{18} cm^{-3} was obtained. In all, p-ZnTe thin films showed promising results for the fabrication of the proposed double heterostructure solar cell.

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