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Performance and Reliability of SiC Power MOSFETs

Daniel J. Lichtenwalner,[1] Brett Hull,[1] Vipindas Pala,[1] Edward Van Brunt,[1] Sei-Hyung Ryu,[1] Joe J. Sumakeris,[2] Michael J. O'Loughlin, [1] Albert A. Burk,[1] Scott T. Allen,[1] and John W. Palmour[1]
[1] Wolfspeed, a Cree Company, 3028 E. Cornwallis Rd, Research Triangle Park, NC 27709, U.S.A.
[2] Cree, Inc. 4600 Silicon Drive, Durham, NC 27703, U.S.A.

ABSTRACT

Due to the wide bandgap and other key materials properties of 4H-SiC, SiC MOSFETs offer performance advantages over competing Si-based power devices. For example, SiC can more easily be used to fabricate MOSFETs with very high voltage ratings, and with lower switching losses. Silicon carbide power MOSFET development has progressed rapidly since the market release of Cree's 1200V 4H-SiC power MOSFET in 2011. This is due to continued advancements in SiC substrate quality, epitaxial growth capabilities, and device processing. For example, high-quality epitaxial growth of thick, low-doped SiC has enabled the fabrication of SiC MOSFETs capable of blocking extremely high voltages (up to 15kV); while dopant control for thin highly-doped epitaxial layers has helped enable low on-resistance 900V SiC MOSFET production. Device design and processing improvements have resulted in lower MOSFET specific on-resistance for each successive device generation. SiC MOSFETs have been shown to have a long device lifetime, based on the results of accelerated lifetime testing, such as high-temperature reverse-bias (HTRB) stress and time-dependent dielectric breakdown (TDDB).

INTRODUCTION

Wide bandgap semiconductors have a clear advantage for power device operation, due primarily to the wider bandgap resulting in lower intrinsic carrier concentrations, and low impact ionization rates (or higher critical fields before avalanche breakdown) [1,2]. The favored polytype for power devices is 4H-SiC, as it has a wide bandgap (3.26 eV), and high electron mobility (~1000 $cm^2V^{-1}s^{-1}$) both parallel to and perpendicular to the c-axis direction [3].

However, due to the many structural polytypes formed by SiC, many years of development were required to achieve single-polytype substrates with low defect densities and good doping control, which then enabled high quality epitaxial layers [4]. Presently, high-quality substrates of 150 mm diameter are available from various suppliers, and Cree recently demonstrated the capability of producing 200 mm diameter 4H-SiC substrates, with uniform epitaxial growth capability on 200mm wafers as well [5]. Preserving the polytype control during epitaxial growth is typically accomplished using an off-axis substrate orientation (4° off-axis in the {11-20} direction) such that step-flow growth dominates [6].

The development of quality power MOSFET devices has been dependent on the 4H-SiC crystal quality. As the dominant SiC MOSFET structure is a vertical device, with current flow and electrical field vertical from top-to-bottom (Fig. 1), defects in the epitaxial drift layer have a major impact on device performance. The major SiC crystalline defects which have traditionally hampered power device performance have been micro-pipes (MPs), and basal-plane dislocations (BPDs). These have resulted in either high leakage currents causing failure under high bias (MPs), or resistance drift during bipolar operation (BPDs). Presently, MP densities have been

reduced to < 0.5 cm^{-2}, and BPD densities are similarly low in the device drift region due to careful control of the epitaxial growth conditions as described previously [4].

Aided by these material advances, in 2011 Cree announced the 1st commercial SiC MOSFET, a 1200 V rated device [7]. Since then, additional product generations, as well as 1700V and 900 V rated devices, have been released. Highlighting the good 4H-SiC epitaxial quality, Cree has demonstrated MOSFET devices with up to 15 kV rating as well [8]. In the following sections, issues related to SiC MOSFET device materials processing, device performance, and reliability will be summarized.

SiC MATERIALS ISSUES

MOSFET SiC drift layer

SiC power MOSFET design typically follows the traditional 'DMOSFET' structure [1] as shown in Fig. 1, in which the electric field is dropped vertically across the epitaxial SiC drift layer with bias applied at the drain (bottom), while the metal-oxide-semiconductor (MOS) electron channel is planar (horizontal). The planar channel is typically formed on the SiC (0001) face, termed the 'Si-face', as this face has resulted in good epitaxial growth control and forms a high quality oxide upon oxidation anneal. Other device variants, such as the trench MOSFET, will not be discussed in detail here. However, it is worth noting that for the trench structure, the MOS channel is on a different SiC face, which has implications for the MOS channel resistance and oxide quality.

Due to the superior materials properties of SiC, the drift layer providing electric field blocking can be much thinner for SiC than for Si, and the doping level can be higher, offering lower resistance [1]. A figure-of-merit (FOM) for the semiconductor drift layer in the 1-D parallel-plane case is expressed as

$$\frac{V_B^2}{R_{on,sp}} = (\mu_N \epsilon_S E_C^3)/4 \quad (1)$$

where V_B is the maximum blocking voltage, $R_{on,sp}$ is the specific on-resistance (ohm-cm^2), μ_N is the electron mobility ($cm^2V^{-1}s^{-1}$), ϵ_S is the semiconductor dielectric constant, and E_C is the critical electric field strength. Due to the higher critical field strength of SiC compared to Si for a given drift doping level, the device blocking voltage can be much higher for SiC at a given $R_{on,sp}$. This is shown in Fig. 2, displaying the 1-D limits of a Si drift layer compared to a 4H-SiC drift layer (this includes the dependence of E_C and electron mobility (μ_N) on doping). Also shown in Fig. 2 are the values obtained from fabricated Cree SiC MOSFET devices rated from 900V to 15 kV. It is clear that for a given voltage rating, the SiC device has a much lower specific resistance. For Si devices, getting the same overall resistance thus requires a much larger die size. Though it has been shown that a Si power MOSFET with a 2-D or 3-D drift structure (such as a superjunction [9]) can result in lower a $R_{on,sp}$ than the Si 1-D limit, it is still well above the value achievable with the simpler 1-D drift structure in present SiC power MOSFETs.

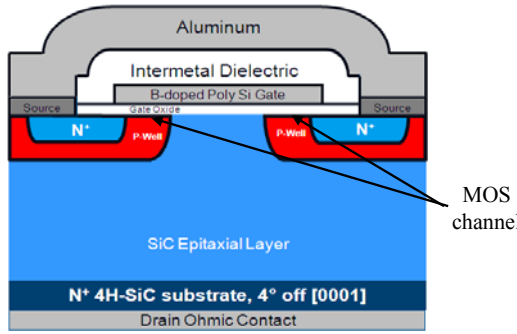

Fig. 1. Schematic cross-section of a SiC vertical DMOSFET structure. The MOS channel is planar, while the SiC epitaxial drift layer supports the vertical current (on-state) and electrical field (off-state).

MOS channel interface

Besides the drift resistance, the MOS channel resistance is another critical component of the total MOSFET on-state resistance. It is evident from the graph in Fig. 2 that the total device resistance rises above the drift limit for devices rated below about 3 kV. The channel resistance becomes a larger percentage of total device resistance as the drift layer is thinned, which is the case for lower-voltage-rated devices. From the 4H-SiC bulk mobility, it would be expected that a channel inversion layer mobility of ~200 $cm^2V^{-1}s^{-1}$ should be attainable for moderately doped channels (~1×10^{16} cm^{-3}). In the past, very high interface state density (D_{IT}) near the SiC/SiO_2 interface resulted in extremely low channel (inversion layer) mobility in 4H-SiC MOSFETs, such that the benefits of the SiC materials properties were not fully realized. However, the demonstration of the effect of nitric oxide (NO) annealing on lowering D_{IT} levels and thus raising the field-effect channel mobility (μ_{FE}) from about ~3 to 30 $cm^2V^{-1}s^{-1}$ [10] helped to make practical low-resistance MOSFET devices a reality. It has been determined that the NO (or N_2O) post-oxidation anneals result in N accumulation at the interface, which lowers the D_{IT} level of shallow e- traps, and may also result in near-surface counterdoping of the SiC. Besides N passivation, it has also been shown that oxide anneals in $POCl_3$ [11] result in high μ_{FE} values. We have recently shown that Barium at the SiC/SiO_2 MOS interface also results in high μ_{FE} values [12], greater than 80 $cm^2V^{-1}s^{-1}$. This is shown in Fig. 3, comparing the measured μ_{FE} from lateral MOSFETs fabricated on p-type (5×10^{15} cm^{-3}) SiC with a Ba interface layer compared to that of a NO treated sample. The Ba sample has double the mobility, which would result in half the channel resistance. A lower interface state density is believed to be the principal reason for this improvement, as shown by the measured D_{IT} obtained from high-low C-V measurements on n-type capacitors (Fig. 4). Although this high-low method underestimates the total D_{IT} in SiC devices [13] it has proven useful for comparing relative trap densities between samples.

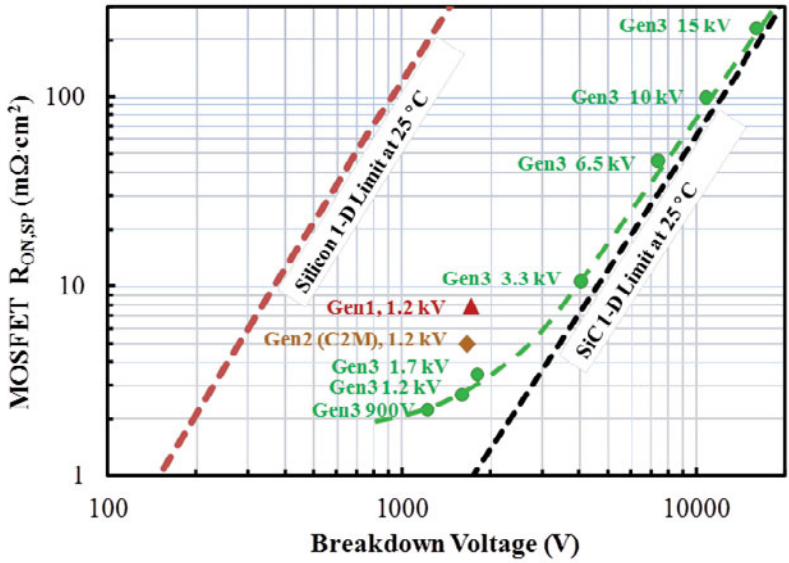

Fig. 2. Comparison of Si and 4H-SiC drift layer properties, in terms of $R_{on,sp}$ and breakdown voltage V_B. Included are points describing the performance points of Cree MOSFETs at room temperature, as reported by Palmour et al. [8].

It is also possible that other effects are present which raise the field-effect mobility, such as a high dielectric constant oxide near the interface (such as a thin barium silicate layer), or other effects which change the interface fields. For a comprehensive review of MOS-related issues in SiC, see the recent publication of Liu et al [14].

SiC MOSFET ELECTRICAL PERFORMANCE

Medium-voltage rated devices (900V to 1200V)

As there are a host of electrical power applications requiring devices with voltage ratings up to ~1700 V [1,2], and Si power device resistance increases rapidly with voltage rating, this voltage range served as a logical entry point for low-resistance SiC power devices [7].

Some key MOSFET properties are the device voltage rating, on-resistance, and threshold voltage. Normally-off (enhancement mode) devices are typically preferred, requiring a threshold voltage of a few volts to ensure the device can block current flow without bias on the gate. The device resistance determines power losses in the on-state, while the overall device structure and semiconductor material determines switching losses.

Typical on-state properties are shown in Fig. 5 for a Cree 1200V, 80 mOhm MOSFET (C2M0080120D) mounted in a TO-247 package. The device is rated to 150 °C, and the on-

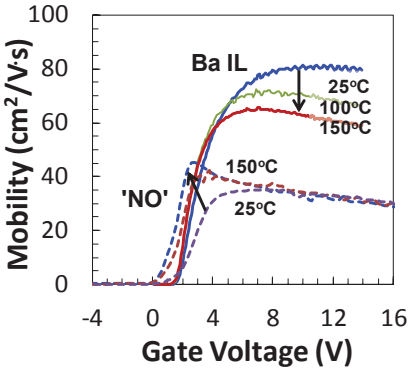

Fig. 3. Comparison of nitric oxide (NO) and Ba interface layer (Ba IL) passivation effects on 4H-SiC field-effect mobility.

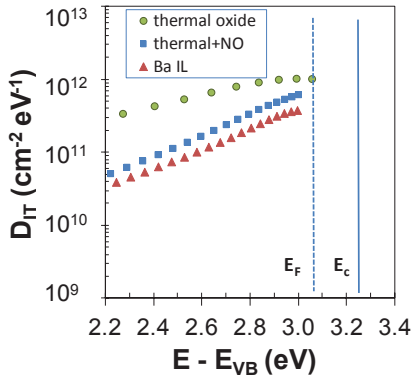

Fig. 4. Interface state density (D_{IT}) of MOS capacitors, comparing an unpassivated thermal oxide on SiC to that of N (NO) or Ba passivated samples.

state gate bias specification is 20V. Device specifications ensure a threshold voltage of >2.4V, and less than 100uA of leakage in the off-state with 1200V of drain bias at 25°C. As indicated in Fig. 6, as temperature is increased to 150 °C, the on-resistance increases 1.6 times. A slight increase in resistance with temperature helps prevent thermal runaway conditions.

An overall device operation range is compactly shown by the 'safe-operating-area' (SOA) plot in Fig.7. This clearly demonstrates the drain voltage (V_{DS}) and current (I_{DS}) limits of a given device. The drift region doping and thickness largely determines the maximum possible voltage; while the device on-resistance determines the I_{DS} current limit as V_{DS} increases from 0V to about 10V. At higher V_{DS}, the maximum current allowed eventually decreases as thermal

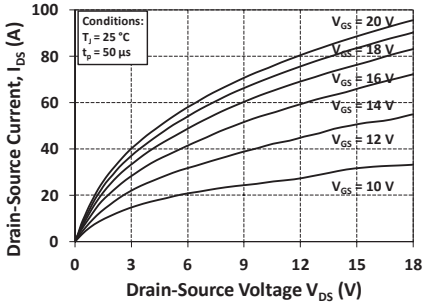

Fig. 5. Output characteristics of a Cree 1200V 80mOhm MOSFET at 25 °C.

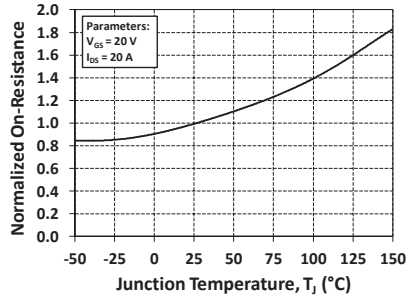

Fig. 6. Normalized on-resistance versus device temperature (1200V MOSFET).

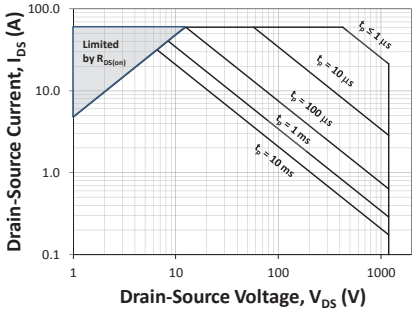

Fig. 7. Safe-operating-area graph for a Cree 1200V 80mOhm MOSFET at 25 °C.

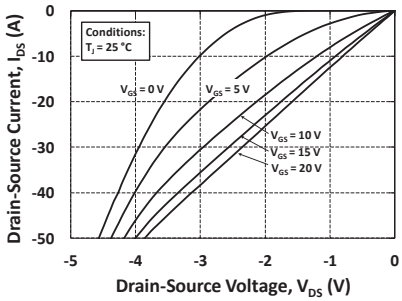

Fig. 8. 1200V MOSFET third-quadrant operation; a linear I-V with the channel on (20V_G), and the PN body-diode current with the gate off (V_G=0).

dissipation would result in heating above the rated temperature of 150 °C. The current limit is higher for short current pulses, shown ranging from 10ms to 1µs.

What is not immediately obvious from the static performance is the fact that the low specific on-resistance offered by SiC (as in Fig. 2) allows a much smaller die size for a SiC device compared to a similarly rated Si device. This is an important factor resulting in a decrease of device capacitances (between gate, source, and drain) or more relevantly gate charges (e.g., gate to drain Q_{GD}; or total gate charge Q_G(tot)), which results in large reductions in switching losses for SiC devices. This results in lower thermal cooling requirements, and allows higher frequency switching, both of which lower system costs and energy costs.

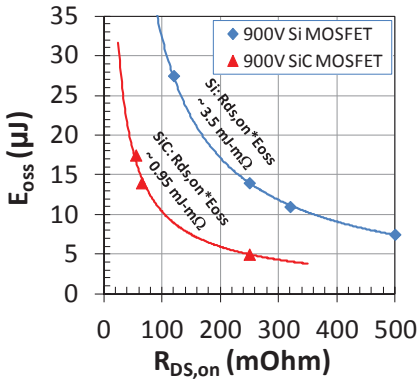

Fig. 9. A comparison of SiC and Si MOSFET efficiency, plotting the output stored energy (E_{oss}) versus the on-resistance ($R_{DS,on}$). A lower product indicates higher efficiency.

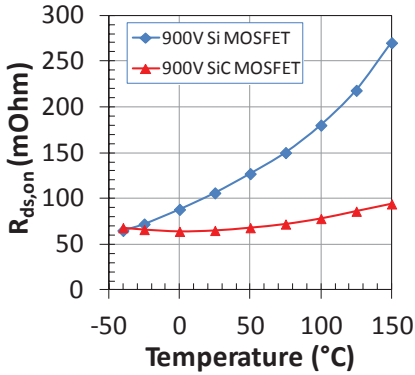

Fig. 10. A comparison of SiC and Si device resistance with temperature, up to 150 °C. The SiC device maintains a lower resistance, thus less conduction losses.

An additional feature of a MOSFET is that under negative drain bias, current can flow through the channel if the device is on ($V_G = 20V$), or through the body PN diode if the channel is off ($V_G < V_T$), shown in Fig. 8. This is important for a variety of applications; for example, a SiC MOSFET can provide the same function as an IGBT paired with an anti-parallel diode.

An example demonstrating the performance advantages of SiC MOSFETs is shown in Fig. 9, comparing Cree 900V SiC MOSFETs to Infineon 900V Si CoolMOS® MOSFETs. The output stored energy (E_{oss}, derived from the drain to source capacitive charge) is proportional to switching power losses, while the on-resistance ($R_{DS,on}$) is proportional to conduction power losses, so minimizing both parameters is key for device efficiency. It is clear that SiC MOSFETs, over a range of device on-resistance values, have much lower loss product ($R_{DS,on}$*E_{oss}) indicating lower overall power losses are possible [15].

Another performance advantage is clear when comparing the $R_{DS,on}$ as a function of temperature. As evident in Fig. 10, for relatively closely rated devices, the SiC MOSFET maintains a significantly lower $R_{DS,on}$ to 150 °C, indicating much lower conduction losses. These performance advances have allowed SiC MOSFETs to be considered as the device of choice for a range of applications, including motor drives and solar invertors, among others.

High-voltage rated devices (up to 15kV)

The materials advances in 4H-SiC epitaxial layer quality have been key to the fabrication of very high-voltage MOSFETs, from 3.3kV and higher. Because the drift layer is now the key resistive component (as evident in Fig. 2), and it must be very thick with very low doping to provide high blocking voltage, substrate and epitaxial layer quality now dominate the device performance. Using high quality 150 µm thick 4.5×10^{14} cm^{-3} N-doped epitaxial layers, we have fabricated 15kV, 10A rated SiC MOSFETs [16], demonstrating a specific on-resistance very close to the theoretical limit, as shown in Fig. 2. The output characteristics and blocking capability are shown in Figs. 11 and 12, respectively. The $R_{on,sp}$ is just above 200 mOhm-cm^2, while the devices block up to 16 kV with <1 µA leakage. While similarly rated SiC IGBTs can have a lower on-state resistance, the MOSFET becomes favored at switching frequencies above about 5 kHz, due to inherently higher switching loss in bipolar devices [16]. This high of a voltage rating has yet to be demonstrated with silicon power semiconductor devices.

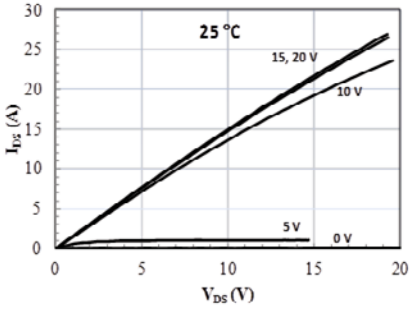

Fig. 11. On-state characteristics of a 15kV, 10A rated SiC MOSFET at 25 °C.

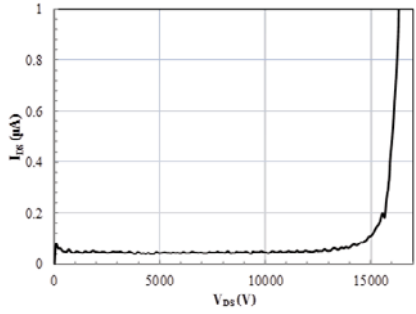

Fig. 12. Blocking capability of a 15kV, 10A rated SiC MOSFET at 25 °C.

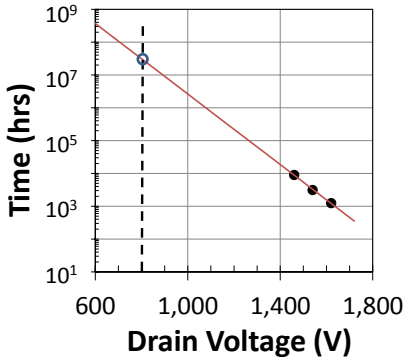

Fig. 13. Mean time to failure from accelerated HTRB testing of 1200V SiC MOSFETs at high V_{DS} stress, at 150 °C.

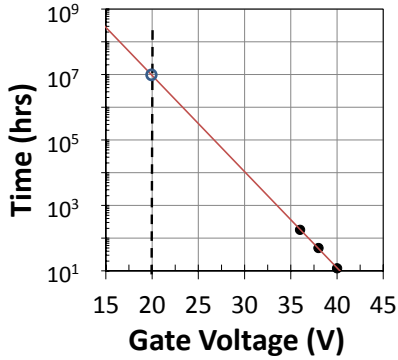

Fig. 14. Mean MOS gate failure time (TDDB) for 1200V SiC MOSFETs stressed at high V_G values, at 150 °C.

SiC MOSFET RELIABILITY

Device performance must be linked with reliability for commercially viable devices. Key tests demonstrating expected device lifetime are: 1) high temperature reverse-bias (HTRB) stress; and 2) time-dependent dielectric-breakdown (TDDB) of the MOS gate dielectric. Both of these tests can be performed under accelerated conditions (above the device operation specifications), extrapolating to device operating conditions in order to obtain long-term failure probabilities, using appropriate mathematical functions.

Results of HTRB tests on 1200V SiC MOSFETs stressed at 1460V, 1540V, or 1620V are shown in Fig. 1, showing the mean time to failure. The mean time to failure at an operating V_{DS} of 800V extrapolates to 3×10^7 hrs. TDDB test results at accelerated gate oxide fields are shown in Fig. 14. Extrapolating to the specified operational gate voltage of 20V, a mean time to failure of 1×10^7 hrs is expected. Both tests indicate mean device lifetimes of >1000 yrs under normal device operating conditions. The commercial devices are subjected to a variety of other tests for qualification purposes, beyond the scope of the present report.

CONCLUSIONS

Due to many materials and processing advances, 4H-SiC MOSFETs have become viable, high-performance power devices. Commercially available versions cover voltage ratings from 900V to 1700V, and demonstration devices covering the range from 600V up to 15kV have been fabricated and evaluated. Device reliability is rapidly improving, and devices in the 900V to 1700V ranges are being utilized for a host of power applications, due to the efficiency advantages which allow lower system costs and lower energy cost.

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REFERENCES

1. B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer Science, New York (2008).
2. T. Kimoto and J.A. Cooper, *Fundamentals of Silicon Carbide Technology*, IEEE Press, John Wiley & Sons, Singapore (2014).
3. H. Iwata and K.M. Itoh, J. Appl. Phys. **89**(11), 6228-6234 (2001).
4. J.J. Sumakeris, J.R. Jenny, and A.R. Powell, *MRS Bulletin* **30**, 280-286 (2005).
5. A.R. Powell, J.J. Sumakeris, Y. Khlebnikov, M. Paisley, R. Leonard, M. O'Loughlin, E. Deyneka, S. Gangwal, J. Ambati, V. Tsvetkov, J. Seaman, A. McClure, C. Horton, O. Kramarenko, V. Sakhalkar, J. Guo, M. Dudley, and E. Balkas, *Inter. Conf. on SiC and Related Materials (ICSCRM)* (Oct. 5, 2015).
6. H.S. Kong, H.J. Kim, J.A. Edmond, J.W. Palmour, J. Ryu, C.H. Carter, Jr., J.T. Glass, and R.F. Davis, *Mater. Res. Soc. Symp. Proc.* **97**, 233 (1987)
7. S. Davis, *Power Electronics Technol.*, pp. 36-40, Feb. (2011).
8. J. W. Palmour, L. Cheng, V. Pala, E. V. Brunt, D. J. Lichtenwalner, G.-Y. Wang, J. Richmond, M. O′Loughlin, S. Ryu, S. T. Allen, A. A. Burk, and C. Scozzie, *Proc. of the 26th Inter. Symp. on Power Semiconductor Devices & IC's (ISPSD)*, pp. 79-82, (2014).
9. CoolMOS™ C7 Technology and Design Guide, Application Note AN 2013-04, V1.0 April (2013), Infineon Technologies.
10. G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R.K. Chanana, R.A. Weller, S.T. Pantelides, L.C. Feldman, O.W. Holland, M.K. Das, J.W. Palmour, *IEEE Electron Dev. Lett.* **22**, 176-178 (2001).
11. D. Okamoto, H.Yano, K.Hirata, T.Hatayama, T.Fuyuki, *IEEE Electron Dev. Lett.* **31**, 710-712 (2010).
12. D.J. Lichtenwalner, L. Cheng, S. Dhar, A. Agarwal, J.W. Palmour, *Appl. Phys. Lett.* **105**(18), 182107 (2014).
13. A. V. Penumatcha, S. Swandono, and J. A. Cooper, *IEEE Trans. on Electron Devices* **60**(3), 923-926 (2013).
14. G. Liu, B.R. Tuttle, and S. Dhar, *Appl. Phys. Rev.* **2**, 021307 (2015).
15. V. Pala, A. Barkley, B. Hull, G. Wang, S.-H. Ryu, E. Van Brunt, D.J. Lichtenwalner, J. Richmond, C. Jonas, D.C. Capell, S. Allen, J. Casady, D. Grider, J. Palmour, *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4145-4150 (2015).
16. S.-H. Ryu, C. Capell, E. Van Brunt, C. Jonas, M. O'Loughlin, J. Clayton, K. Lam, V. Pala, B. Hull, Y. Lemma, D. Lichtenwalner, Q. J. Zhang, J. Richmond, P. Butler, D. Grider, J. Casady, S. Allen, J. Palmour, M. Hinojosa, C. W. Tipton and C. Scozzie, *Semicond. Sci. Technol.* **30**, 084001 (2015).