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# Performance assessment of a triple-junction solar cell with 1.0 eV GaAsBi absorber

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## Abstract

Group III–V semiconductor multi-junction solar cells are widely used in concentrated-sun and space photovoltaic applications due to their unsurpassed power conversion efficiency and radiation hardness. To further increase the efficiency, new device architectures rely on better bandgap combinations over the mature GaInP/InGaAs/Ge technology, with Ge preferably replaced by a 1.0 eV subcell. Herein, we present a thin-film triple-junction solar cell AlGaAs/GaAs/GaAsBi with 1.0 eV dilute bismide. A compositionally step-graded InGaAs buffer layer is used to integrate high crystalline quality GaAsBi absorber. The solar cells, grown by molecular-beam epitaxy, achieve 19.1% efficiency at AM1.5G spectrum, 2.51 V open-circuit voltage, and 9.86 mA/cm$^2$ short-circuit current density. Device analysis identifies several routes to significantly improve the performance of the GaAsBi subcell and of the overall solar cell. This study is the first to report on multi-junctions incorporating GaAsBi and is an addition to the research on the use of bismuth-containing III–V alloys in photonic device applications.

**Keywords** Multi-junction solar cells · III–V photovoltaics · GaAsBi · Molecular beam epitaxy

## Introduction

Space and terrestrial concentrated-sun photovoltaics are the primary applications of multi-junction (MJ) solar cells [1, 2]. In both operating conditions, the highest achievable efficiency is determined by bandgap combinations of its constituent subcells. However, in practice, the efficiency of MJ devices is also determined by their materials aspect. Given the scalability and stringent application requirements, any new MJ architecture must prove itself against the mature GaInP/InGaAs/Ge triple-junction (3 J) technology [3].

Emerging multi-junction solar cells hold the promise of achieving higher efficiency than the current commercial 3 J Ge-based cells, which currently achieve 30% under the AM0 spectrum. The most common approach is to retain the top two high-quality lattice-matched subcells, namely the GaInP (1.8–1.9 eV bandgap) and the InGaAs (1.35–1.41 eV) subcells, while increasing the bandgap of the bottom subcell to 0.9–1.0 eV [4]. To date, the best performance for the

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bottom subcell has been demonstrated by the InGaAs alloy [3–7]. Several versions of such 3 J solar cells have been proposed, with the best achieving 39.5% efficiency under one-sun AM1.5G and 34.2% under AM0 space spectra [8]. The design of 3 J devices that incorporate bottom InGaAs subcell relies on a several micrometres thick buffer layer and an inverted metamorphic (IMM) epitaxy to accommodate an almost 2% lattice mismatch [5, 9, 10]. Dilute nitrogen-based alloys, such as GaInNAs and GaInNAsSb, have also shown potential for use in 3 J and 4 J devices because they allow for bandgap variation in the 0.7–1.4 eV range while maintaining the desired lattice constant [11, 12]. A triple-junction cell incorporating GaInNAsSb has demonstrated an efficiency of 44.4% at a concentrated-sun AM1.5G spectrum. However, despite their potential, nitrogen-based alloys have not gained wider adoption in photovoltaics yet due to voltage-limiting factors that require further attention.

Dilute bismide $GaAs_{1-x}Bi_x$ is similar to dilute nitrides in that both demonstrate large bandgap reduction at low isoelectronic dopant concentrations. With GaAsBi, the bandgap reduction of as much as 80–90 meV/Bi% can be achieved, and at 1.0 eV bandgap, its lattice mismatch with GaAs is only 0.6% [13, 14]. Incorporation of Bi mainly perturbs the valence band, unlike dilute nitrogen alloys in which the conduction band is affected more. This difference offers alternative electronic band engineering methods in photovoltaics. Furthermore, much thinner and less complicated buffer layer is needed to incorporate 1.0 eV GaAsBi in an MJ device, as compared to InGaAs, due to a smaller lattice mismatch [15]. However, unlike dilute nitrogen alloys, the growth mechanisms and materials properties of GaAsBi alloy are less explored. For example, only recently it was shown that typical dilute GaAsBi layers grown on (001) GaAs possess pronounced optical anisotropy associated with the ubiquitous $CuPt_B$-type ordering [16–18]. Little work has been done on growing high crystal quality thick GaAsBi layers that are needed in solar cell applications [19–21]. This is likely due to the metastability of GaAsBi, which requires temperatures below 400 °C and fine-tuning of III/V elemental ratios to incorporate Bi into GaAs lattice [13, 22]. Recent works on molecular-beam epitaxy (MBE) growth of GaAsBi on lattice-matched InGaAs buffers suggest that crystal quality and Bi solubility can be enhanced [15, 23–25]. In our recent study, the growth and analysis of GaAsBi/InGaAs heterojunction 1.0 eV solar cells was reported, where we improved on the previous GaAsBi photovoltaic results [26]. Nevertheless, there have been limited reports so far on the use of GaAsBi in solar cell applications. Studies have mainly focused on the material properties or use of bismide as a single-junction absorber.

This work is the extension of the GaAsBi material applications into multi-junction solar cells. We present an MBE-grown thin-film triple-junction AlGaAs/GaAs/GaAsBi solar cell with a 1.87/1.42/1.00 eV bandgap combination. The performance of the solar cells was evaluated through current–voltage measurements under AM1.5G illumination, external quantum efficiency measurements, and device modelling.

## Experimental methods

The multi-junction solar cell was grown in a Veeco GENxplor MBE chamber equipped with solid-state sources. A valved cracker was used for the As source. Doping was performed with Be, Si, and Te. The latter was switched on only at the tunnel junction regions to supplement Si doping. The cell was grown on a quarter of a 2″ semi-insulating (001) GaAs epi-ready substrate (Wafertech, Ltd). The substrate temperature was controlled by a thermocouple and monitored with a kSA BandIt broadband pyrometry module. The outgassing and oxide removal from the substrate were performed at standard temperatures. The layers were grown at 0.6–0.7 μm/h, except the tunnel junctions, which were grown at 0.1 μm/h speed. The growth temperature of all layers up to the step-graded InGaAs buffer was 580 °C. The InGaAs buffer was deposited at 500 °C. The InGaAs buffer and GaAsBi layer were grown using optimized parameters described elsewhere in [15]. The back contact InGaAs layers were deposited at 430 °C.

A thin-film triple-junction solar cell was obtained by GaAs substrate etching. The etching procedure, including back surface metallization with metal contacts, electrochemical deposition of a 20-μm-thick Cu, and securing the cell to a polyimide sheet, is described elsewhere in [10].

The top contact was formed using standard photolithography procedures. The metal lift-off procedure was carried out in acetone at room temperature. Trenches between the active areas and edges of the sample were etched with a mixture of phosphoric acid and hydrogen peroxide. AZ1518 (MicroChemicals) photoresist was employed as a protective coating layer for the active area during etching.

Veeco Savannah S200 atomic layer deposition (ALD) reactor, equipped with a capacitively coupled plasma generator, was used to deposit antireflective coating $TiO_2/SiO_2$ (58.3/114.0 nm) at 60 ℃ substrate temperature. Before the deposition, the GaAs contact layer was etched down to the AlGaAs window layer using a selective etching solution $NH_4OH$ (28%): $H_2O_2$ (35%): $H_2O = (1:4:20)$. The samples were then immediately placed in a vacuum desiccator. The ARC was deposited

using tetrakis(dimethylamino)titanium and tris(dimethylamino)silane as precursors using oxygen plasma as an oxygen source.

The *J–V* characteristics were measured at room temperature on a Keithley 4200-SCS (Tektronix) semiconductor parameter analyser. A fully reflective solar simulator SS1.6 K (ScienceTech) was used to illuminate samples with AM1.5G spectral light. High-voltage Xenon lamp was used as a light source. External quantum efficiency (EQE) measurements were performed with a Bentham PVE300 spectrometer. Wavelength was varied from 300 to 1400 nm with a step size of 5 nm, and the mixture of halogen and xenon lamps was used as a light source with the monochromator. An additional halogen lamp was used for light bias with the following filters from Schott: RG630 (for the top junction), BG23 (for the middle junction), and KG1 (for the middle junction). For the middle and bottom junctions, an infrared mirror was placed next to the other filters. A voltage bias was set when measuring the bottom cell, as described in [27].

Calculation of the solar cell's band edge diagram was performed with the Silvaco TCAD software suite. Materials parameters for the GaAsBi/InGaAs subcell used in the simulation are described elsewhere in [26].

Structural and elemental analysis of the multi-layered structure was carried out using a cold-field-emission aberration-corrected scanning transmission electron microscope (STEM) JEM-ARM 200cF (JEOL) operated at 200 kV, equipped with a 100 mm$^2$ silicon drift-detector JED-2300 (JEOL) for energy-dispersive spectroscopy imaging (EDS). For STEM imaging, the microscope's parameters were set as follows: probe convergence semi-angle of 22 mrad; high-angle annular dark-field (HAADF) detector's inner and outer semi-angles of 68 and 280 mrad, respectively; low-angle annular dark-field (LAADF) detector's inner and outer semi-angles of 30 and 120 mrad, respectively; and bright-field (BF) detector's outer semi-angles of 34 mrad. High-resolution phase-contrast TEM imaging was carried out using FEI Tecnai G2 F20 X-TWIN operated at 200 kV accelerating voltage. Cross-sectional samples were prepared in a focused ion beam (FIB) FEI Helios Nanolab 650 microscope using the lift-off technique.

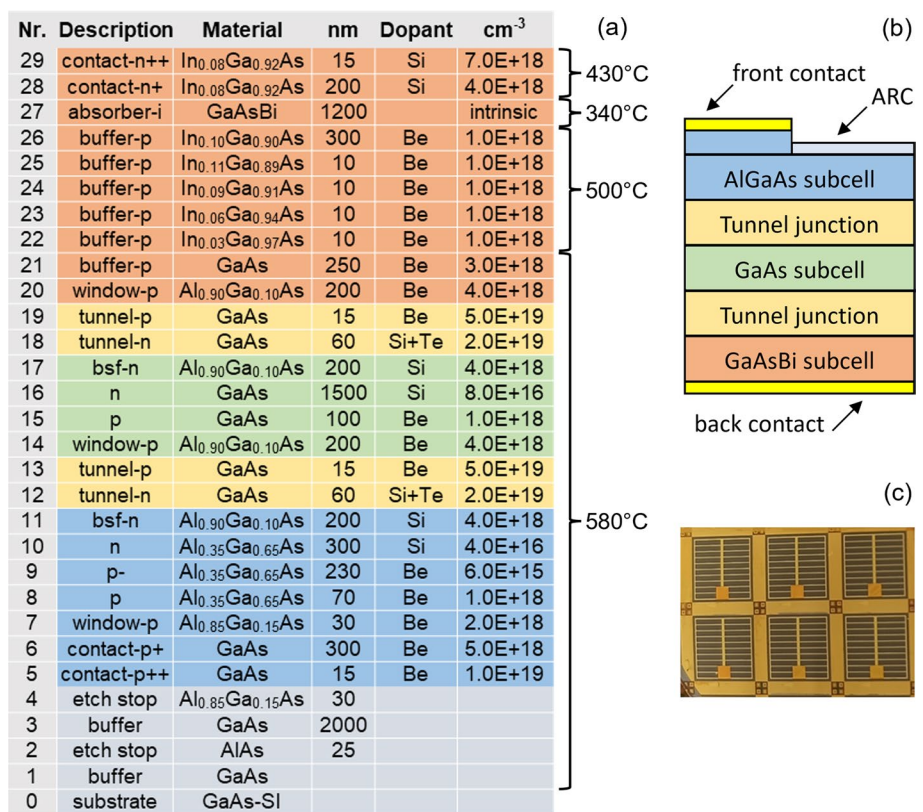## Results and discussion

### Device structure

The triple-junction solar cell featuring a GaAsBi absorber layer is depicted in Fig. 1a, b. The solar cell is grown inverted on a semi-insulating GaAs substrate starting from the top highest bandgap $Al_{0.35}Ga_{0.65}As$ subcell, followed by the GaAs middle subcell, and finally, the GaAsBi-based bottom subcell. After growth, a back contact of AuGe/Ni/Au is deposited, followed by electrochemical copper deposition and attachment of the structure to a Kapton polyimide. The substrate is then removed by etching [10]. Layers 2–4 (see Fig. 1a) are employed to assist with the substrate etching steps and further device processing. Standard photolithography steps are carried out to form top contacts. A thin-film 3 J solar cell, obtained through the aforementioned process, is illustrated in Fig. 1b, while Fig. 1c shows a photograph of a completed device with several mesa cells.

The decision to use the inverted growth method was primarily driven by two factors. Firstly, the instability of the GaAsBi alloy above around 450 °C leads to the ejection of Bi from the lattice and formation of Bi droplets [13, 28]. The higher substrate temperatures required to grow the AlGaAs and GaAs subcells (580 °C, see Fig. 1a) with good crystal quality would damage the GaAsBi subcell, making it necessary to grow the bismide layer last. Secondly, an InGaAs buffer layer was utilized to increase the lattice constant to match that of the bismide. The $Al_xGa_{1-x}As$ alloy is almost exactly lattice-matched with GaAs for all *x*, for the practical purposes at hand. Therefore, by growing the top two subcells first, the likelihood of their crystal structure being compromised by dislocations generated in the InGaAs buffer layer is significantly reduced. We acknowledge that alternative material choices for the graded buffer layer, instead of InGaAs, could be used [5, 7, 8]. In fact, using a buffer layer material with a larger bandgap, such as GaInP, GaAsP, or AlInGaAs, would be advantageous in reducing parasitic absorption. In this case, InGaAs was chosen due to the availability of sources and a preference for its lower growth temperature to maintain the stability of the tunnel diodes.

The *p*-on-*n* device polarity, utilized in this 3 J device, was largely determined by the Be dopant diffusion properties in the tunnel diodes. Previous studies, along with our secondary-ion mass spectroscopy studies (not shown here), have demonstrated that Be diffuses towards the growth surface, making it challenging to maintain high doping density (on the order of $10^{19}$ cm$^{-3}$) in a thin region [29, 30]. Furthermore, the diffused Be may also compensate the *n*-type doped tunnel diode region if the *p*-type tunnel portion is grown first. We found that using an *n*-on-*p* tunnel diode polarity, coupled with 200-nm-thick $Al_{0.90}Ga_{0.10}As$ barrier layers encompassing the tunnel diodes, allows for retaining their stability and peak tunnelling current densities 20–30 mA/cm$^2$ under prolonged annealing times experienced by the tunnel diode

**Fig. 1** **a** Layer structure of the triple-junction solar cell grown on SI-GaAs substrate. It shows used alloys and their description, layer thicknesses (nm), dopant atoms, and carrier concentrations (cm$^{-3}$). BSF abbreviates back surface field. Substrate temperatures (as measured by BandIt pyrometer) at which the growth of different parts of the solar cell was performed are shown on the right. **b** Depiction of a completed solar cell with removed GaAs substrate. **c** Photograph of completed solar cell mesa structures with ARC and contact grids. The active area of each mesa solar cell, considering grid shading, measures to 0.2 cm$^2$

| Nr. | Description | Material | nm | Dopant | cm$^{-3}$ |
|-----|-------------|----------|-----|--------|-----------|
| 29 | contact-n++ | In$_{0.08}$Ga$_{0.92}$As | 15 | Si | 7.0E+18 |
| 28 | contact-n+ | In$_{0.08}$Ga$_{0.92}$As | 200 | Si | 4.0E+18 |
| 27 | absorber-i | GaAsBi | 1200 | | intrinsic |
| 26 | buffer-p | In$_{0.10}$Ga$_{0.90}$As | 300 | Be | 1.0E+18 |
| 25 | buffer-p | In$_{0.11}$Ga$_{0.89}$As | 10 | Be | 1.0E+18 |
| 24 | buffer-p | In$_{0.09}$Ga$_{0.91}$As | 10 | Be | 1.0E+18 |
| 23 | buffer-p | In$_{0.06}$Ga$_{0.94}$As | 10 | Be | 1.0E+18 |
| 22 | buffer-p | In$_{0.03}$Ga$_{0.97}$As | 10 | Be | 1.0E+18 |
| 21 | buffer-p | GaAs | 250 | Be | 3.0E+18 |
| 20 | window-p | Al$_{0.90}$Ga$_{0.10}$As | 200 | Be | 4.0E+18 |
| 19 | tunnel-p | GaAs | 15 | Be | 5.0E+19 |
| 18 | tunnel-n | GaAs | 60 | Si+Te | 2.0E+19 |
| 17 | bsf-n | Al$_{0.90}$Ga$_{0.10}$As | 200 | Si | 4.0E+18 |
| 16 | n | GaAs | 1500 | Si | 8.0E+16 |
| 15 | p | GaAs | 100 | Be | 1.0E+18 |
| 14 | window-p | Al$_{0.90}$Ga$_{0.10}$As | 200 | Be | 4.0E+18 |
| 13 | tunnel-p | GaAs | 15 | Be | 5.0E+19 |
| 12 | tunnel-n | GaAs | 60 | Si+Te | 2.0E+19 |
| 11 | bsf-n | Al$_{0.90}$Ga$_{0.10}$As | 200 | Si | 4.0E+18 |
| 10 | n | Al$_{0.35}$Ga$_{0.65}$As | 300 | Si | 4.0E+16 |
| 9 | p- | Al$_{0.35}$Ga$_{0.65}$As | 230 | Be | 6.0E+15 |
| 8 | p | Al$_{0.35}$Ga$_{0.65}$As | 70 | Be | 1.0E+18 |
| 7 | window-p | Al$_{0.85}$Ga$_{0.15}$As | 30 | Be | 2.0E+18 |
| 6 | contact-p+ | GaAs | 300 | Be | 5.0E+18 |
| 5 | contact-p++ | GaAs | 15 | Be | 1.0E+19 |
| 4 | etch stop | Al$_{0.85}$Ga$_{0.15}$As | 30 | | |
| 3 | buffer | GaAs | 2000 | | |
| 2 | etch stop | AlAs | 25 | | |
| 1 | buffer | GaAs | | | |
| 0 | substrate | GaAs-SI | | | |

(a) 430°C / 340°C / 500°C / 580°C

(b) front contact — ARC — AlGaAs subcell — Tunnel junction — GaAs subcell — Tunnel junction — GaAsBi subcell — back contact

(c)

during the full device growth period [31]. For the *n*-type tunnel diode regions, we employed a co-doping of Si with Te to enhance dopant stability and raise carrier density to $2 \times 10^{19}$ cm$^{-3}$.

Studies have shown that an intrinsic 1.0 eV GaAsBi (~ 5.5% Bi) is slightly *p*-type with a carrier density of $1 \times 10^{15} - 1 \times 10^{16}$ cm$^{-3}$ [32]. Although it is possible to dope GaAsBi either *p*- or *n*-type, which could potentially improve the subcell's $V_{oc}$, there is a risk that already low carrier lifetimes in the bismide will decrease even further [26, 33]. To stay on the safe side, we used an intrinsic GaAsBi. For the intrinsic GaAsBi subcell, the *p*-on-*n* device polarity is more favourable over the *n*-on-*p* because it provides an electric field at the back of the absorber, which enhances photogenerated carrier extraction.

The triple-junction solar cell was modelled using the Silvaco TCAD software suite. Figure 2 shows the diagram of the conduction and valence band edges. It should be noted that the actual band bending may differ somewhat due to dopant diffusion, particularly in the tunnel diode regions. As can be seen in Fig. 2, the electric field extends over most of the AlGaAs top subcell, which facilitates charge carrier extraction. Regarding the bismide absorber, the band bending

**Fig. 2** Conduction (cb) and valence band (vb) edges at different positions in the GaAsBi-based triple-junction solar cell. The Fermi level is at 0.0 eV, and simulation was done in thermal equilibrium conditions. The numbering indicates: 1—top window layer, 2—AlGaAs subcell, 3—first tunnel diode, 4—GaAs subcell, 5—second tunnel diode, 6—GaAs/InGaAs buffer layer, 7—GaAsBi absorber layer, 8—InGaAs back contact layer
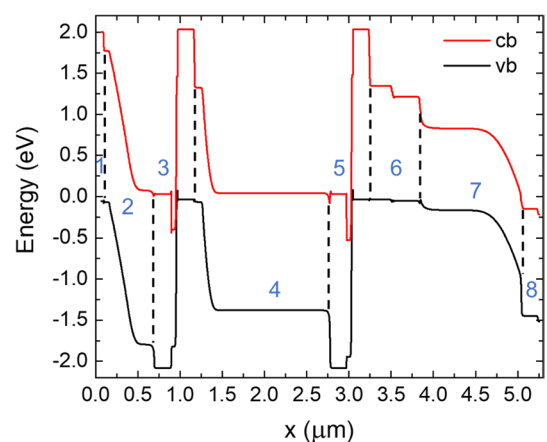
**Fig. 3** BF-STEM and EDS characterization of the cross-sectional 3 J device along [110] zone-axis. BF-STEM image shows the entire triple-junction solar cell. Subcells and different layers are labelled, including the position of the step-graded InGaAs buffer layer. The inset, overlaid on the STEM image, displays EDS elemental map of a narrow sample region
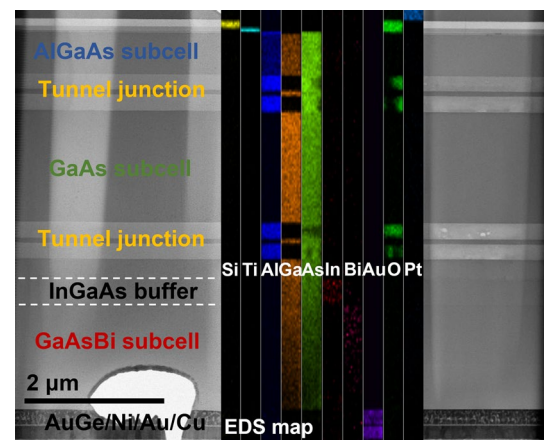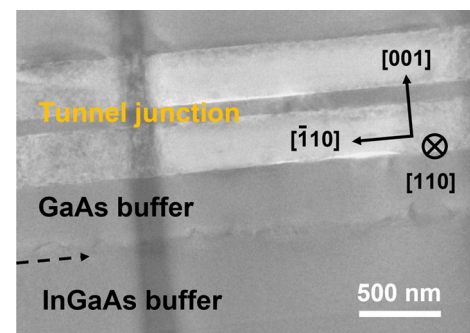


**Fig. 4** BF-TEM image of the sample near the InGaAs buffer layer. The visible corrugated contrast at the GaAs/InGaAs interface, marked with an arrow, is due to dislocations. Crystallographic directions of the sample are indicated



is situated towards the back and so quantum efficiency at longer wavelength photons should be enhanced in the *p-i-n* bismide configuration. We note that the *p*- and *n*-layers of the bismide diode are InGaAs alloys, thereby formally forming a heterojunction diode. The figure also indicates that no significant electronic barriers for charge carrier extraction should exist at the InGaAs/GaAsBi interfaces.

The materials parameters for the modelling of the bismide were adopted from our recent article on GaAsBi/InGaAs solar cells as the growth conditions for GaAsBi in the 3 J device were kept the same [26]. The simulations used 0.2 ns electron and 0.05 ns hole lifetimes, as well as 1800 cm$^2$/V s and 20 cm$^2$/V s mobilities, respectively. With these parameters, the bismide subcell limits the short-circuit current of the 3 J device and the subcells were thinned accordingly. The simulations suggest that a short-circuit current density ($J_{sc}$) of 12.2 mA/cm$^2$ can be achieved under the AM1.5G spectrum. The modelled device exhibited a $V_{oc}$ of 2.57 V, fill factor (*FF*) of 0.78, and power conversion efficiency (*η*) of 24.5%.

To investigate the structural quality of the triple-junction solar cell, cross-sectional scanning transmission electron microscopy (STEM) characterization was carried out. Figure 3 displays a bright-field (BF) STEM image of the solar cell, with an energy-dispersive spectroscopy (EDS) imaging inset. The sample surface was covered with Pt to protect it during focused ion beam (FIB) sample preparation. Below the Pt, the double ARC layer, different subcells, GaAs tunnel junctions, and back contact metals are visible. The thin tunnelling region is surrounded by 200-nm-thick visibly brighter AlGaAs layers (layers 11, 14, 17, and 20 in Fig. 1a). The exposed high Al content AlGaAs layers readily oxidize in air, and this can be seen in the EDS map. The vertical columnar-like contrast is due to TEM sample thickness variations, and the void in GaAsBi subcell is from FIB damage. The sample becomes thinner towards the back contact, which is apparent from the diminishing Ga and As EDS signals. A weak bismuth EDS signal can be seen from the dilute GaAsBi absorber layer. We note that no phase-separation or Bi droplets were detected in the 1200-nm-thick GaAsBi layer, as determined by STEM imaging. This confirms optimized growth conditions for high structural quality GaAsBi employed in these devices.

A zoomed-in BF-TEM image of the InGaAs buffer layer region (layers 22–26) is shown in Fig. 4. The corrugated contrast visible along the GaAs buffer (layer 21) and InGaAs buffer interface is attributed to the high density of dislocations. Notably, no significant dislocation contrast is visible in the GaAsBi absorber layer (Fig. 4). In our previous study, we reported an upper limit for the dislocation density, $\rho$, in the GaAsBi layer grown on a step-graded InGaAs buffer configuration, which was determined to be $\rho < 1 \times 10^8$ cm$^{-2}$ [15]. The dislocations were primarily concentrated at the GaAs/InGaAs interface

**Fig. 5** External quantum
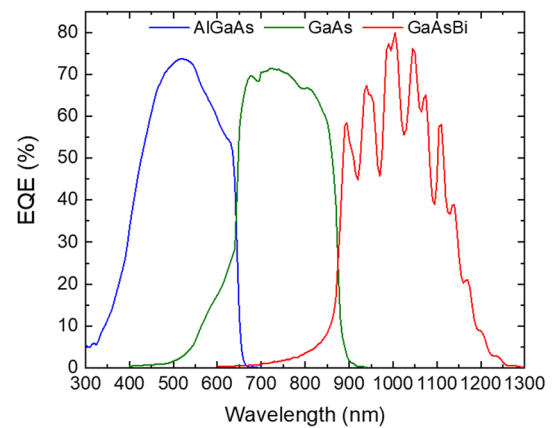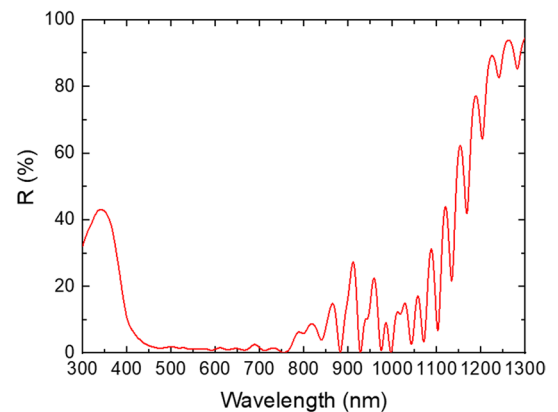efficiency of the 3-junction
solar cell



**Fig. 6** Reflectance spectrum
of the 3-junction obtained
using device simulation



and within the four 10-nm-thick InGaAs buffer layers, similar to our observations in the current device. In future studies, additional techniques such as cathodoluminescence or surface etch pit counting could be employed to further refine the assessment of dislocation density.

## Photovoltaic performance

Figure 5 shows the EQE results of a representative solar cell. The spectral response of the GaAsBi subcell extends up to 1250 nm wavelength and slightly beyond. Simulations suggest that the reflectance in the 1000–1250 nm spectral range increases from 5 to 90% (refer to Fig. 6). The tunnel diode regions, encapsulated by the $Al_{0.90}Ga_{0.10}As$ layers, strongly reflect longer wavelength photons that should otherwise reach the bottom GaAsBi subcell. The Fabry–Perot interference effects are also visible due to the reflection of light from the back metal contact and internal reflections in the solar cell. The reflection from the back contact effectively increases the optical path in GaAsBi allowing for a thinner absorber. To improve carrier extraction at the top AlGaAs subcell, graded doping levels and a reduced $n$-type AlGaAs base thickness were employed [34]. Due to thinned AlGaAs layer used for current matching and resultant incomplete absorbance, spectral overlap with GaAs subcell in the 500–650 nm region can be seen in Fig. 5.

The $J$–$V$ data of the triple-junction solar cell are presented in Fig. 7, acquired at room temperature under AM1.5G solar spectrum illumination. The inset in Fig. 7 lists the photovoltaic characteristics of the most efficient cell ($\eta = 19.1\%$, red curve) in the set. The $V_{oc}$ of the solar cells varies from 2.46 to 2.53 V, $J_{sc}$ ranges from 9.50 to 9.90 mA/cm², and FF ranges from 0.72 to 0.78. The spread in $V_{oc}$ and FF values could be attributed to several factors, including sample processing effects and spatial elemental inhomogeneities that may have occurred during growth. Our investigations show that the $V_{oc}$ of a standalone AlGaAs top cell can vary between 1.20 and 1.25 V, $V_{oc}$ of a GaAs cell—between 0.98 and 1.0 V, while a 0.99 eV bandgap GaAsBi demonstrated 0.34 V in our previous study [26]. Based on these values, we can expect the $V_{oc}$ of the triple-junction solar cell to be in the range of 2.52–2.59 V.

Next, we will discuss strategies for improving the performance of the 3 J solar cell. Firstly, it is important to note that the overall architecture of the 3 J device was partially influenced by the available sources and dopants in the

**Fig. 7** Room-temperature *J–V* characteristics of five 3-junction solar cell mesa structures obtained under AM1.5G solar spectrum. The inset values refer to the best efficiency solar cell in this sample set
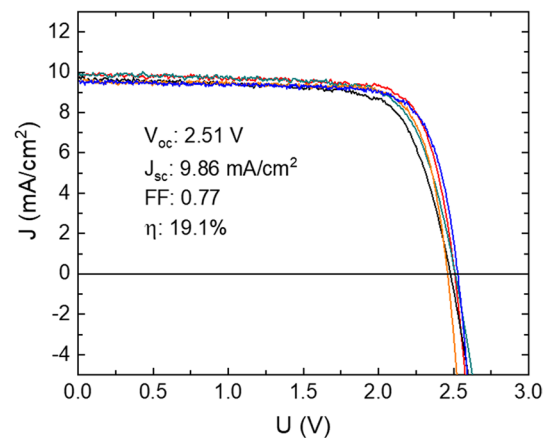


MBE system. We utilized an $Al_xGa_{1-x}As$ alloy for the top subcell, which is known to have suboptimal performance characteristics. High concentrations of Al can result in reduced carrier lifetimes and a significant bandgap-voltage offset ($W_{oc} = E_g/q - V_{oc}$), potentially attributed to the presence of oxygen-related or DX-defect centres [35, 36]. In addition, there may be a high interface recombination velocity at the AlGaAs window and back surface field layers, which can diminish the EQE of the subcells. By substituting the top AlGaAs subcell with GaInP, we anticipate an increase in $V_{oc}$ by up to 0.3 V, resulting in a 21% efficiency for the 3 J device (using the relation $\eta = V_{oc} \times J_{sc} \times FF/P$), assuming all other factors remain constant. Furthermore, reducing the thickness of the tunnel diode encapsulation layers and replacing them with phosphorus-based alloys such as AlInP, GaInP, or AlGaInP could mitigate long-wavelength reflection losses and enhance the EQE of the GaAsBi subcell. We estimate that implementing these changes alone could achieve a current-matching $J_{sc}$ of approximately 12.0 mA/cm$^2$, and utilizing the GaInP top subcell would yield an efficiency of 26%. Further efficiency improvements of up to 2 percentage points are possible by increasing the fill factor to 0.82–0.84. It is reasonable to expect that the *FF* would be improved to some extent due to the aforementioned material choices. As for the GaAs subcell, the growth of GaAs crystals is well developed and near-optimal cell performance with a $V_{oc}$ of 1.0 V can be routinely achieved.

Several approaches can be considered to improve the performance of the GaAsBi subcell in the MJ device. As mentioned previously, the reflection losses that affect EQE could be reduced through light management and alternative materials to AlGaAs. Another method to increase subcell current is to use a patterned back contact layer and a thicker GaAsBi absorber. Our previous modelling suggests that the optimal thickness is around 1400 nm [26]. Voltage offsets, $W_{oc}$, in GaAsBi are typically 0.60–0.65 V and tend to decrease with decreasing Bi concentration [19, 22]. Short charge carrier lifetimes, on the order of 0.1 ns, seem to be the primary cause of large $W_{oc}$ values in GaAsBi, which also negatively affects the $J_{sc}$ [26]. Currently, the lifetimes in GaAsBi may be influenced by dislocations, as well as Bi-related defect complexes and defects that emerge similarly in low-temperature grown GaAs [37–39]. Based on the estimated upper limit of the dislocation density in GaAsBi, $\rho < 1 \times 10^8$ cm$^{-2}$, the expected minority carrier lifetime, as reported in [37], would be approximately 0.1 ns, which aligns with our findings. Consequently, further research could focus on reducing the dislocation density in GaAsBi. It is worth noting that increasing the *p*-type carrier concentration to around $5 \times 10^{16}$ cm$^{-3}$ could enhance the $V_{oc}$ of the GaAsBi subcell by up to 0.1 V [26]. However, it is important to ensure that doping GaAsBi does not significantly compromise the diffusion length of the carriers. By implementing these optimizations, an efficiency of 30% with a GaAsBi-based triple-junction configuration appears feasible. To achieve efficiency improvements beyond 30%, it would be necessary to reduce the average $W_{oc}$ of the 3 J device, minimize optical losses, and mitigate resistance losses [2, 8, 37].

Further research on GaAsBi synthesis remains necessary, particularly focusing on deep-level point-defect control and gaining a better understanding of the nature of defects. Our findings indicate that, in addition to tuning of the III/V ratio guided by the presence of surface Bi and Ga droplet formation, stable growth temperature is a crucial factor in achieving a uniform bismide layer. Additionally, while the step-graded InGaAs buffer layer employed in our study offers one approach to incorporate GaAsBi, future research could explore alternative transparent buffer layers and methods, such as a compositionally graded GaAsBi absorber. The latter would allow for uninterrupted GaAsBi deposition, minimizing surface contamination and potentially enhancing carrier collection efficiency.

## Conclusions

In this study, we presented a thin-film triple-junction solar cell incorporating dilute GaAsBi alloy for the first time. The semiconductor alloy composition of the subcells consisted of AlGaAs/GaAs/GaAsBi with nominally 1.87/1.42/1.0 eV bandgap combination, respectively. The best solar cells exhibited a power conversion efficiency of 19.1%, an open-circuit voltage of 2.51 V, and a short-circuit current of 9.86 mA/cm$^2$ under AM1.5G illumination. To grow high-quality 1.0 eV GaAsBi, we used a 340-nm-thick InGaAs buffer layer to expand the lattice constant beyond the GaAs. The bottom subcell employed intrinsic GaAsBi and *p*-on-*n* device polarity, which enhances the extraction of charge carriers generated deeper within the bismide layer. The bismide was 1200 nm thick and took advantage of reflection from the back metal contact to increase the effective optical path. The EQE data and reflectance spectrum suggest that better light management could add 2 mA/cm$^2$ to the bismide subcell. Likewise, replacing AlGaAs top subcell with phosphorus-based GaInP would allow for achieving higher overall $V_{oc}$. We estimate that the 0.99 eV GaAsBi subcell generated approximately 0.34 V, which translates to a 0.65 V voltage offset, similar to those found in dilute nitrides. The techniques for alloy growth and incorporation of GaAsBi call for further studies to improve its photovoltaic characteristics. This study demonstrates an advanced optoelectronic device based on bismuth-containing alloys and paves the way for their application in high-efficiency solar cells.

**Data availability** The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Declarations

**Competing interests** The authors have no competing interest to disclose.

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