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Electrical Properties of Ultrathin Hf-Ti-O Higher *k* Gate Dielectric Films and Their Application in ETSOI MOSFET

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Abstract

Ultrathin Hf-Ti-O higher *k* gate dielectric films (~2.55 nm) have been prepared by atomic layer deposition. Their electrical properties and application in ETSOI (fully depleted extremely thin SOI) PMOSFETs were studied. It is found that at the Ti concentration of Ti/(Ti + Hf) ~9.4%, low equivalent gate oxide thickness (EOT) of ~0.69 nm and acceptable gate leakage current density of 0.61 A/cm^2 @ $(V_{fb} - 1)V$ could be obtained. The conduction mechanism through the gate dielectric is dominated by the F-N tunneling in the gate voltage range of −0.5 to −2 V. Under the same physical thickness and process flow, lower EOT and higher I_{on}/I_{off} ratio could be obtained while using Hf-Ti-O as gate dielectric compared with HfO_2. With Hf-Ti-O as gate dielectric, two ETSOI PMOSFETs with gate width/gate length (*W/L*) of 0.5 μm/25 nm and 3 μm/40 nm show good performances such as high I_{on}, I_{on}/I_{off} ratio in the magnitude of 10^5, and peak transconductance, as well as suitable threshold voltage (−0.3~−0.2 V). Particularly, ETSOI PMOSFETs show superior short-channel control capacity with DIBL <82 mV/*V* and subthreshold swing <70 mV/decade.

Keywords: Ultrathin Hf-Ti-O gate dielectric films, Higher k, Atomic layer deposition, Electrical properties, ETSOI MOSFET

Background

On the basis of International Technology Roadmap for Semiconductors (ITRS) 2013 [1], reduction of the equivalent gate oxide thickness (EOT) below 0.7 nm with appropriate metal gates remains as the most difficult challenge associated with the future device scaling.

Hf-based oxide high-*k* has been applied in 45- [2], 32-, 22-, and 14-nm technology nodes. An apparent way to scale EOT is to reduce the physical thickness of the Hf-based oxide. However, there is little room in this direction. One of the possible EOT scaling approaches is to introduce a new high-*k* material with *k* value greater than that of HfO_2 [3, 4], particularly higher *k* ($k > 30$) [1].

Considering the process compatibility of Hf-based oxide high-*k*, investigation on the electrical properties of Hf-based higher *k* gate dielectrics is of significance in extending Hf-based high-*k* to the future nodes as well as continuing CMOS scaling. One way to increase the permittivity of HfO_2 is combining it with very high-*k* materials, for instance TiO_2 with a *k* value of 50~80 due to remote phonon scattering [5, 6]. Introducing Ti into HfO_2 could tune the *k* value according to the Ti content, thus achieving desired *k* value [7, 8]. Ultrathin EOT (~8 Å) was achieved by using bi-layer sputtered TiO_2/HfO_2 dielectric with effective permittivity ~36 [9].

Recently, as the mainstream bulk devices face formidable challenges to scale beyond 20-nm node, there is an increasingly renewed interest in fully depleted devices such as FinFET and ETSOI for continued CMOS scaling [10]. ETSOI MOSFET is considered as one of the main options for continued MOSFET scaling in 22- and 16/14-nm technology nodes, owing to its superior short-channel control capacity and immunity to random dopant fluctuation [11–14].

The previous studies have rarely utilized Hf-Ti-O higher *k* in short-channel MOSFET especially ETSOI

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MOSFET to investigate the effect of Hf-Ti-O on device performances including I_{on}/I_{off} ratio (switch ratio) and short-channel effects. Investigation on the application of Hf-Ti-O higher k in ETSOI MOSFET, a new device structure will help to evaluate practicability of Hf-Ti-O in the future technology nodes and continue CMOS scaling.

In this study, in order to obtain EOT below 0.7 nm, ultrathin Hf-Ti-O higher k gate dielectric films (~2.55 nm) have been prepared by atomic layer deposition (ALD). Their electrical properties and application in short-channel ETSOI PMOSFETs were studied. For contrast, MOS capacitor and ETSOI MOSFET with HfO_2 (~2.55 nm) as high-k gate dielectric were prepared as control samples.

Methods

Preparation of the Hf-Ti-O Higher *k* and MOS Capacitors

The MOS capacitors were prepared on 8-in. p-Si (100) substrates with a resistivity of 8~12 Ω cm. Since high k/Si interface quality is critical to the EOT scaling and device performance, ~0.6-nm SiO_2 interfacial layer (IL) was intentionally grown by ozone oxidization of Si before Hf-Ti-O higher k deposition. $[(CH_3)(C_2H_5)N]_4Hf$ and $TiCl_4$ were used as the metal precursors. Deionized water was chosen as an oxygen source and N_2 (99.999%) as a carrier and purge gas. The substrate temperature was kept at 300 °C. Sixteen-cycle HfO_2/4-cycle TiO_2/16-cycle HfO_2 sandwich structure was utilized to reduce the Ti diffusion. As for the control sample, 34-cycle HfO_2 was prepared. Then, PDA (post deposition annealing) in 90% N_2/10% O_2 at 450 °C for 15 s was performed. Then, the TiN was used as the metal gate with a gate area of $100 \times 100\ \mu m^2$ and W as the capping layer. After gate patterning, backside Al was deposited for the ohmic contact and the forming gas annealing was carried out in 95% N_2/5% H_2 at 450 °C for 20 min.

Characterization of the Hf-Ti-O Higher k/IL/Si Stack and Electrical Properties

The gate stack structure was characterized by high-resolution transmission electron microscopy (HRTEM). The Hf-Ti-O film composition and interfacial reaction were investigated by XPS. High-frequency capacitance–voltage (C–V) at 1 MHz and gate leakage current density-gate voltage (J_g–V_g) measurements were performed for the MOS capacitors. The EOT and flat-band voltage (V_{fb}) were extracted by fitting the measured high frequency C–V data through a C–V simulator developed by UC Berkeley, including quantum mechanical effect.

Preparation of the ETSOI PMOSFETs

The ETSOI PMOSFETs were fabricated on 8-in. SOI wafers with a buried oxide (BOX) thickness of 145 nm by using gate last process scheme. Top Si was thinned to ~8.5 nm. Dummy polysilicon gate was formed followed by a thin spacer (~8 nm). Faced raised source and drain were in situ epi-grown with boron doped. Silicon loss in source and drain areas should be carefully controlled to form high quality SiGe. RTA (rapid thermal annealing) was performed to drive in dopants to form extensions. After silicide and interlayer dielectric (ILD) formation, dummy gate was removed. Then, the preparations of interfacial layer and Hf-Ti-O higher k films for ETSOI PMOSFETS were entirely the same as those for the capacitor. TiN was selected as PMOSFET work function metal.

Characterization of the ETSOI MOSFET Performance

The device performances were extracted from the typical transfer characteristics measurement of the drian current (I_d) versus gate voltage (V_g), where the threshold voltages (V_t) were extracted through the constant current method when I_d equals to 0.1 μA (W/L).

Results and Discussion

Characterization of the Hf-Ti-O Higher *k*/IL/Si Stack

Figure 1 shows the high-resolution cross-section TEM image of Hf-Ti-O higher k/IL/Si stack. It could be seen that the Hf-Ti-O film is about 2.55 nm thick and remains amorphous after PDA at 450 °C. The interfacial layer thickness is about 0.57 nm.

Figure 2 illustrates the O 1s spectra of Hf-Ti-O/IL/Si stack. It is found that O 1s peak could be fitted by a standard Gaussian curve-fitting procedure and could be deconvoluted into three subpeaks, corresponding to Hf(Ti)-O (530.2 eV), Si-O (532.3 eV), and silicate Hf(Ti)-O-Si (531.4 eV), respectively, showing the formation of interfacial silicate. Additionally, XPS analysis shows that the atomic ratio of Ti/(Hf + Ti) is ~9.4%.

Characterization of the Electrical Properties of Hf-Ti-O Higher k/IL/Si Stack

Figure 3 demonstrates the measured and simulated C–V characteristics of the MOS capacitors with Hf-Ti-O (a) and HfO_2 (b) as gate dielectrics, where the labeled dots denote the measured data and the solid curves show the simulated C–V curves. The EOT of TiN/Hf-Ti-O/IL/Si stack is extracted to be 0.69 nm from Fig. 3a. Furthermore, the effective permittivity of laminated Hf-Ti-O/IL (interfacial layer) is calculated to be as high as 17.6 for which two reasons are responsible. One is the higher permittivity of Hf-Ti-O

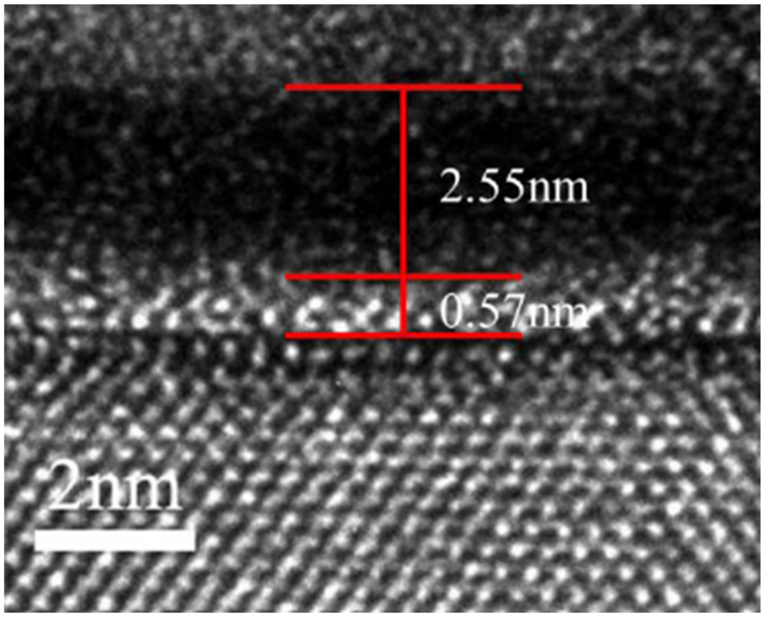

Fig. 1 (Color online) High-resolution cross-sectional TEM image of the Hf-Ti-O/IL/Si stack

higher k which should be greater than 30 on the basis of our previous study [15]. The other is the formation of interfacial silicate layer whose permittivity is greater than that of SiO_2. In addition, the smooth and distortionless $C-V$ curves also indicate the good interface quality and low interface state density. The flat-band voltage (V_{fb}) is about −53.5 mV.

The extracted EOT of MOS capacitor with HfO_2 as gate dielectric is 0.85 nm (as shown in Fig. 3b), greater than that of MOS capacitor with the same physical

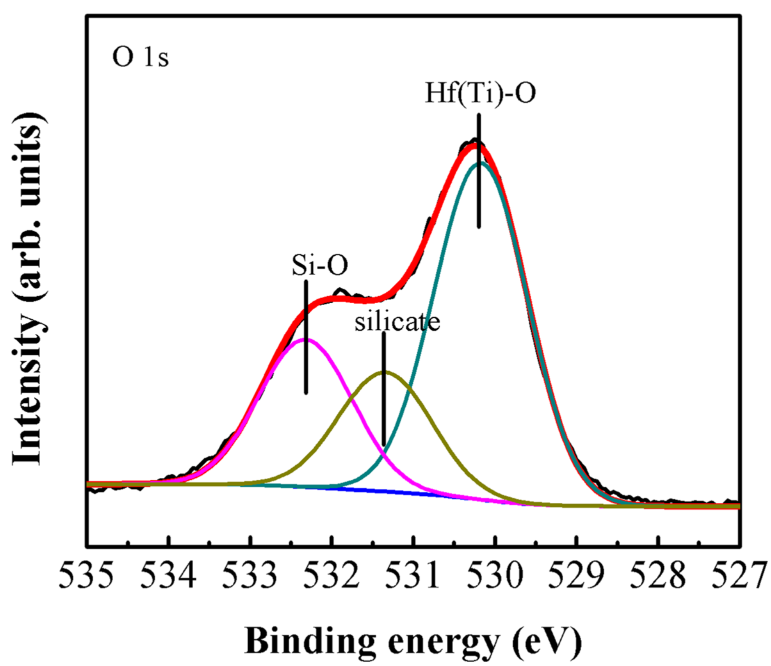

Fig. 2 (Color online) XPS analysis of O 1s core level for Hf-Ti-O/IL/Si stack

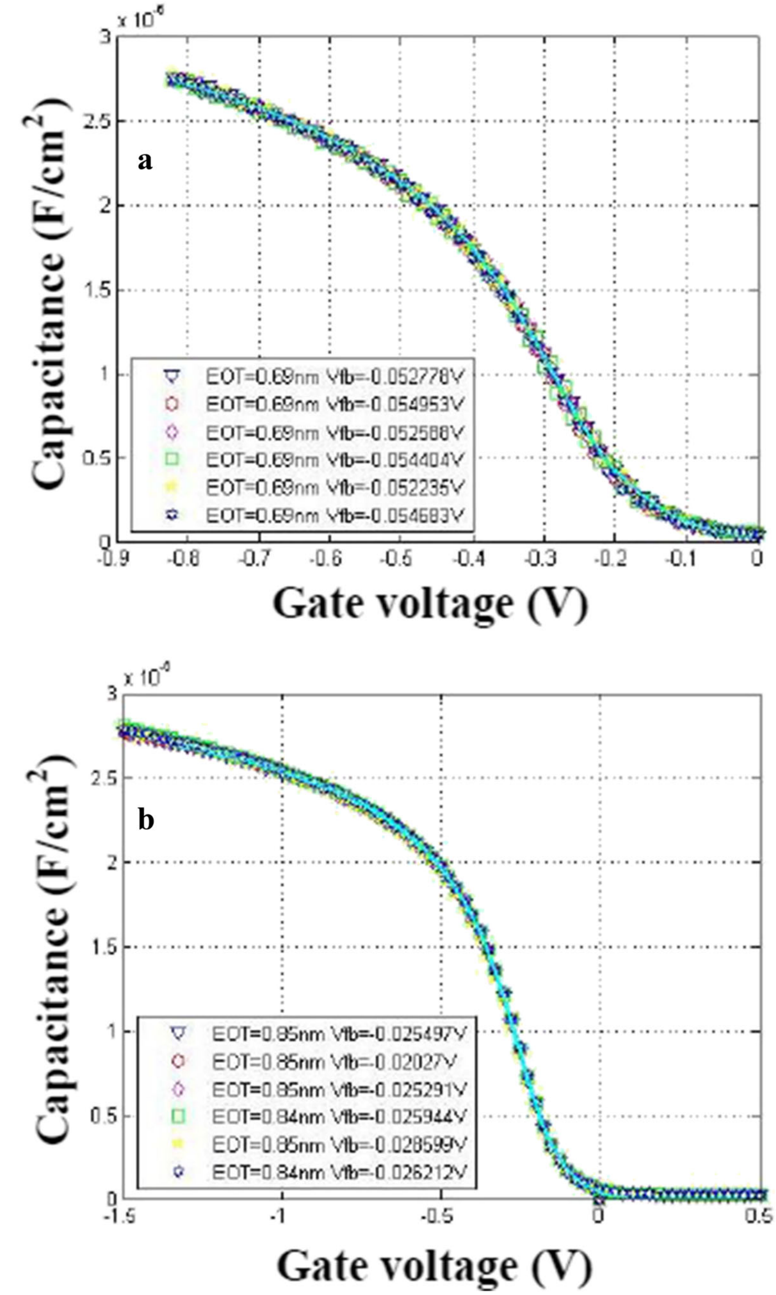

Fig. 3 (Color online) Capacitance–voltage (*C*–*V*) curves at 1 MHz with a gate area of 100 × 100 μm^2 **a** with Hf-Ti-O as gate dielectric and **b** with HfO_2 as gate dielectric

thickness Hf-Ti-O as gate dielectric. The calculated effective permittivity of laminated HfO_2/IL is 14.3. Since the capacitors formed by the laminated high *k*/interfacial layer are series capacitors, the permittivities of HfO_2 and Hf-Ti-O are calculated to be 20.2 and 30.0, respectively, while assuming the interfacial layer is of the same permittivity of ~6.2.

It is known that the low EOT is helpful in increasing the I_{dsat} (saturation drive current) [16] and reducing the short-channel effects (SCE) [17], thus improving the control capacity of gate bias voltage on the channel charges. Lower EOT could be obtained by using Hf-Ti-O higher *k* compared with HfO_2 with the same physical thickness, suggesting Hf-Ti-O is beneficial to decrease

SCE. Additionally, the extracted flat-band voltage (V_{fb}) is about −25.1 mV.

Integration of higher k materials, while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing, are also challenges to be faced [1]. The gate leakage current density (J_g) versus gate voltage (V_g) for TiN/Hf-Ti-O/IL/Si stack is demonstrated in Fig. 4a. $J_g < 1$ A/cm^2 @ $(V_{fb} - 1)V$ is acceptable in 22-nm technology node and beyond. In the present study, the J_g at $V_g = (V_{fb} - 1)V$ is 0.61 A/cm^2, which is at least five orders lower than that of SiO_2 at the same EOT of 0.69 nm [9, 18], and is slightly lower than that of $TaN/TiO_2/HfO_2/Si$ stack with ~0.8-nm EOT [9], while the J_g at $V_g = (V_{fb} - 1)V$ is 7.3×10^{-2} A/cm^2 while using HfO_2 as gate dielectric (not shown here).

It is known that TiO_2 has smaller band gap and conduction band offset compared with HfO_2 [16],

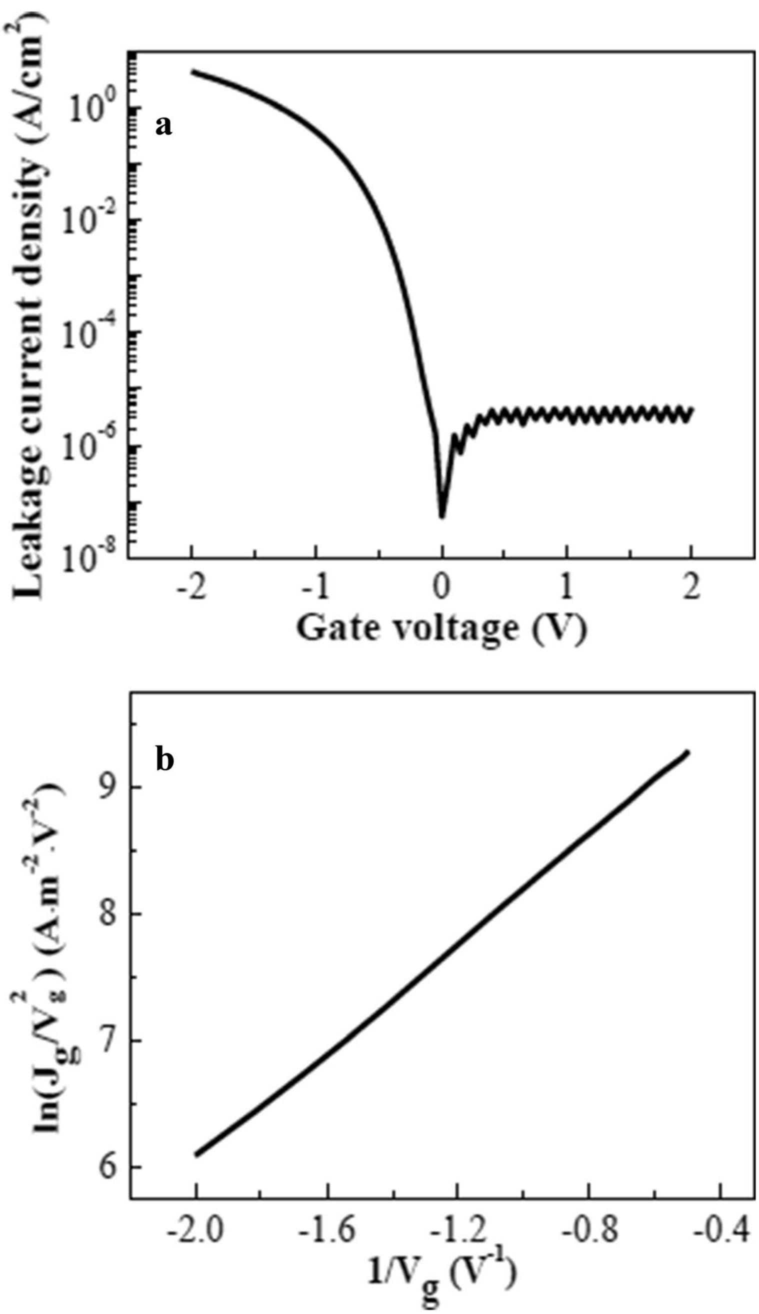

Fig. 4 a Gate leakage current density versus gate voltage (J_g–V_g). **b** F-N tunneling mechanism leading to the reduction in band gap and conduction band offset of Hf-Ti-O. However, it is reported that if the Ti content in the Hf-Ti-O films is no higher than 21%, the conduction band offset is still greater than 1.06 eV [8]. Thus, the less Ti concentration of ~9.4% in Hf-Ti-O higher k influences the band gap, band offsets, and J_g not too much. In particular, the intentionally grown SiO_2 interfacial layer also helps to decrease the gate leakage current. As a result, the acceptable gate leakage current density with low EOT of ~0.69 nm was obtained in this study.

It is known that oxygen vacancies are the intrinsic defects in HfO_2 [19, 20]. As for TiO_2, oxygen migration leads to oxygen vacancies [21], the common defects in TiO_2. Oxygen vacancies decrease the resistivity of TiO_2, which makes TiO_2 an n-type semiconductor [22, 23]. Thus, the conduction mechanism through the Hf-Ti-O gate dielectric is expected to be dominated by the Poole–Frenkel emission, a trap-assisted mechanism due to oxygen vacancies. Whereas, it is found that in the gate voltage range of −0.5 to −2 V, there exists a relationship of $\ln\left(\frac{J_g}{V_g^2}\right) \propto \frac{1}{V_g}$, as shown in Fig. 4b, showing that the gate leakage current follows Fowler–Nordheim tunneling [17], an electric field-assisted tunneling mechanism. Fowler–Nordheim tunneling occurs when the electric field is rather large, namely the gate dielectric is rather thin. The possible suppression of oxygen vacancy formation or oxygen migration in the $HfO_2/TiO_2/HfO_2$/IL stack still needs further study.

Low EOT of ~0.69 nm and acceptable gate leakage current density for the MOS capacitor indicate the scalability of Hf-based Hf-Ti-O higher k to 10-nm technology node and beyond.

Characterization of the ETSOI MOSFET Performance

In our previous study, we found that for the ETSOI PMOSFET with a W/L of 3 μm/25 nm and with Hf-Ti-O as gate dielectric, when the linear threshold voltage (V_{tlin} at $V_{ds} = -0.05$ V) and saturation threshold voltage (V_{tsat} at $V_{ds} = -0.9$ V) were −0.21 and −0.16 V, respectively, the obtained I_{on}/I_{off} ratio was 3.2×10^4 [24], showing good performances while using Hf-Ti-O films as the high k gate dielectric.

For comparison, the ETSOI PMOSFET with the same physical thickness HfO_2 as gate dielectric was prepared. Under the same process flow, the extracted V_{tlin} and V_{tsat} were −0.22 and −0.17 V, respectively, and the obtained I_{on}/I_{off} ratio was 1.34×10^4 (as shown in Fig. 5). In other words, under the same physical thickness, lower EOT and higher I_{on}/I_{off} ratio could be obtained while utilizing Hf-Ti-O as gate dielectric, suggesting the potential of Hf-Ti-O as higher k.

The I_{on}/I_{off} ratio illustrates the switching performance of a MOSFET at a certain gate bias voltage. The higher the I_{on}/I_{off} ratio, the shorter the switching time. In this study, some process parameters were adjusted in order to increase the I_{on}/I_{off} ratios of ETSOI PMOSFETs with Hf-Ti-O as high k gate dielectric. Subsequently, two ETSOI PMOSFETs with two gate width/gate length of 0.5 μm/25 nm and 3 μm/40 nm were prepared. Figure 6 shows the typical transfer characteristics (I_d–V_g) of two ETSOI PMOSFETs. The device parameters are listed in Table 1. It is found that for both PMOSFETs, they have suitable threshold voltage in the range of −0.3~−0.2 V. For the PMOSFET with W/L of 0.5 μm/25 nm, the linear threshold voltage (V_{tlin} at $V_{ds} = -0.05$ V) and saturation threshold voltage (V_{tsat} at $V_{ds} = -0.9$ V) are −0.35 and −0.28 V, respectively. For the PMOSFET with W/L of 3 μm/40 nm, V_{tlin} and V_{tsat} are −0.27 and −0.22 V, respectively. For two PMOSFETs with W/L of 0.5 μm/25 nm and 3 μm/40 nm, their extracted on-state drive currents (I_{on}) are 246 and 453 μA/μm, respectively, and their I_{on}/I_{off} ratios are 1.12×10^5 and 1.56×10^5, respectively.

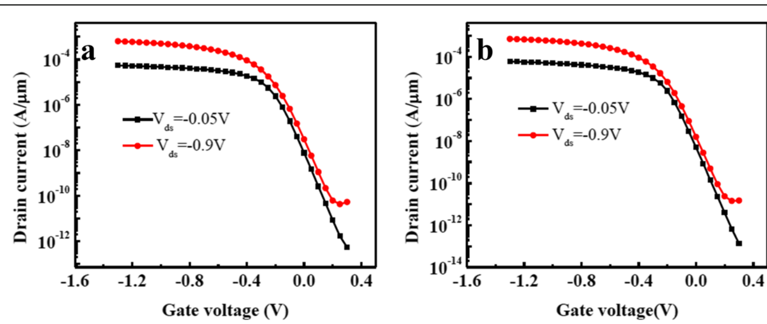

Fig. 5 (Color online) Typical transfer characteristics (I_d–V_g) of two ETSOI PMOSFETs with W/L = 3 μm/25 nm (—*black square*—$V_{ds} = -0.05$ V, —— • —— $V_{ds} = -0.9$ V). **a** With HfO_2 as gate dielectric. **b** With Hf-Ti-O as gate dielectric

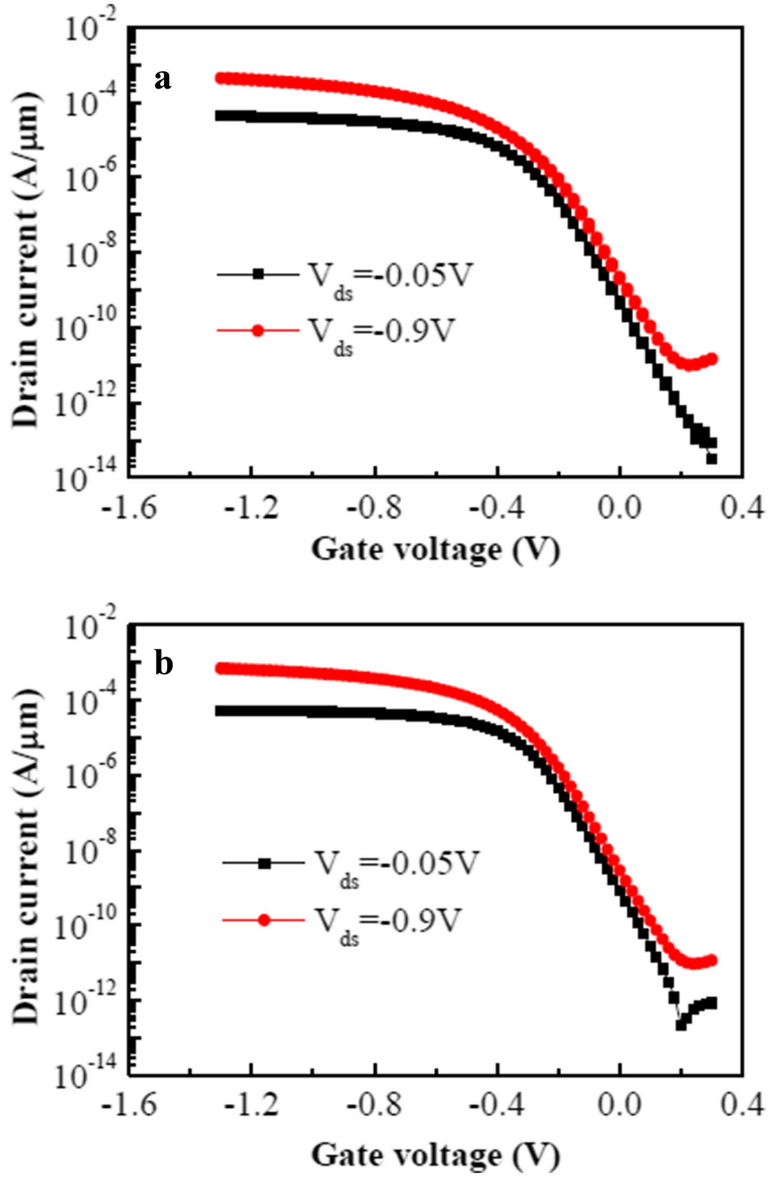

Fig. 6 (Color online) Typical transfer characteristics (I_d–V_g) of two ETSOI PMOSFETs with Hf-Ti-O as gate dielectric ((—*black square*—V_{ds} = −0.05 V, --•-- V_{ds} = −0.9 V). **a** W/L = 0.5 μm/25 nm. **b** W/L = 3 μm/40 nm

Specially, ETSOI PMOSFETs with Hf-Ti-O as high k gate dielectric have superior short-channel control capacity with low DIBLs (DIBL, drain-induced barrier lowering) which are 82 and 59 mV/V for PMOSFETS with W/L of 0.5 μm/25 nm and 3 μm/40 nm, respectively. It is concluded that short-channel effects (SCE) are well controlled even for gate length downscaled to 25 nm.

Modern bulk MOSFETs usually have a subthreshold swing (SS) of 100 mV/decade or more, and typical values for the subthreshold swing in ETSOI MOSFETs are 70~80 mV/decade [25]. In this study, lower subthreshold swings, 70 and 66 mV/decade at V_{ds} = −0.9 V for PMOSFETs with a gate width/gate length of 0.5 μm/25 nm and 3 μm/40 nm, respectively, have been achieved. Moreover, low SS also indicates excellent interface quality [18].

In thin body devices, short-channel effects are controlled by the body thickness instead of the channel doping. The extremely thin top Si film limits naturally the source/drain junction depth as well as the depletion region of source/drain junction, thus improving the DIBL property related with short-channel effects and subthreshold characteristics, as well as lowering the static power consumption.

Table 1 Device parameters for ETSOI PMOSFETs with Hf-Ti-O as gate dielectric

Parameters	PMOSFET (W/L = 0.5 μm/25 nm)	PMOSFET (W/L = 3 μm/40 nm)
I_{on} (μA/μm)	246	453
I_{off} (A/μm)	2.2×10^{-9}	2.9×10^{-9}
I_{on}/I_{off}	1.12×10^5	1.56×10^5
V_{tsat} (V)	−0.28	−0.22
V_{tlin} (V)	−0.35	−0.27
g_m (μS/μm)	522	856
DIBL (mV/V)	82	59
SS (mV/decade)	70	66

Figure 7 demonstrates the transconductance (g_m) versus gate voltage (V_g) curves. The high peak transconductances (g_m) of 522 and 856 μS/μm (also listed in Table 1) for PMOSFETs with W/L of 0.5 μm/25 nm and 3 μm/40 nm, respectively, also show well-behaved transistor characteristics.

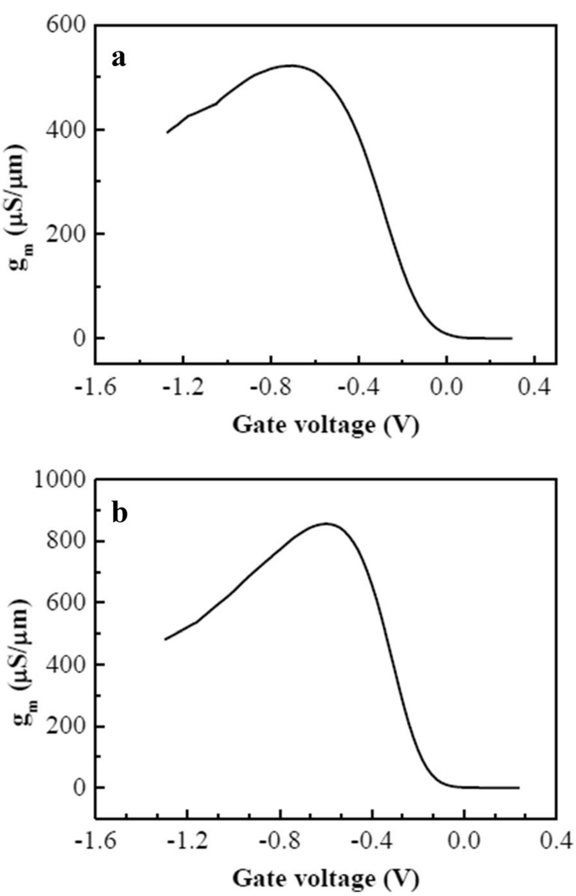

Fig. 7 Transconductance (g_m) versus gate voltage (V_g) curves of the two ETSOI PMOSFETs. **a** W/L = 0.5 μm/25 nm. **b** W/L = 3 μm/40 nm

Conclusions

In summary, low EOT of ~0.69 nm, acceptable gate leakage current density, and good PMOSFET performances including high I_{on}, I_{on}/I_{off} ratio, g_m, and suitable threshold voltage, as well as low I_{off}, DIBL, and SS for two ETSOI PMOSFETs with a gate width/gate length of 0.5 μm/25 nm and 3 μm/25 nm could be obtained while utilizing Hf-Ti-O higher k gate dielectric, appropriate high k/Si interface processing technology, and metal gates. The conduction mechanism through the gate dielectric in NMOS capacitor is dominated by the F-N tunneling in the gate voltage range of −0.5 to −2 V instead of Poole−Frenkel emission. Compared with HfO_2, lower EOT and better ETSOI PMOSFET performance could be obtained while using Hf-Ti-O gate dielectric. Namely, Hf-Ti-O has the potentiality to be used as higher k and is promising in extending the application of Hf-based high k in 10-nm technology node and beyond, although further research on optimizing technological parameters to improve the performances of ETSOI PMOSMETs is still needed. The combination of higher k gate dielectric material and new ETSOI device structure will help to improve transistor performance and continue CMOS scaling.

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Authors' contributions
YX, XC, and FW designed the experiments. YX, XC, ZT, and BT performed the experiments. HZ and WW contributed to the analysis and interpretation of the data. JD and JY were involved in the discussion of the manuscript. All authors read and approved the manuscript.

Competing interests
The authors declare that they have no competing interests.

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