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High-performance HfO_x/AlO_y-based resistive switching memory cross-point array fabricated by atomic layer deposition

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Abstract

Resistive switching memory cross-point arrays with $TiN/HfO_x/AlO_y/Pt$ structure were fabricated. The bi-layered resistive switching films of 5-nm HfO_x and 3-nm AlO_y were deposited by atomic layer deposition (ALD). Excellent device performances such as low switching voltage, large resistance ratio, good cycle-to-cycle and device-to-device uniformity, and high yield were demonstrated in the fabricated 24 by 24 arrays. In addition, multi-level data storage capability and robust reliability characteristics were also presented. The achievements demonstrated the great potential of ALD-fabricated HfO_x/AlO_y bi-layers for the application of next-generation nonvolatile memory.

Keywords: RRAM; Cross-point array; Atomic layer deposition (ALD)

Background

Metal oxide-based resistive random access memory (RRAM) has been extensively studied as one of the most promising candidates for next-generation nonvolatile memory due to the great performances such as fast switching speed, low operating voltage, 3D integration, and good compatibility with CMOS fabrication processes [1-5]. For high-density integration of RRAM array, a cross-point structure with the smallest cell area of $4F^2$ is needed [6,7]. However, the metal oxide-based RRAM devices usually have a large variability [8-10], which hinders application in industries. Thus, it is imperative to seek an effectively technical solution to minimize the variability of RRAM devices.

Various transitional metal oxides such as HfO_x [11-13], TaO_x [14-16], TiO_x [17-19], and ZrO_x [20-22] have been reported as resistive switching materials. Among them, HfO_x is a superior resistive switching material, which has stable electrical properties, good process repeatability, and small leakage current [23,24]. Based on a previous work [25], an additional buffer oxide layer of AlO_y which has a larger oxygen ion migration barrier (E_m) will confine the switching in the active oxide, which can improve the uniformity in HfO_x-based RRAM devices. Both physical vapor deposition (PVD) and atomic layer deposition (ALD) have been applied to fabricate resistive switching layers. Compared to PVD, the ALD technique has more advantages at constructing uniform, conformal, and ultrathin films, which is a central component for high-density and 3D integration.

In this paper, the bi-layered HfO_x/AlO_y films are deposited by ALD as the resistive switching layer of cross-point RRAM array, which shows the precise control of the resistive switching layer in thickness, uniformity, and conformity. The fabricated $TiN/HfO_x/AlO_y/Pt$ RRAM devices in the cross-point array show excellent performances including low operation voltage (+2/−2 V), sufficient resistance ratio (>10), smaller cycle-to-cycle and device-to-device variations, and high yield (>95%). Meanwhile, multi-level data storage capability, good direct current (DC) endurance (>1,000 cycles), and retention ($>10^4$ s at 85°C) properties are demonstrated in the devices.

Methods

The fabrication flow of the HfO_x/AlO_y-based cross-point RRAM array is schematically shown in Figure 1. Firstly, both the 20-nm Ti adhesion layer and 100-nm Pt bottom electrode (BE) layers were deposited on a SiO_2/Si substrate by physical vapor deposition (PVD). Then, the Pt bottom electrode bars were formed by photolithography and lift-off. After that, the 20-nm SiO_2 film was

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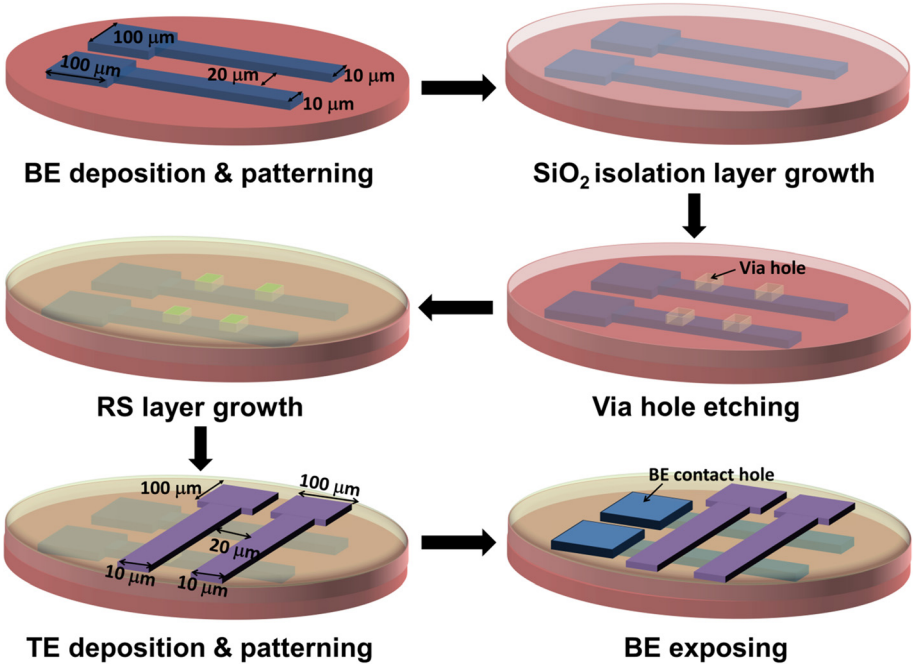

Figure 1 Process flow of the fabrication of HfO_x/AlO_y-based cross-point RRAM array.

deposited by plasma-enhanced chemical vapor deposition (PECVD) to serve as the isolation layer. Different sizes of via holes through the SiO_2 isolation layer from 1×1 μm^2 to 10×10 μm^2 were formed by reactive ion etching (RIE). Then, 3-nm AlO_y and 5-nm HfO_x layers were deposited by ALD (Picosun, Masala, Finland) at 300°C, using H_2O and trimethylaluminum (TMA)/tetrakis[ethylmethylamino]hafnium (TEMAH) as precursors, followed by a furnace annealing in O_2 ambient at 500°C for 30 min. After the 40-nm TiN was sputtered and patterned by photolithography and dry etching to define the top electrode (TE) bars, the contact holes to the pad of the bottom electrode Pt were formed by dry etching. The fabricated array size is 24×24, with cross-bar width of 10 μm and pitch along the x and y directions of 20 μm. The pad area of the electrodes is 100×100 μm^2.

Electrical characterizations were performed using an Agilent B1500A semiconductor parameter analyzer (Agilent Technologies, Inc., Santa Clara, CA, USA). During the measurements, voltage was applied on the TE, while the BE was grounded.

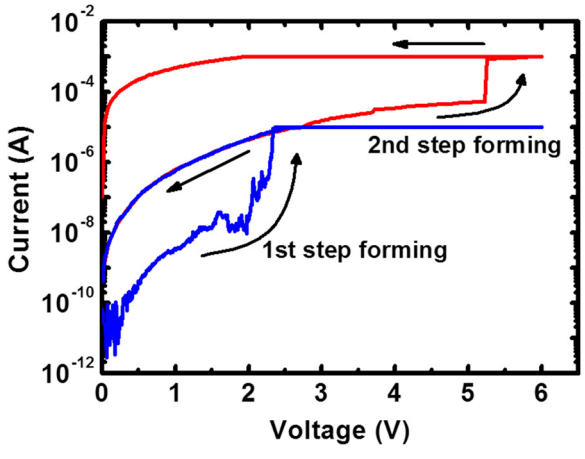

Figure 2 Current–voltage curves of the two-step forming process. The blue line is the first step, corresponding to the soft breakdown of the AlO_y layer, and the red line is the second step, referring to the soft breakdown of the HfO_x layer.

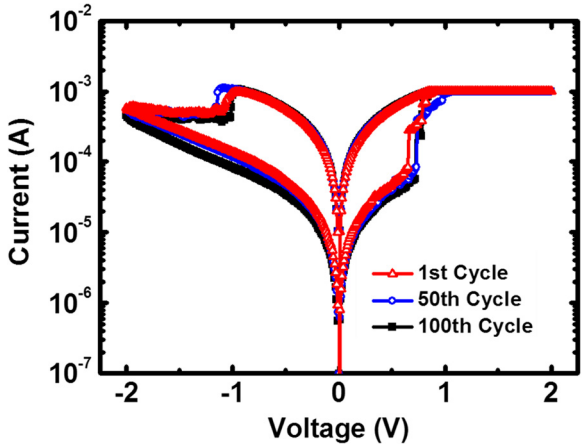

Figure 3 Typical DC current–voltage curve. Measured DC *I-V* characteristics of the HfO_x/AlO_y-based RRAM device for 100 consecutive cycles. Good cycle-to-cycle uniformity can be observed.

Results and discussion

The resistance values of the fresh devices were usually higher than that of the high-resistance state (HRS) after a RESET process. A two-step forming process was required to activate the RRAM devices and achieve stable resistive switching behaviors. The current–voltage (*I-V*) curve of the forming process using voltage sweeping is shown in Figure 2. This two-step forming behavior can be attributed to the inhomogeneous distribution of the electric field in HfO_x/AlO_y layers, which corresponds to the breakdown of HfO_x and AlO_y layers, respectively. The TE, resistive switching layer, and BE comprise a metal-insulator-metal (MIM) structure, which can be regarded as a plate capacitor with two kinds of dielectrics. According to Gauss's law, when a voltage is applied across the TE and BE, the electric field intensity in the HfO_x layer and AlO_y layer can be obtained by the following equations:

$$\varepsilon_{HfO_x} E_{HfO_x} = \varepsilon_{AlO_y} E_{AlO_y} \quad (1)$$

$$E_{HfO_x} d_{HfO_x} + E_{AlO_y} d_{AlO_y} = V \quad (2)$$

Here, $\varepsilon HfO_x/\varepsilon AlO_y$ refers to the dielectric constant of HfO_x/AlO_y, $EHfO_x/EAlO_y$ is the electric field intensity in the HfO_x/AlO_y layer, $dHfO_x/dAlO_y$ is the thickness of the HfO_x/AlO_y layer, and V is the value of the

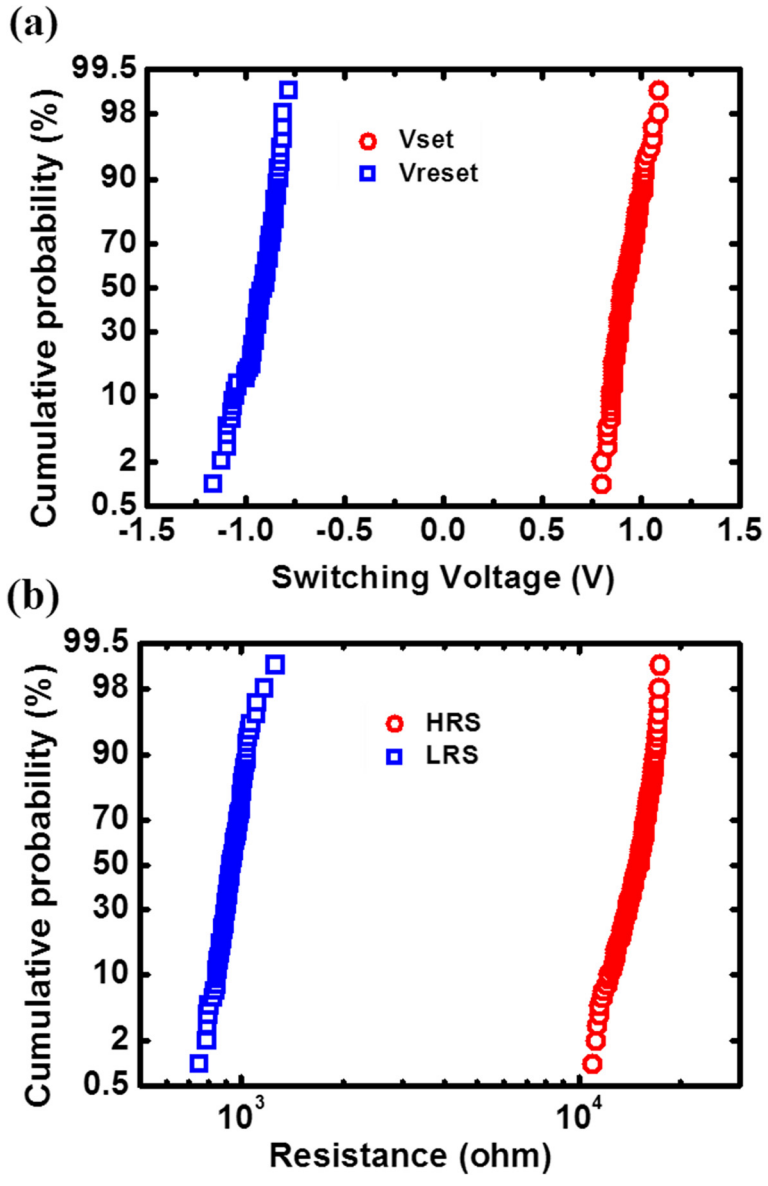

Figure 4 Distributions of switching voltages and HRS/LRS resistances. (a) Distribution of switching voltages. **(b)** Distribution of HRS and LRS extracted from the 100 consecutive cycles. The resistances were read at 0.1 V.

applied voltage. By calculating the above equations, the electric field intensity in the AlO_y layer is found to be stronger than that in the HfO_x layer. Therefore, the dielectric breakdown happens firstly in the AlO_y layer at a lower voltage, and then it happens in the HfO_x layer at a higher voltage.

A typical DC *I-V* curve is shown in Figure 3. During SET/RESET operation, bias voltage was applied to the top electrode from 0 to +2/−2 V and then swept back to 0 V, while the bottom electrode was kept grounded. The devices show typical bipolar resistive switching behaviors, with the 1st/50th/100th DC *I-V* characteristics shown in the figure. The good consistency between the 1st, 50th, and 100th cycles reveals excellent switching cycle uniformity of the RRAM device. Moreover, both switching voltages and HRS/low-resistance state (LRS) distributions were obtained from 100 consecutive DC sweep cycles as shown in Figure 4a,b, respectively. In DC sweep mode, Vset means the voltage at which the current abruptly increases to the compliance current during the set process, and Vreset refers to the voltage at which the current begins decreasing during the reset process. The good cycle-to-cycle uniformity may be attributed to the interfacial effect of the HfO_x/AlO_y layer [25]. The additional buffer oxide layer of AlO_y has a larger oxygen ion migration barrier (E_m) and can confine the

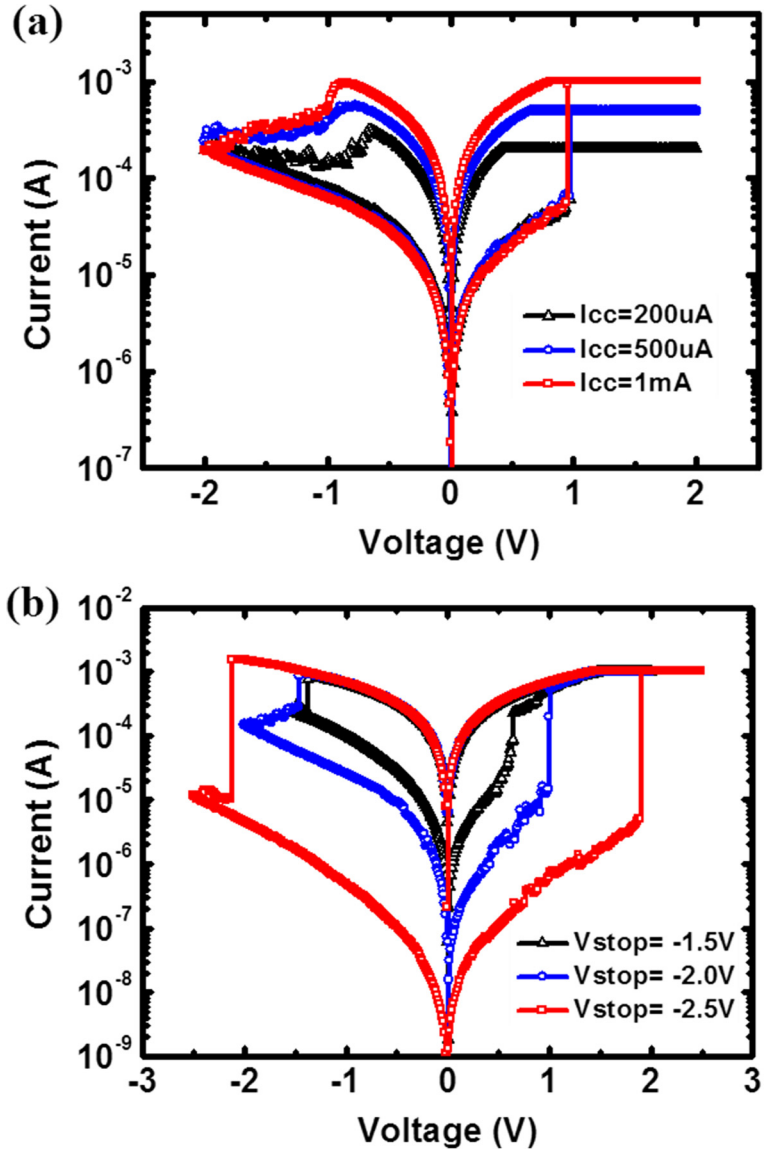

Figure 5 Multi-level RRAM cell. Multi-level resistance states achieved in the HfO_x/AlO_y-based RRAM **(a)** for the SET process by modulating current compliance, and **(b)** for the RESET process by modulating stop voltage.

switching in the active oxide. Among the measured 150 uniformly distributed cells having one 24 × 24 array, only seven RRAM devices cannot switch, which shows the high yield (>95%) of the cross-point array.

A multi-level cell in RRAM is a desirable capability for high-density memory and neuromorphic computing system applications. The multi-level resistive switching behavior of the HfO_x/AlO_y-based devices can be achieved by adjusting both current compliance during the SET operation and stop voltage during the RESET process, as shown in Figure 5. The LRS resistance can be modulated by SET current compliance possibly due to the modulation of the diameter or number of conductive filament (CF), while the HRS resistance can be controlled by RESET stop voltage possibly due to the modulation of the ruptured CF length [24].

Excellent uniformity of the devices is crucial for array operation, since a large device-to-device variation of resistances or switching voltages may cause READ/WRITE failure. To investigate the device-to-device uniformity, resistance distribution and switching voltage distribution of ten devices were statistically measured and extracted. The results are shown in Figure 6a,b, with solid marks and error bars representing the mean values and standard deviations of 100 consecutive cycles, respectively. It can be found that the HfO_x/AlO_y devices show good

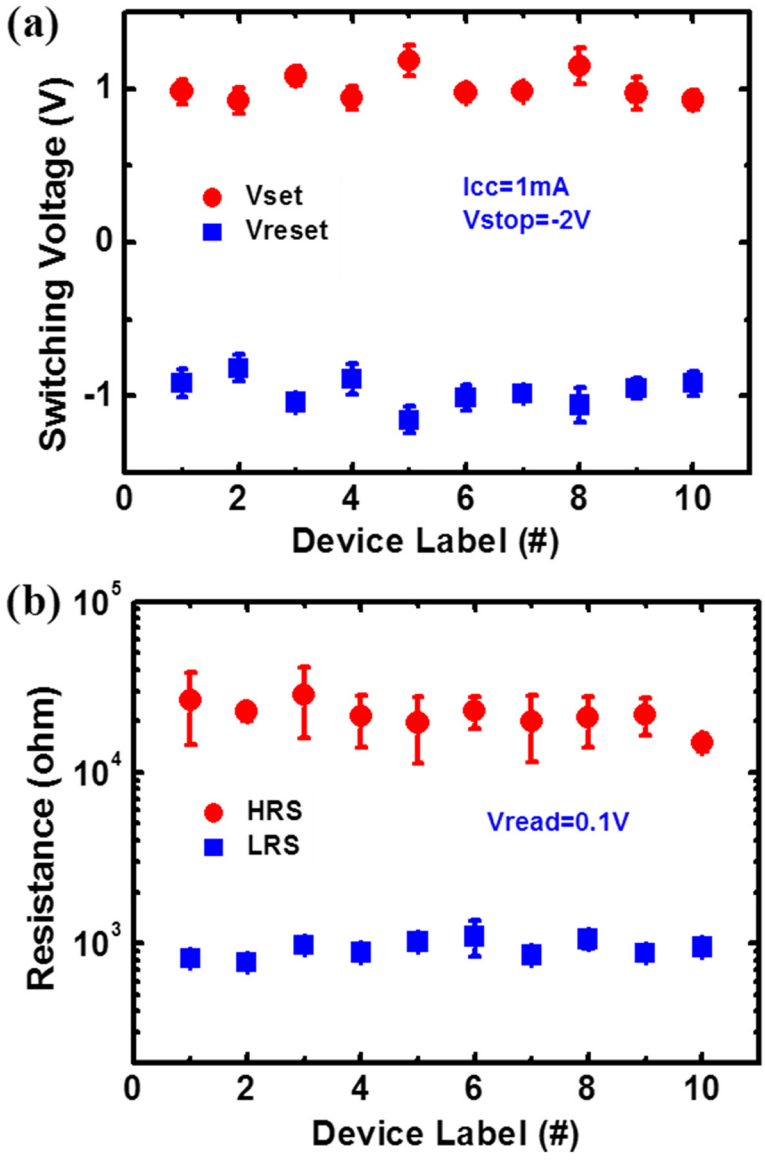

Figure 6 Device-to-device variation. (a) Measured device-to-device variation of HRS and LRS distributions. **(b)** Measured device-to-device variation of switching voltage distribution.

uniformity, which may be ascribed to the precisely controlled resistive switching layer properties in thickness, uniformity, and conformity of the HfO_x/AlO_y layers by the ALD technique.

Figure 7a exhibits the SET/RESET endurance of 1,000 DC sweep cycles of the HfO_x/AlO_y-based RRAM devices. The set compliance current was 1 mA, and the reset stop voltage was −2 V. Both LRS and HRS were read at +0.1 V. Data of every cycle was extracted. Though the resistance is not very stable, the resistance ratio is always larger than 10.

In order to confirm the nonvolatility of the devices, time-dependent evolution of the resistance values of both HRS and LRS was monitored at 85°C. The resistance was read every second with a read voltage of 0.1 V. As shown in Figure 7b, both LRS and HRS show no signs of degradation for 10^4 s.

Conclusions

Excellent resistive switching characteristics of TiN/HfO_x/AlO_y/Pt RRAM devices in a cross-point array structure have been demonstrated in this work. The devices in the array show excellent cycle-to-cycle and device-to-device switching uniformity, which can be attributed to the precisely controlled HfO_x/AlO_y bi-layered resistive switching layer by ALD and the effect on the resistive switching behaviors. These superior characteristics of the cross-point RRAM array could be useful for future nonvolatile memory applications.

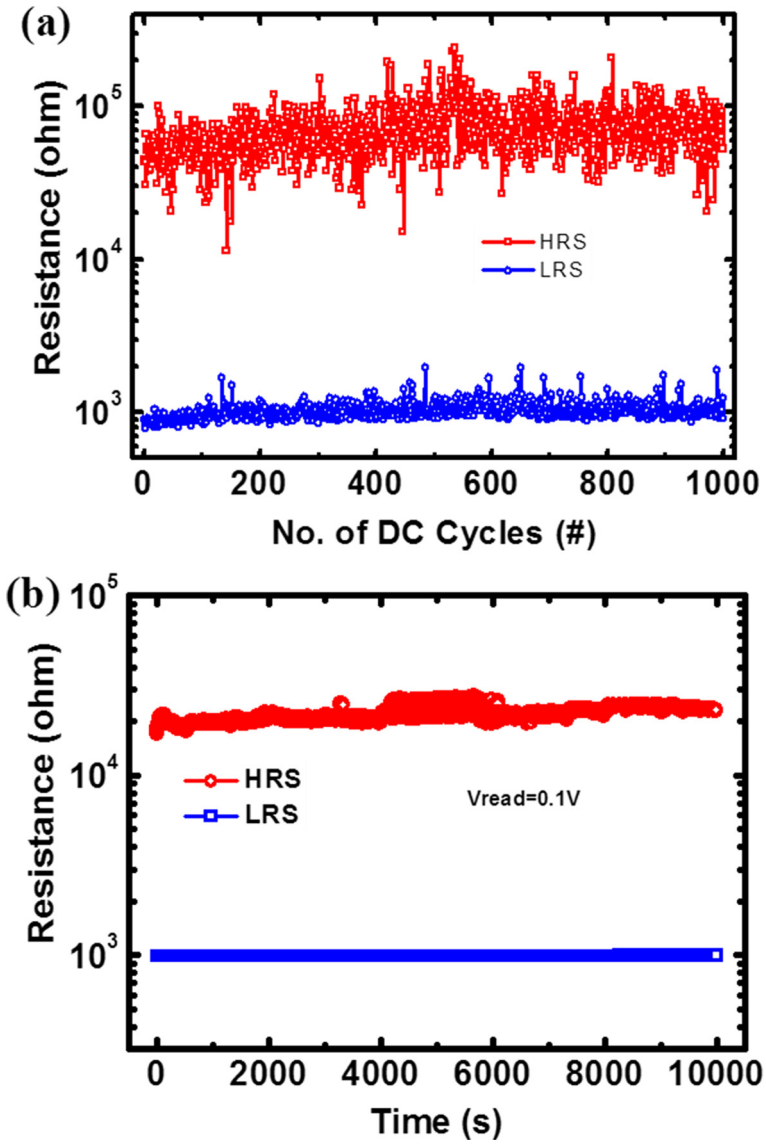

Figure 7 Endurance and data retention. (a) DC endurance characteristics for 1,000 cycles. **(b)** Data retention for both HRS and LRS for 10^4 s at 85°C.

Competing interests
The authors declare that they have no competing interests.

Authors' contributions
ZC fabricated the cross-point memory arrays with the assistance of FZ, carried out the measurement and analysis, and drafted the manuscript under the instruction of JK, XL, LL, and BG. BC and YZ provided useful suggestions for the layout design. JK supervised the work and finalized the manuscript. All authors read and approved the final manuscript.

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