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Design and implementation of arrhythmic ECG signals for biomedical engineering applications on FPGA

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Abstract In this study, eight arrhythmic ECG signals from vital signals [sinus tachycardia, supraventricular tachycardia, premature ventricular complex (PVC), atrial fibrillation, AV block: 3rd degree, ventricular fibrillation, sinus bradycardia, first-degree AV block] were designed mathematically, and then modelled on FPGA by VHDL and Xilinx-Vivado software. The mathematical extrapolation of the signals was created in accordance with the literature and after examining the time and amplitude values of many ECG signals from the Physiobank ATM section of the MIT-BIH (Massachusetts Institute of Technology-Beth Israel Hospital) arrhythmia database. These signals were synthesized for the Zynq-7000 XC7Z020 FPGA chip for using in biomedical calibration applications and ECG simulators. The ECG signals were modelled with a 14-bit AD9767 DAC module that worked in coherence with this development board, and observed in real-time by 4 channel oscilloscope. Matlab-based ECG signals were taken as reference and compared with the results obtained from the FPGA-based ECG signals design. The FPGA chip resource consumption values obtained after the place–route process, the test results obtained from the design, the MSE (mean squared error) values of the designed signals, the operating frequencies of the system and each signal have been presented. The maximum operating speed of this system is 651.827 MHz. In this study, it has been shown that FPGA-based ECG signal generation system can be implemented on FPGA chips, and the designed system can be safely used in ECG simulators.

1 Introduction

Biological signals from living organs reveal useful information about that tissue, and are vital in clinical and research platforms. Biomedical signals are mainly used to detect and diagnose certain pathological or physiological conditions. Also, these signals are used in biomedical research to analyze and model biological systems [1]. The main aims of signal processing are signal noise removal, precise recognition of a signal pattern through analysis, feature extraction for determinant dysfunction, prediction of future pathological or functional events using size reduction and machine learning techniques, and the simulation of signal models to ensure the correct functionality of medical devices that employ biomedical signals for diagnosis and treatment [2]. The research in this work focuses on the processing of biomedical signals that are used for calibrating medical devices employed in the cardiological field. The development of new technologies in healthcare is improving both diagnosis and treatment, but at the same time, problems with safety and efficacy are increasing. The clinical engineering departments of hospitals or related companies generally take the main responsibility for the general management of such technology. Traditionally, clinical engineering departments and related firms are primarily responsible for performing preventive, corrective maintenance repair and calibration in quality control procedures as well as medical devices. This study involves the application of a calibration method, as a quality control procedure in line with international standards, to cardiological devices, to ensure patient safety and wellbeing. A calibration exercise can be defined as a documented comparison of the the measuring device to be checked with a traceable reference device. The reference standard may also be called a "calibrator" [3]. Logically, the reference is more accurate than the device to be calibrated. The reference device should also be traceably calibrated. In some cases, the reference is not a device, but it can be, for example, a mass, a

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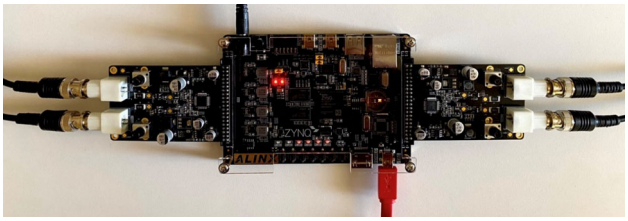


Fig. 1 Zynq-7000 SoC XC7Z020 FPGA development board and 14-bit AN9767 DAC module

mechanical part, a physical reference, a liquid or a gas. Functional testing and calibration of medical equipment is a routine activity that must be performed periodically. Accordingly, digital ECG simulator test devices that produce vital sign signals have been developed for using in cardiological fields. The device emulates a range of normal sinus rhythm, arrhythmia, and test waveforms to evaluate the performance of conventional and modern ECG, and physiological monitoring systems (patient monitor, defibrillators, oxygen saturation devices, blood pressure devices, in vitro/in vivo body temperature measurement devices and end-tidal carbon dioxide recorders). It is also used for staff and student training for the diagnosis of various cardiac events or arrhythmias [4]. In literature, microcontrollers [5] are generally used in the hardware design of the ECG simulators, and this study was carried out by making use of VHDL and FPGA-based technology. FPGA, which stands for **F**ield **P**rogrammable **G**ate **A**rrays, is defined as a hardware chip used to perform logical operations. It consists of an integrated network or logic blocks placed on a chip. These blocks and circuits are programmable logic gates. FPGAs consist of individually **C**onfigurable **L**ogic **B**locks (CLBs) connected via programmable interconnects. As the name of this semiconductor technology suggests, the main advantage of the FPGAs is their ability to be programmed when applied in the field, in contrast to other types of semiconductor chips (e.g. ASICs) that are mostly rigid in their designs and applications.

FPGA technology can be found employed in a wide range of applications that include health, automotive, artificial intelligence, artificial neural networks [6], fuzzy logic [7,8], chaos and chaotic oscillator design [9,10], pseudo and real random number generators [11], video, image [12,13], and signal processing [14], telecom and datacom, server and cloud, defense, and space industries. The work of Koyuncu et al. [15] introduced a new design for an FPGA-based real-time chaotic oscillator. On the other hand, Schwiegelshohn et al., implemented an FPGA-based traffic sign detection application for automotive camera systems on Spartan-6 FPGA development boards [16]. Tang et al. developed an FPGA-based real-time moving target detection system for unmanned aerial vehicle application [17]. In the study by Alabdo et al., an FPGA-based architecture application has been developed for direct visual control robotic systems [18]. In the work presented by Maheshwarappa et al., Software Defined Radio (SDR) architecture was utilized to support multiple signals from multiple satellites, deploy mobile or distributed ground station nodes to increase spacecraft access time, and provide a future SDR for distributed satellite systems [19]. Yılmaz et al. performed a thermodynamic and economic analysis of a geothermal energy supported hydrogen production system using real-time artificial neural networks on FPGA [20]. In the study carried out by Purwins et al., the deep learning method was applied to voice recognition, environmental sound detection, musical information retrieval, synthesis and conversion processes in the field of digital signal processing [21]. In the thesis presented by Taşdemir [22], real-time images captured by a camera were processed with Fast and Harris corner detection and Sobel edge detection algorithms on a Zybo Z7-20 FPGA development board. The processed images were then observed on a monitor via HDMI. In the study conducted by Obadi et al., an application for detecting human vital signs using radar sensors was developed. The work also discusses the integration and coexistence of the human vital signs with communication systems, and the issues encountered in spectrum sharing [23]. A new chaos-based dual entropy core (DEC) TRNG with high operating frequency and high bit generation rate has been realized using a 3D Pehlivan-Wei Chaotic Oscillator (PWCO) structure designed using the RK5-Butcher numerical algorithm on an FPGA and ring oscillator. This TRNG model was developed by Alçın et.al. and was encoded on Virtex-7 FPGA using a 32-bit IQ-Math fixed-point number standard in VHDL [24].

ECG simulators are test devices that produce the same electrical activity of the heart and are used for the calibration of medical devices such as ECG, rhythm holter, patient monitor and defibrillator, all of which measure the vital signs of the patient. Microcontrollers are generally used as hardware in the simulator. In the study presented by Kontodimopoulos et al., a prototype ECG simulator test device was designed and developed for quality control of electrocardiograph and ECG monitor testing and training of waveform recognition [25]. In the study performed by Paul et al., an ECG simulator design was carried out using an ATMega32 microcontroller [26]. On the other hand, Güney et al., presented a new design for a Matlab Web Figure-based ECG simulator that provided ten different arrhythmic signals [27]. In the study by Valais et al., the ECG simulator, whose circuit design was based on the Atmel ATmega8515 microcontroller, was tested on the 12-lead Envitec ECG device [28]. Shirzadfar and Khanahmadi [29], designed an ECG simulator using an ATmega32 or an ATmega16 microcontroller. In the study presented by Das et al., an ECG simulator was designed using a dsPIC30F4013 microcontroller, and the design could test 12-lead ECG devices [30]. In the study performed by Suharinto et al., an ECG simulator was designed using an AT89S52 microcontroller and tested on a 12-lead ECG device [31].

Examples of applications related to vital signs signals using FPGA technology in the literature: in the study presented by Yang et al., a real-time ECG mon-

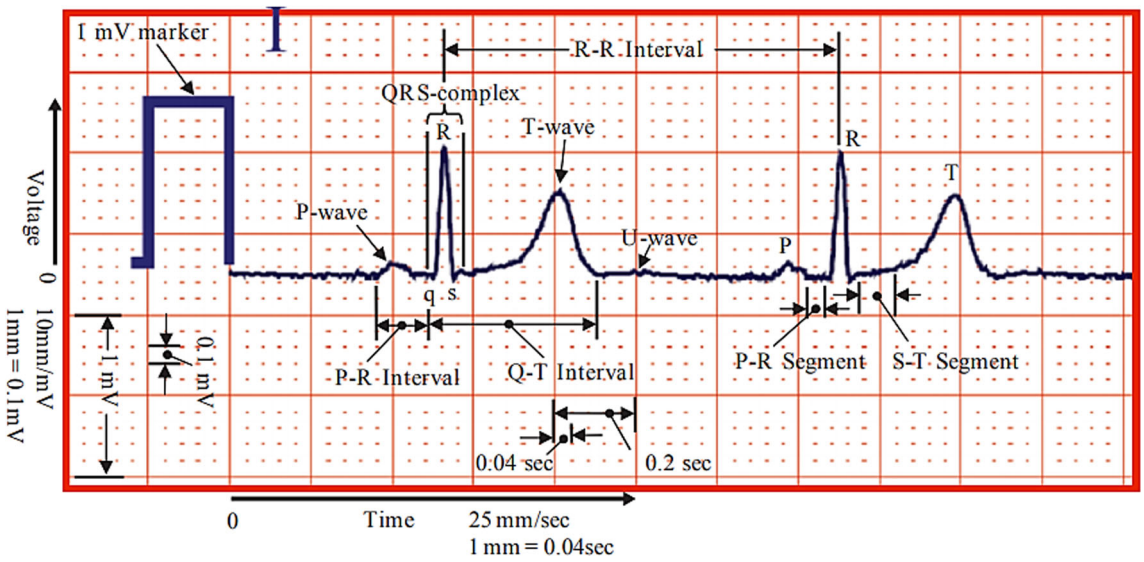
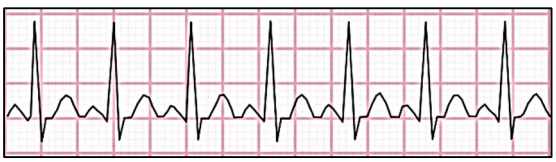
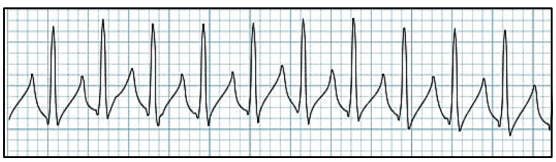
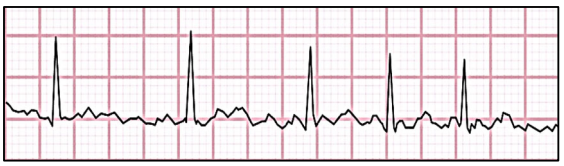
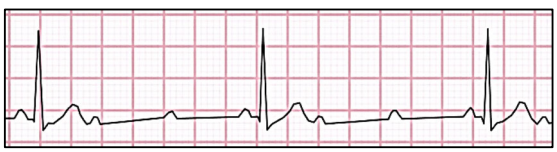
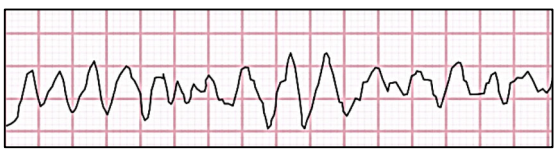
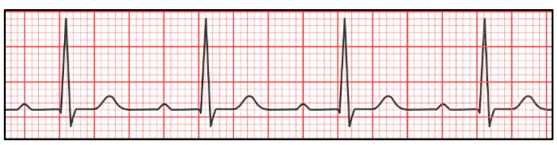


Fig. 2 Typical ECG of a normal person

Table 1 8 arrhythmic ECG Signals used in the design

	
Sinus Tachycardia	Supraventricular Tachycardia
	
Premature Ventricular Complex (PVC)	Atrial Fibrillation
	
AV block: 3rd degree	Ventricular Fibrillation
	
Sinus Bradycardia	First Degree AV Block

itoring system was designed using VHDL as a programming language and a Spartan-3 FPGA development board [32]. In the study by Cvikl and Zemva, QRS complex detection was performed on the signals using the Virtex-II PRO XC2VP30-FF896-7 FPGA kit [33]. Jewajinda and Chongstitvatana [34], presented an FPGA-based ECG signal classification which was based on genetic algorithm and block-based neural network. In the study conducted by Özdemir and Danışman, fault-tolerant artificial neural networks were applied to Cyclone-III FPGA for classification of ECG signals received from an MIT-BIH arrhythmia database [35].

In the work of Desai [36], the heart rate was calculated from ECG signals by using an Altera Cyclone-IV FPGA development board. In their research, Chatterjee et al. [37], used a Xilinx Spartan-2 kit for real-time detection of P and T waves on ECG signals. In the study carried out by Özdemir and Danışman, a classification of ECG signals from the MIT-BIH arrhythmia database was made by comparing artificial neural networks on Cyclone-III FPGA with both 32-bit and 16-bit floating point numerical representation [38]. In the study presented by Aboutabikh and Abouker-dah, a multi-band digital filter using Altera Cyclone II FPGA, was designed and used to extract ECG signals. A digital oscilloscope was then used to characterize the output signals [39]. Woo et al. [40], designed a Xilinx Spartan-3 FPGA-based and real-time ECG simulator, which produces an analog ECG signal in the range of 0 to 5 volts. The system uses ECG data as input and is transferred to the output. In the study by Egila et al. [41], an FIR filter was applied on the ECG signals obtained from the MIT-BIH arrhythmia database using the discrete wavelet transform method. The system was implemented using the Spartan-3AN FPGA development board. In the study conducted by Alhelal et al. [42], an FIR filter was applied on ECG signals obtained from MIT-BIH arrhythmia database. The system, designed using Altera DE-II FPGA development board, was used to detect QRS complexes on signals. Wang et al. [43], designed and implemented an arterial pulse wave generator to produce test signals reflecting specific physiological conditions. The generator used an Altera Cyclone FPGA kit that employed the piecewise Gaussian-cosine fitting method. In the work of Ma et al. [44], a new real-time R wave detection algorithm implemented on FPGA was investigated. In this work, the ECG signal was processed by wavelet lifting, while the R wave was detected using differential operations.

In the study presented by Panigrahy et al., an FPGA-based heart rate calculation was performed by detecting the R peaks of the signal samples obtained from the MIT-BIH arrhythmia database [45]. Gu et al. [46], to accelerate ECG signal processing, presented a streaming architecture implemented on FPGA. The proposed system included QRS detection, feature extraction, and pre-diagnosis. In the study carried out by Kumar et al., a Xilinx Spartan-3E FPGA starter kit and the ECG signals obtained from international databases were processed by digitizing and the application of an FIR filter [47]. Wess et al. [48], presented an FPGA-based ECG arrhythmia detection application that was developed using a Zynq Zedboard FPGA kit and Artificial Neural Network. In the study performed by Alfaro-Ponce et al., arrhythmia detection was accomplished using parallel continuous artificial neural networks on a Xilinx Zynq-7000 FPGA development board [49]. In the study presented by Madiraju et al., a Pan-Tompkins algorithm method using a Virtex-6 FPGA kit was developed for time-domain QRS detection on ECG signals obtained from the MIT-BIH arrhythmia database [50]. Zairi et al., presented a classification of ECG signals from the MIT-BIH arrhythmia database that was made using an Nexys4 Artix7 FPGA kit with artificial neural networks [51]. In the research conducted by Meddah et al., QRS detection and heart rate calculations were conducted on ECG signals by using a Nexys-4 FPGA kit [52]. The work of Karataş et al. [53], presented a normal sinus rhythm that was designed with VHDL. This normal sinus rythim was used for biomedical calibration applications in a Xilinx-Vivado program, and synthesized for a Zynq-7000 XC7Z020 FPGA chip. In the study carried out by Giorgio et al., the detection of ventricular late potentials in ECG signals was achieved using a Cyclone-V FPGA kit [54]. In the work of Jain, the heart rate was calculated by using the R–R interval found in the ECG signals and a ZedBoard Zynq-7000 FPGA development kit [55]. Zhua et al. [56], designed an FPGA-based 8-channel ECG signal acquisition system, of which the main features were data acquisition, analog-to-digital conversion, analog front-end and electrodes.

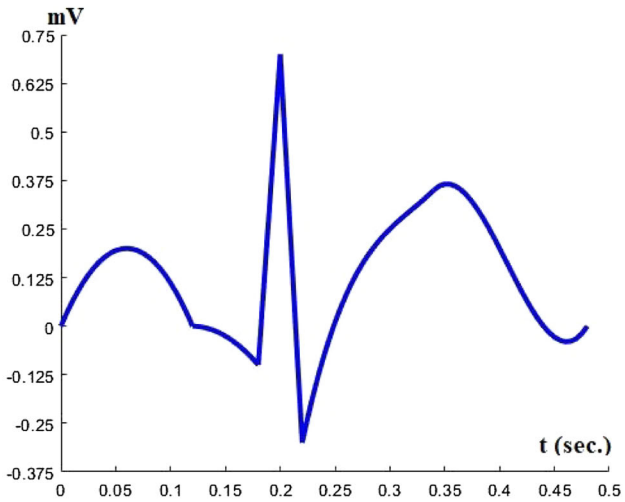
The modeling results of AV block: 3rd degree, sinus bradycardia, ventricular fibrillation and first degree AV block signals is shown in Table 4.

In this study, a contribution to literature was made by modeling 8 arrhythmic ECG signals (sinus bradycardia, sinus tachycardia, supraventricular tachycardia, first-degree AV block, ventricular fibrillation, premature ventricular complex, atrial fibrillation, and third-degree AV block) on FPGA. The hardware-designed FPGA-based ECG simulator is well advantageous when compared to other simulators – due to its highly valuable features which include parallel operation ability with other present simulators, high operating speed, a reprogrammable structure, a revisable signal range, and a conversion of signals into analog signals by expressing them as mathematical equations. If the design system in this study is converted into a final product, the soft-

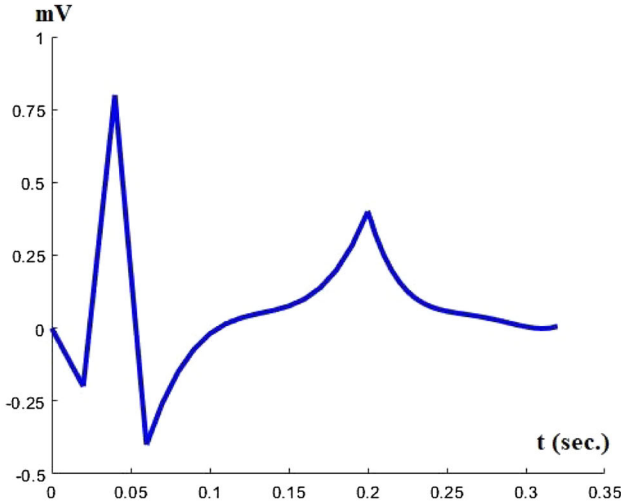
Table 2 Mathematical equations for sinus bradycardia signal

$x = 0.000 : 0.010 : 0.080;$ $\mathbf{y_1 = 0.04 * \sin(x * \frac{\pi}{0.08})}$	(1)
$x = 0.080 : 0.005 : 0.160;$ $y_2 = 0^* x;$	(2)
$x = 0.160 : 0.005 : 0.180;$ $y_3 = -2^* x + 0.32;$	(3)
$x = 0.180 : 0.005 : 0.200;$ $y_4 = 16^* x - 2.92;$	(4)
$x = 0.200 : 0.005 : 0.220;$ $y_5 = -20^* x + 4.28;$	(5)
$x = 0.220 : 0.005 : 0.240;$ $y_6 = 6^* x - 1.44;$	(6)
$x = 0.240 : 0.005 : 0.400;$ $y_7 = 0^* x;$	(7)
$x = 0.400 : 0.010 : 0.600;$ $\mathbf{y_8 = 0.08 * sin\ (x * \frac{\pi}{0.2})}$	(8)
$x = 0.600 : 0.010 : 0.800;$ $\mathbf{y_9 = -0.01 * sin(x * \frac{\pi}{0.2})}$	(9)
$x = 0.800 : 0.005 : 1.200;$ $y_{10} = 0 * x;$	(10)

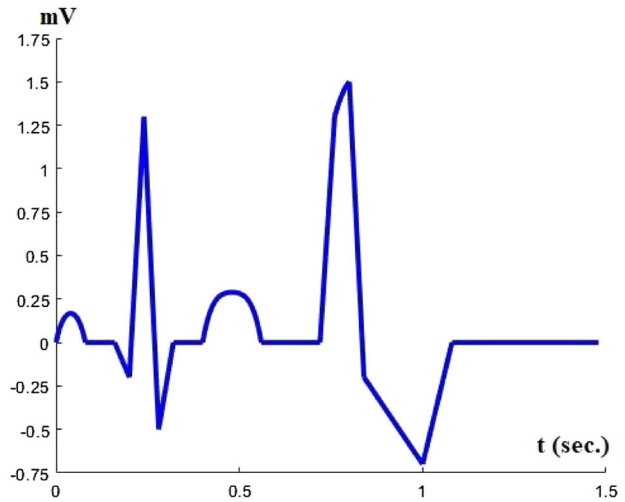
Table 3 Sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals



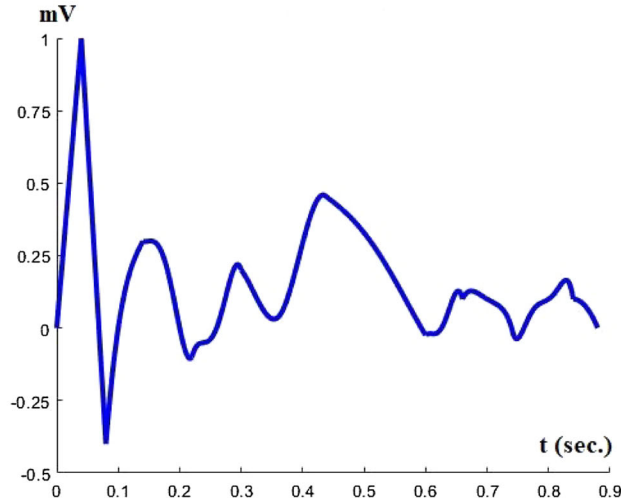
Sinus Tachycardia (125 bpm)



Supraventricular Tachycardia (210 bpm)



Premature Ventricular Complex (PVC)



Atrial Fibrillation (68 bpm)

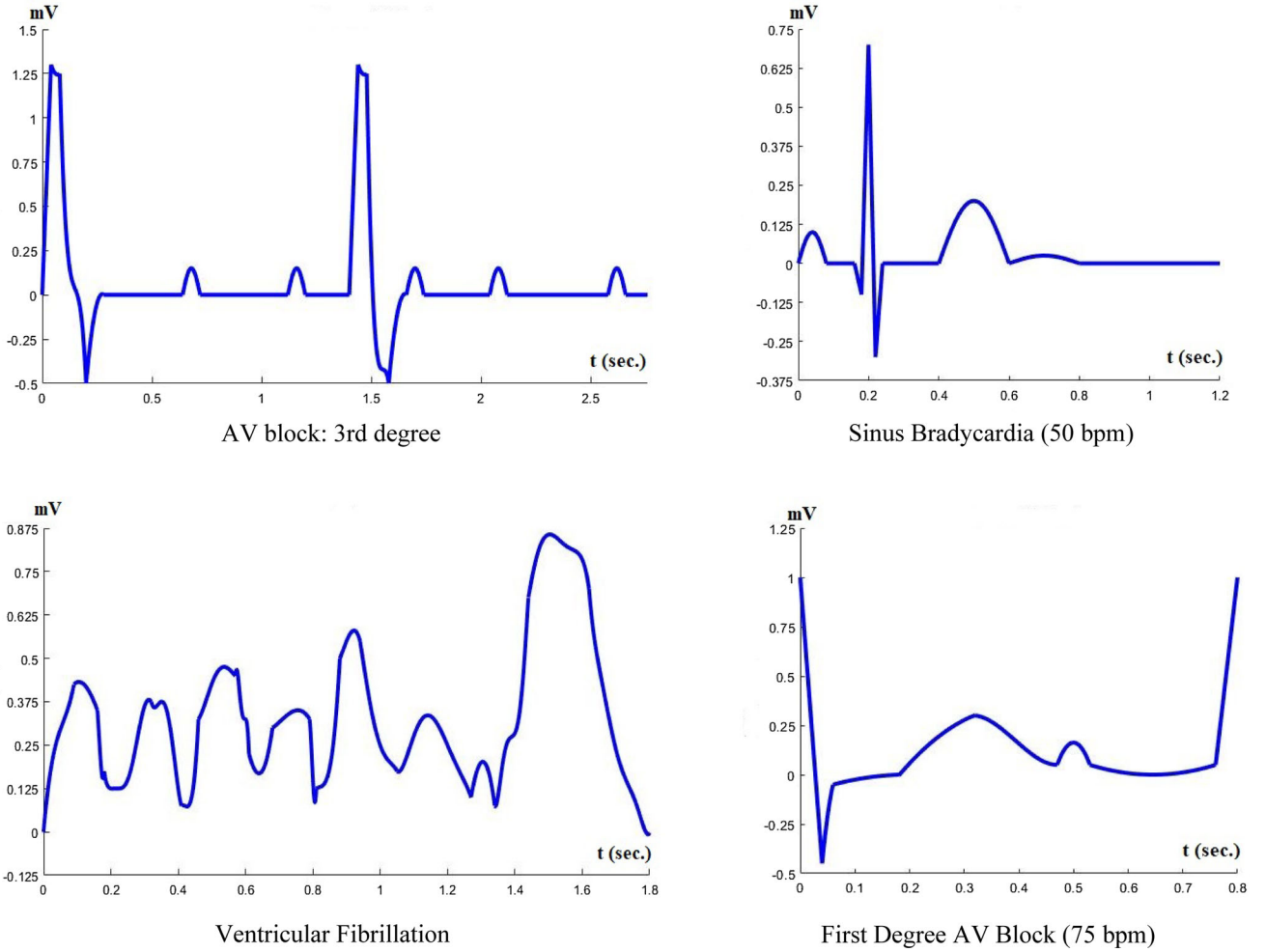
ware can be rearranged to have 12, 6 or 3 leads of vital signs. The current version is designed based on a lead-II configuration. In this way, it has been shown that FPGA chips can be used safely in biomedical calibration applications.

2 Background information

2.1 Development FPGA board and system components

Nowadays, the most important application of programmable logic device (PLD) technology is field programmable gate arrays (FPGAs). FPGAs are digital integrated circuits that consist of programmable logic blocks and interconnections between these blocks. FPGAs are constructed with the aim of performing the logic functions required by the designer. Therefore, the function of each logic block can be edited by the user. The functionality of the basic logic gates and the more complex circuit elements is increased with FPGAs. It is called 'field programmable' because the logic blocks and interconnects can be reprogrammed repeatedly after the manufacturing process. Compared to other platforms, it stands out because of its highly attractive features that include parallel operation, low power consumption, fast initial prototyping, high performance and high operating frequency. FPGA-based systems can be designed and tested using languages such as VHDL, Verilog, Handel-C, System C [57]. An FPGA consists of three programmable components: configurable logic

Table 4 AV block: 3rd degree, ventricular fibrillation, sinus bradycardia and first degree AV block signals



blocks (CLB), input–output blocks (IOBs), and interconnects [58].

This study was carried out using the Zynq-7000 SoC XC7Z020 FPGA development board and the 14-bit AN9767 DAC module shown in Fig. 1. The AX7020 FPGA development board uses an Xilinx's Zynq7000 series of chips, model XC7Z020-2CLG400I, in a 40-pin FPGA package. The ZYNQ7000 chip can be divided into a Processor System part (PS) and a Programmable Logic part (PL). On the AX7020 development board, the PS and PL sections of the ZYNQ7000 are equipped with a wealth of external interfaces and devices for user convenience and functional verification [59].

2.2 ECG signal

The process of recording and interpreting the systole and diastole phases of the atrium and ventricles of the heart; the electrical activity that occurs during the stimulation of the heart; and the transmission of the stimulus on a moving millimetric paper by magnifying the electrical potential created by the heart tissue is called electrocardiography; the recording device is called electrocardiograph; and the trace obtained is called electrocardiogram [60]. This noninvasive method has been developed to examine and diagnose the operations of the heart muscle and the neurotransmitter system of the heart. With this method, important information about conditions such as cardiac dilatation and megacardia, any decrease in the amount of blood going to the heart, problems in the heart valves, new or old heart damage, heart rhythm problems and many hearts and pericardial diseases that are at risk of premature death can be observed [61]. Therefore, the processing and modeling of ECG signals is considered as one of the most important issues in biomedical applications [62]. A heartbeat begins when the sinoatrial node emits an electrical impulse. This node generates an impulse at certain intervals and at a certain speed. The impulse generation and conduction system of the heart consists of four parts as shown in Fig. 2: sinoatrial node (SA), atrioventricular node (AV), atrioventricular bundle (Bundle of His) and Purkinje fibers. The former two form part of the impulse initiation system, while

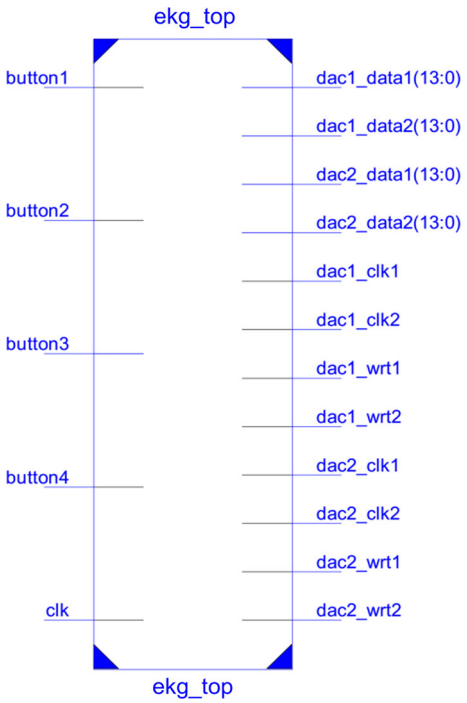


Fig. 3 First-level RTL scheme of FPGA-based ECG signal generation system

the latter two pertain to the conduction system [63]. An ECG signal, is a normal sinus rhythm (NSR) signal consisting of waves, segments and intervals. In Fig. 2, an example of an ECG signal recorded on a moving millimeter paper with an ECG device from a normal human being is given. Waves P, Q, R, S, T and U are also shown. However, it should be noted that a typical and normal ECG may not show the U wave. Figure 2 also illustrates the various segments that can be found in a typical ECG; PR-Segment ve ST-Segment Intervals; QT-Interval, PR-Interval, RR-Interval. Complex; QRS [60].

In this study, a total of eight arrhythmic ECG signals [sinus tachycardia, supraventricular tachycardia, premature ventricular complex (PVC), atrial fibrillation, AV block: 3rd degree, ventricular fibrillation, sinus bradycardia, and first degree AV block] all shown in Table 1, were considered. After numerically extracting these signals in accordance with literature, each signal was expressed with mathematical formulas and then with VHDL in Vivado to be applied to FPGA chips.

3 Design of FPGA-based ECG signal

The ECG signals used in this study were first mathematically formulated on Matlab, and then modeled with VHDL in the Xilinx-Vivado program. The mathematical inference of the signals was created in accordance with the literature, and after examining the time and amplitude values of many ECG signals from the

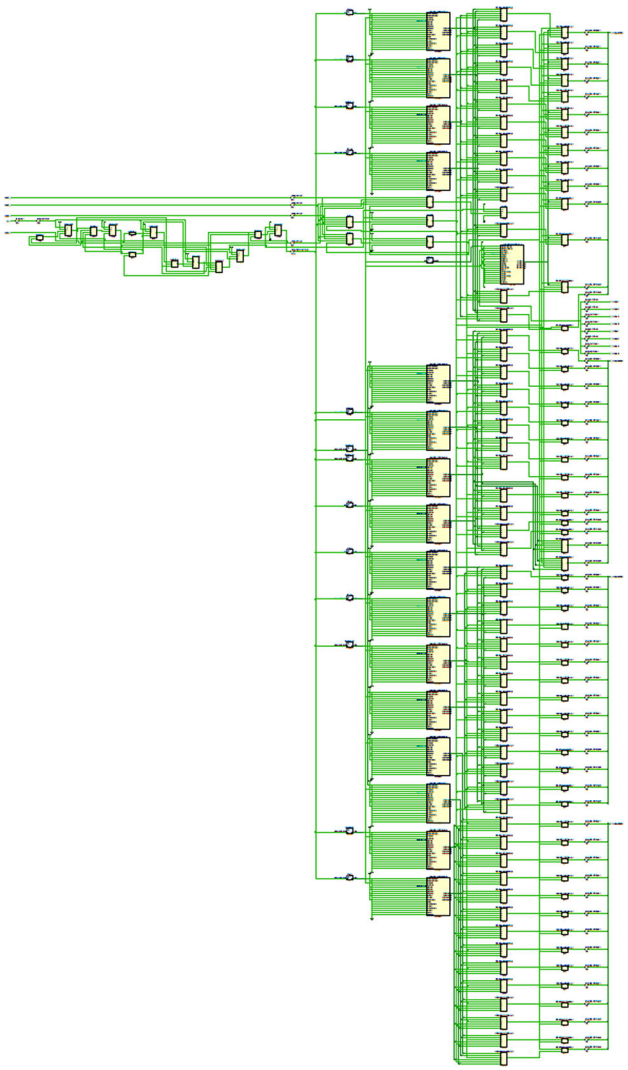


Fig. 4 Second-level RTL scheme of the system

Physiobank ATM section of the MIT-BIH arrhythmia database [64]. These signals were synthesized for the Zynq-7000 XC7Z020 FPGA chip and also modeled by the 14-bit AN9767 DAC module that worked simultaneously with the FPGA chip. These vital sign signals could be observed in real-time on a 4-channel oscilloscope.

The system is designed as a block that generates ECG signals according to certain given parameters. The results of the mathematical equations (functions that calculate ECG values) derived within this study are recorded in LUTs (look-up table). Subsequently, the phase register was created. The phase register increased with each rising clock signal, and this increasing value was modeled to load the values in the LUT and transfer them to the output. This operation was repeated for each period [8].

The generic part of the output signal is defined by the following parameters: the number of bits, LUT depth, number of points, total memory usage, clock speed and fixed NSR parameters. Control signals (clk-clock, rst-

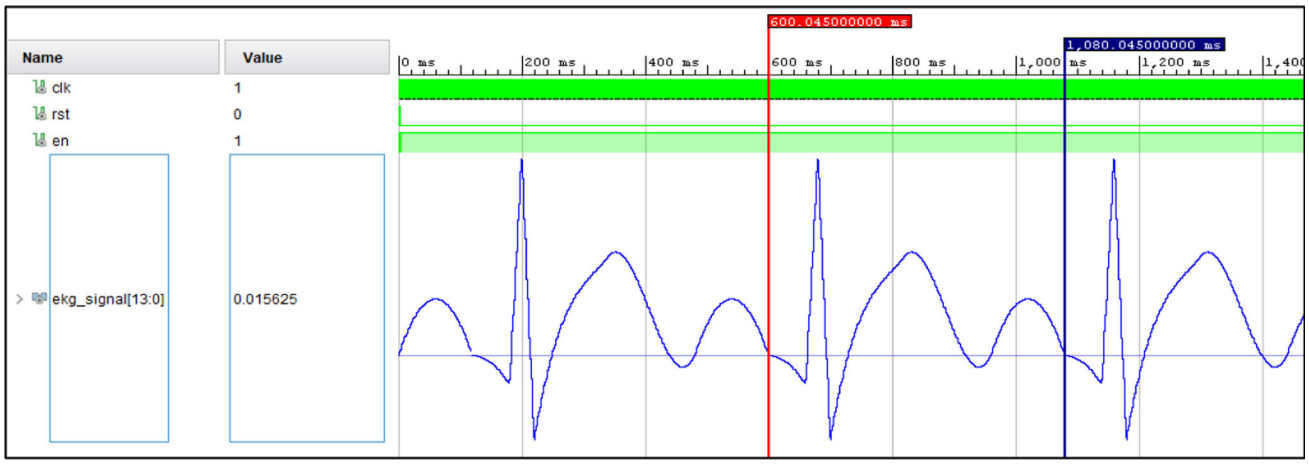


Fig. 5 Vivado simulation of sinus tachycardia

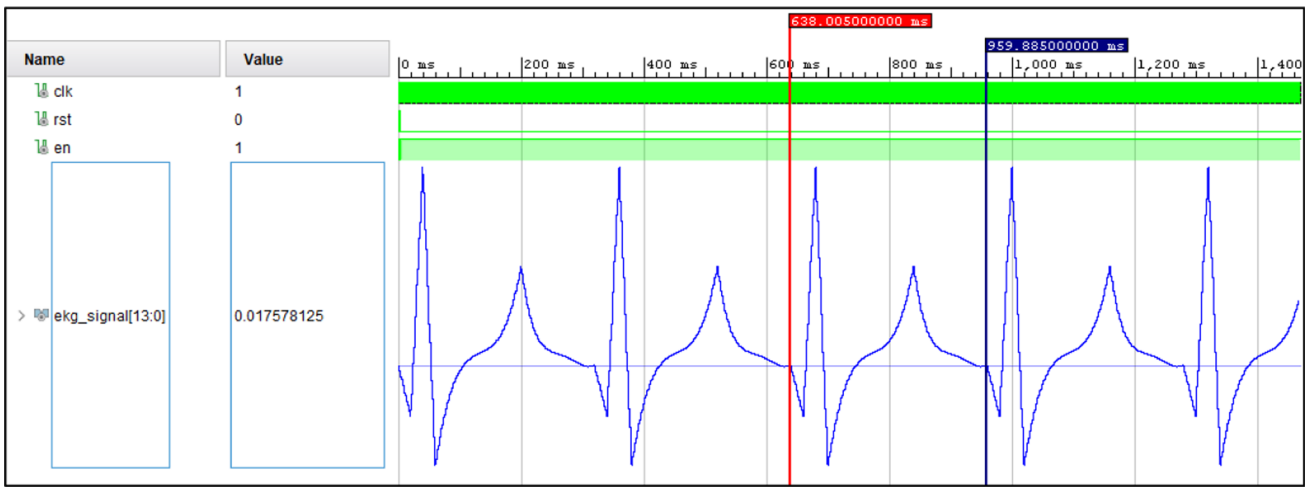


Fig. 6 Vivado simulation of supraventricular tachycardia

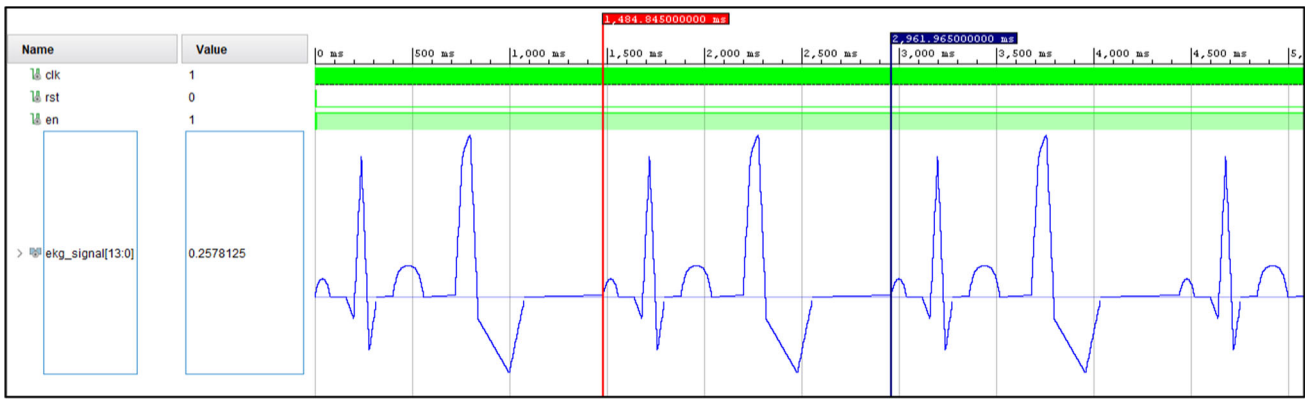


Fig. 7 Vivado simulation of premature ventricular complex

reset, en-enable) and the output signal are defined in the port section. The output signal was 14 bits, LUT size was 10 bits, and the number of dots was 2^{10}. The total memory usage was equal to the output signal $\times 2^{Lut_size}$ (12×2^{10}).

In the architecture section of Vivado design; the output signal is 14-bit length and each element has $2^{10(\mathrm{Lut_{size}})}$ elements. In this section, there are functions that convert from real to signed conversion, and functions that calculate ECG values and indexes. In addition, it is ensured that the signals designed in the LUT are produced, the calculated LUT values are transferred to the output, and the phase register increases by "k" with each rising clock pulse.

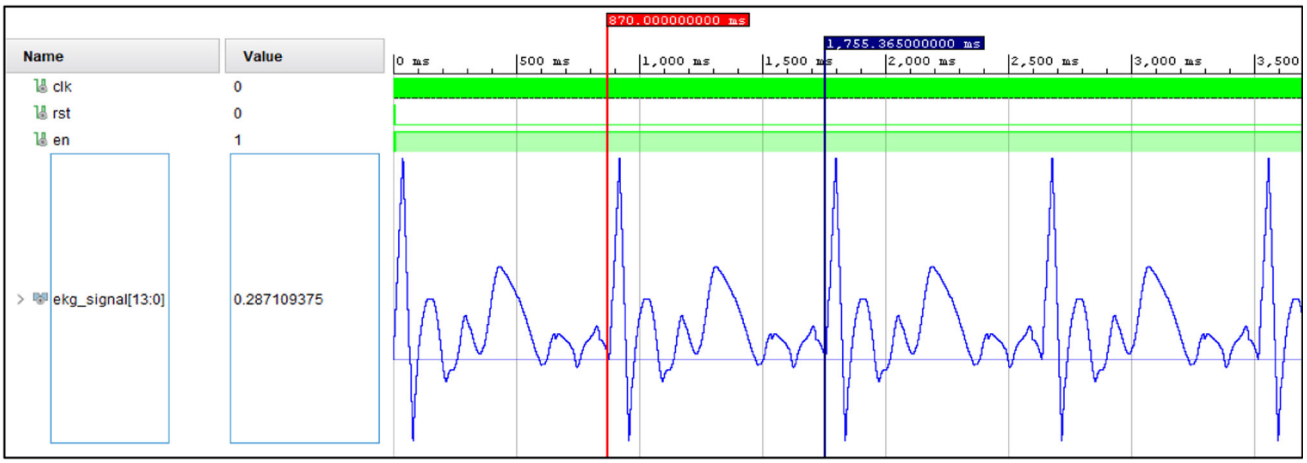


Fig. 8 Vivado simulation of atrial fibrillation

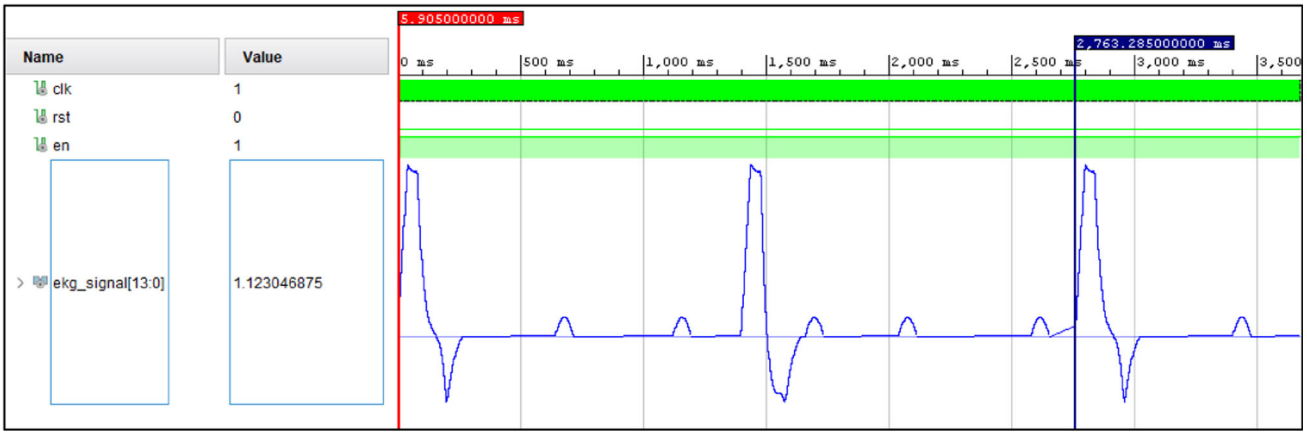


Fig. 9 Vivado simulation of AV block: 3rd degree

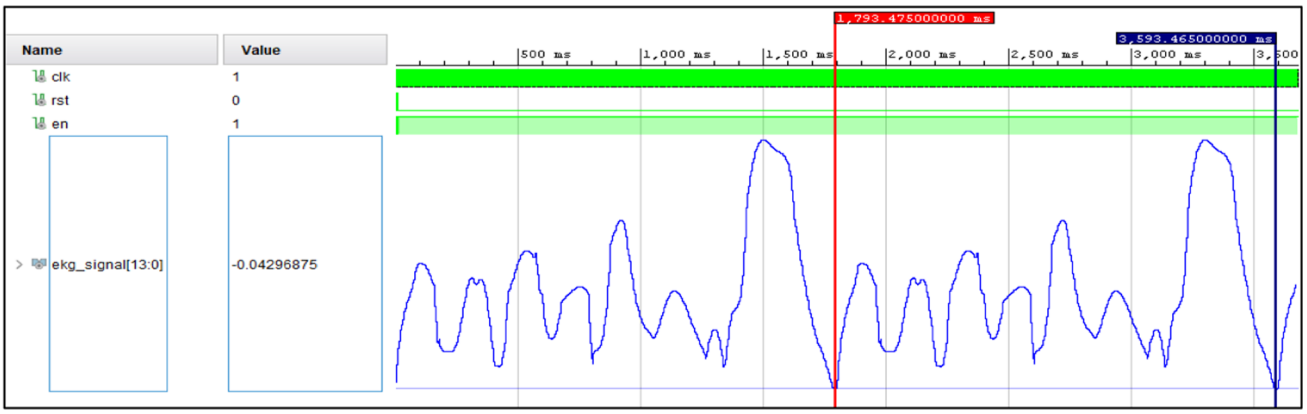


Fig. 10 Vivado simulation of ventricular fibrillation

The working principle of the system is as follows. Temporary phase value is created in the main process section. All registers are reset in the reset state. When the enable is "1", the temporary phase value increases by k in each rising clock signal, and the results stored in the LUT (amplitude values of arrhythmic ECG signals) are transferred to the output. In this study, eight LUTs have been used for eight arrhythmic ECG signals. Then, the transfer of ECG signals to the output via DAC has been performed using PL buttons on the FPGA board.

The results of the mathematical equations (functions that calculate ECG values) created in this study are recorded in the LUTs (look-up table). The "x" parameter in the equations is the time parameter in seconds of the vital signs signal. "y" is the amplitude parameter of vital signs signals in mV. The design of other

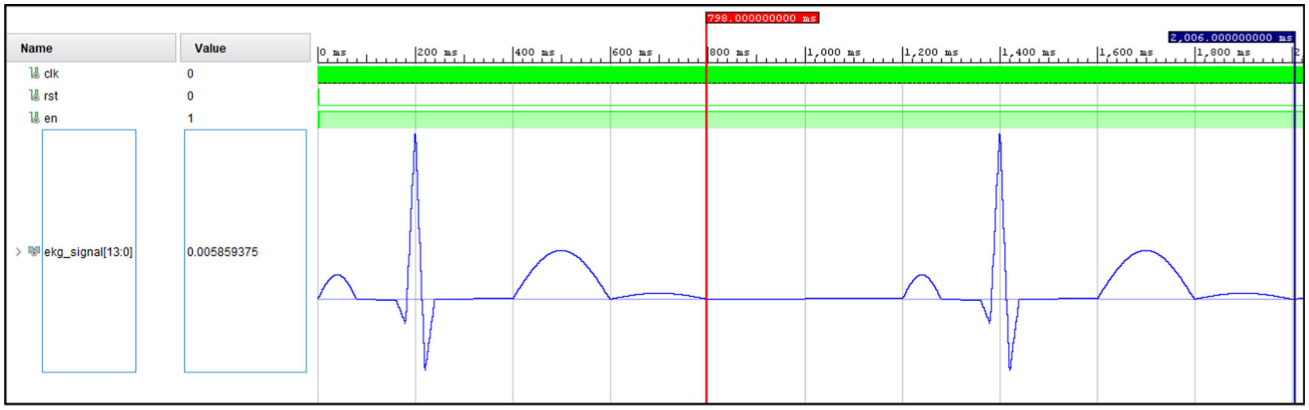


Fig. 11 Vivado simulation of sinus bradycardia

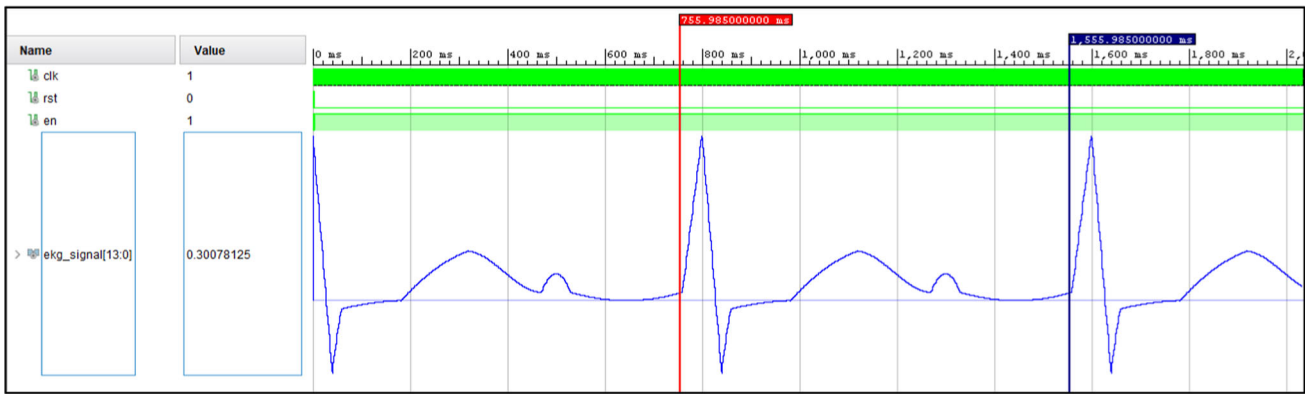


Fig. 12 Vivado simulation of first degree AV block

arrhythmic ECG signals has been mathematically modeled as piecewise functions using similar methods as for the sinus bradycardia signal.

The mathematical equations of the sinus bradycardia signal are given in Table 2. For the NSR signal designed with the heart rate of 50 beats per minute (bpm), the mathematical equations of the generations of P wave, PR-segment (stationary period), ST-segment (stationary period), T wave, U wave and the stationary period from the end of the T wave to the beginning of the P wave have been given in Eqs. (1), (2), (7)–(10), respectively. Also, the mathematical equations of the generation of QRS complex have been given in Eqs. (3)–(6).

The modeling results of sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals, which were mathematically derived and modeled in accordance with time and amplitude values, are shown in Table 3.

The wave segments (stationary period) except for P, QRS and T waves in the sinus bradycardia signal represent the stationary periods. In some arrhythmic signals, this stationary period is present, in others it is not. In Eqs. 2, 7 and 10 found in the sinus Bradycardia signal, the result of amplitude (Y) is always 0 regardless of the time (X) value. When mathematical inference is performed, it is shown as 0^*X to indicate the time intervals of the X values in Eqs. 2, 7 and 10.

The modeling results of sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals, which were mathematically derived and modeled in accordance with time and amplitude values, are shown in Table 3.

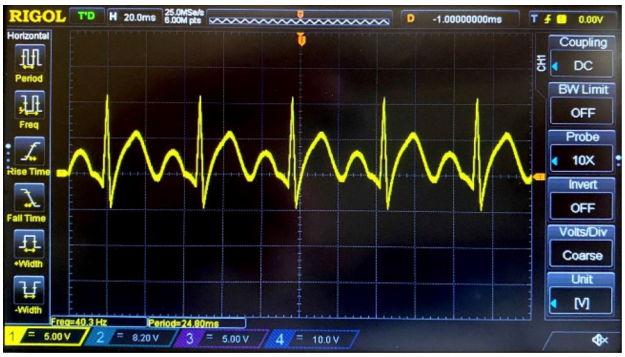
First and second level block diagrams of the system obtained in the study are given in Figs. 3 and 4, respectively.

4 Implementation and test results of FPGA-based ECG signal

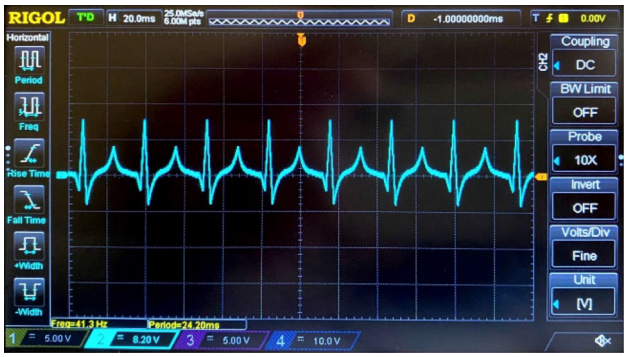
Using the VHDL, eight arrhythmic ECG signals were designed in Xilinx-Vivado. After the coding process, a testbench was made, and sinus tachycardia, supraventricular tachycardia, premature ventricular complex (PVC), atrial fibrillation, AV block: 3rd degree, ventricular fibrillation, sinus bradycardia, first degree AV Block were obtained and displayed on the Vivado simulation screen, in between Figs. 5 and 12, respectively (Figs. 5, 6, 7, 8, 9, 10, 11, 12).

The sinus tachycardia supraventricular tachycardia, premature ventricular complex ve atrial fibrillation, AV block: 3rd degree, ventricular fibrillation, sinus bradycardia, first degree AV block signals obtained from the modelling were observed simultaneously from

Table 5 Oscilloscope results of sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals

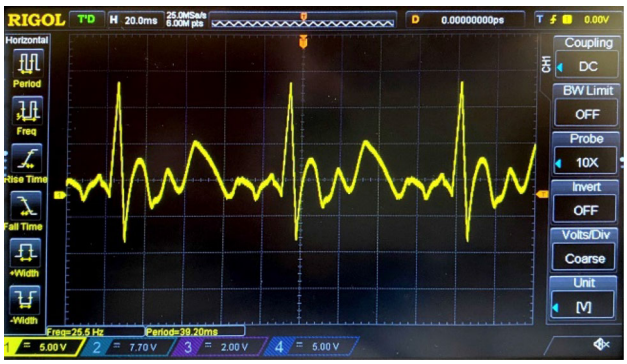


Sinus Tachycardia



Supraventricular Tachycardia

Premature Ventricular Complex (PVC)



Atrial Fibrillation

a 4-channel oscilloscope by using 2 14-bit AN9767 DAC modules working in coherence with the Zynq-7000 XC7Z020 FPGA development board, as shown in Tables 5 and 6.

When PL button-1 on the Alinx brand Zynq-7000 XC7Z020 FPGA development board is pressed, sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals are simultaneously observed from the 4-channel oscilloscope, as displayed in Fig. 13.

The results obtained from the FPGA-based sinus bradycardia signal design were compared with the numerical-based sinus bradycardia signal as reference and shown in Table 7. The result of this comparison gave a maximum MSE value of 9.3017E−06 obtained from the FPGA-based sinus bradycardia signal design. Other arrhythmic ECG signals were compared with a similar method, and MSE results are given in Table 9.

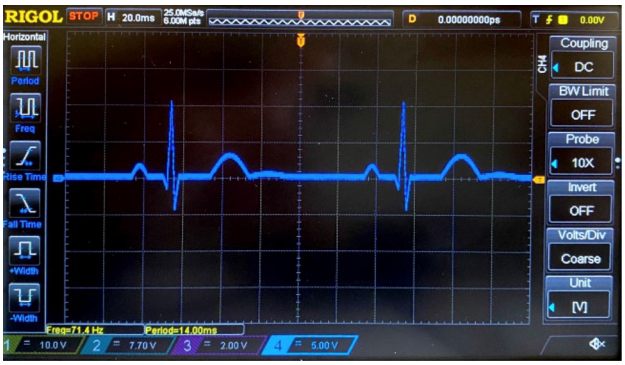
When PL button-2 on the Alinx brand Zynq-7000 XC7Z020 FPGA development board is pressed, AV block: 3rd degree, sinus bradycardia, ventricular fibrillation and first degree AV block signals are simultaneously observed from the 4-channel oscilloscope, as in Fig. 14.

ECG signals are synthesized for the Zynq-7000 XC7Z020 FPGA. FPGA chip resource usage of the design with Place&Route operations are given in Table 8, while the maximum operating frequencies and MSE values of the system are given in Table 9.

Table 6 Oscilloscope results of AV block: 3rd degree, ventricular fibrillation, sinus bradycardia and first degree AV block signals

AV block: 3rd degree

Ventricular Fibrillation



Sinus Bradycardia

First Degree AV Block

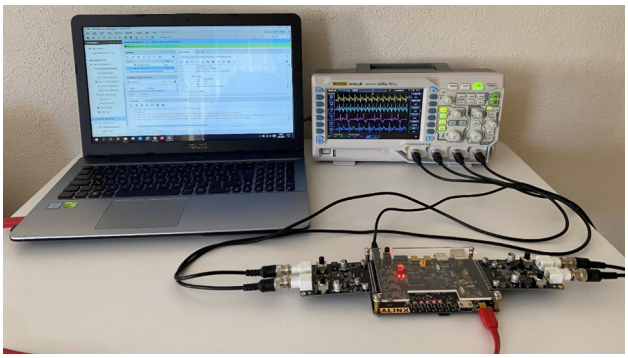


Fig. 13 System components and the oscilloscope results of sinus tachycardia, supraventricular tachycardia, premature ventricular complex and atrial fibrillation signals (PC, Alinx Zynq-7000 XC7Z020 FPGA development board and 2 × 14-bit AN9767 DA modules and 4-channel Oscilloscope)

5 Conclusion

In this study, eight arrhythmic ECG signals from vital signs [sinus tachycardia, supraventricular tachycardia, premature ventricular complex (PVC), atrial fibrillation, AV block: 3rd degree, ventricular fibrilla-

Table 7 Comparison of sinus bradycardia signal in terms of time and amplitude in Numerical and Vivado

Sinus bradycardia	Time (s)	Amplitude (mV)	
	Numerical and Vivado	Numerical	Vivado
Equation (1)	0.00000	0.000000	0.000000
	0.01000	0.038268	0.036011
	0.02000	0.070496	0.070496
	0.03000	0.092388	0.091248
	0.04000	0.099792	0.099792
	0.05000	0.092388	0.091858
	0.06000	0.071106	0.071106
	0.07000	0.038268	0.036926
Equation (1-2)	0.08000	0.000000	0.000000
Equation (2-3)	0.16000	0.000000	0.000000
Equation (3)	0.16500	− 0.026855	− 0.026855
	0.17000	− 0.050000	− 0.050354
	0.17500	− 0.073853	− 0.073853
Equation (3-4)	0.18000	− 0.100000	− 0.099851
Equation (4)	0.18500	0.113525	0.113525
	0.19000	0.300000	0.301208
	0.19500	0.488892	0.488892

Table 7 continued

Sinus bradycardia	Time (s)	Amplitude (mV)	
	Numerical and Vivado	Numerical	Vivado
Equation (4-5)	0.20000	0.700000	0.676575
Equation (5)	0.20500	0.436096	0.436096
	0.21000	0.200000	0.201416
	0.21500	− 0.033264	− 0.033264
Equation (5-6)	0.22000	− 0.300000	− 0.292053
Equation (6)	0.22500	− 0.221558	− 0.221558
	0.23000	− 0.150000	− 0.151367
	0.23500	− 0.080872	− 0.080872
Equation (6-7)	0.24000	0.000000	0.000000
Equation (7-8)	0.40000	0.000000	0.000000
Equation (8)	0.41000	0.031287	0.032959
	0.42000	0.061646	0.061646
	0.43000	0.090798	0.092163
	0.44000	0.117188	0.117188
	0.45000	0.141421	0.142517
	0.46000	0.161438	0.161438
	0.47000	0.178201	0.178833
	0.48000	0.190125	0.190125
	0.49000	0.197538	0.197754
	0.50000	0.199890	0.199890
	0.51000	0.197538	0.197449
	0.52000	0.190430	0.190430
	0.53000	0.178201	0.177917
	0.54000	0.160522	0.160522
	0.55000	0.141421	0.140991
	0.56000	0.118713	0.118713
	0.57000	0.090798	0.090637
	0.58000	0.059814	0.059814
	0.59000	0.031287	0.031128
Equation (8-9)	0.60000	0.000000	0.000000
Equation (9)	0.61000	0.003911	0.003967
	0.62000	0.007629	0.007629
	0.63000	0.011350	0.011292
	0.64000	0.014954	0.014954
	0.65000	0.017678	0.017700
	0.66000	0.020142	0.020142
	0.67000	0.022275	0.022278
	0.68000	0.023804	0.023804
	0.69000	0.024692	0.024719
	0.70000	0.025024	0.025024
	0.71000	0.024692	0.024719
	0.72000	0.023776	0.023804
	0.73000	0.022278	0.022278
	0.74000	0.020225	0.020142
	0.75000	0.017678	0.017700
	0.76000	0.014954	0.014954
	0.77000	0.011350	0.011292
	0.78000	0.007725	0.007629
	0.79000	0.003967	0.003967
Equation (9-10)	0.80000	0.000000	0.000000
Equation (10)	1.20000	0.000000	0.000000

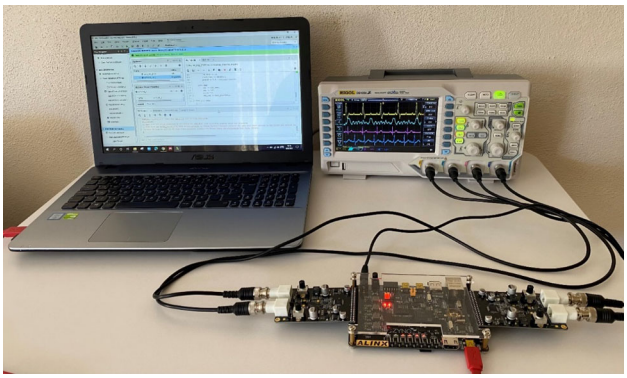


Fig. 14 Oscilloscope results of AV block: 3rd degree, sinus bradycardia, ventricular fibrillation and first degree AV block signals and system components (PC, Alinx Zynq-7000 XC7Z020 FPGA development board and 2 × 14-bit AN9767 DA modules and 4-channel Oscilloscope)

tion, sinus bradycardia, first degree AV block] were implemented on the Zynq-7000 FPGA development platform XC7Z020 chip for using in biomedical calibration applications. First of all, eight arrhythmic ECG signals were mathematically modeled. Then, the system design including the 8 arrhythmic ECG signals was implemented using VHDL in Xilinx-Vivado program. Error analyses were carried out for the results obtained by using the Matlab models as references. After the design process, the system containing the 8 arrhythmic ECG signals was synthesized for the Zynq-7000 XC7Z020 FPGA chip using the Xilinx-Vivado program, and following the Place-Route process, the FPGA chip statistics and the operating speed of the system have been presented for the Zynq-7000 XC7Z020 FPGA chip. The maximum operating speed of this system has been obtained 651.827 MHz. The design of arrhythmic ECG signals was performed in real time, and observed in real time on a 4-channel oscilloscope by means of two 14-bit AN9767 DA modules working in coherence with the development board. Oscilloscope outputs obtained from the design of real-time ECG signals on FPGA were given. With this study, it has been shown that hardware FPGA-based vital signs generation system can be designed using FPGA chips, that the system can be used safely in biomedical calibration applications and that it can be employed in ECG simulators used for calibration tests of medical devices in the field of cardiology. The system was designed based on a lead-II configuration. In future studies, if the system is converted into a compact structure, the software can be rearranged to have 12, 6 or 3 leads. Moreover, other

Table 8 The chip statistics and the maximum operating frequencies for the Zynq-7000 XC7Z020 chip of FPGA-based ECG signal generation system

Logic utilization	Slice LUTs (53200)	Slice registers (106400)	Slice (13300)	LUT as logic (53200)	LUT flip flop pairs (53200)	Maximum operating frequency (MHz)
Ecg top module	347	447	264	347	134	651.827
Sinus tachycardia	18	31	16	18	9	663.504
Supraventricular tachycardia	12	31	16	12	6	657.614
Premature ventricular complex	16	30	16	16	8	657.614
Atrial fibrillation	20	31	16	20	10	651.827
AV block: 3rd degree	15	32	16	15	8	663.504
Ventricular fibrillation	17	32	16	17	9	657.614
Sinus bradycardia	19	32	16	19	10	651.827
First degree AV block	19	32	16	19	10	651.827

Table 9 Mean square error values derived from vital signs design

Vital signs	Mean squared error (MSE)
Sinus tachycardia	1.95208E−05
Supraventricular tachycardia	6.1387E−06
Premature ventricular complex	4.23756E−05
Atrial fibrillation	1.37319E−05
AV block: 3rd degree	7.68791E−05
Ventricular fibrillation	6.744811E−04
Sinus bradycardia	9.3017E−06
First degree AV block	1.04504E−05

arrhythmic ECG signals can be modeled using similar methods and also vital sign signals such as SPO_2, $ETCO_2$ and blood pressure can be added to increase the variety of signals to be used for calibration.

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Data Availability Statement This manuscript has associated data in a data repository. [Authors' comment: There are no external data associated with manuscript.]

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