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Top-down fabrication of silicon nanowire devices for thermoelectric applications: properties and perspectives*

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Abstract. In this paper, the most recent achievements in the field of device fabrication, based on nanostructured silicon, will be reviewed. Top-down techniques for silicon nanowire production based on lithography, oxidation and highly anisotropic etching (wet, plasma and metal assisted) will be discussed, illustrating both advantages and drawbacks. In particular, fabrication processes for a massive production of silicon nanowires, organized and interconnected in devices with macroscopic dimensions, will be shown and discussed. These macroscopic devices offer the possibility of exploiting the nanoscale thermoelectric properties of silicon in practical applications. In particular, the reduced thermal conductivity of silicon nanowires, with respect to bulk silicon, makes possible to obtain high efficiencies in the direct conversion of heat into electrical power, with intriguing applications in the field of green energy harvesting. The main experiments elucidating the electrical and thermal properties of silicon nanowire devices will be shown and discussed, and compared with the recent theoretical works developed on the subject.

1 Introduction

The direct conversion of heat into electrical power by exploiting a temperature gradient is a phenomenon that has been well-known since the 19th century. Currently, thermoelectric devices are largely employed for temperature sensing and controlling in a huge number of domestic and industrial plants. As thermoelectric generator (TEG) devices are simple, compact, robust and very reliable in light of the absence of moving mechanical parts, they offer interesting opportunities in the fields of energy scavenging and green energy harvesting. However, their applications are currently limited by the characteristics of the available thermoelectric materials. The parameter $Z = S^2\sigma/k_t$, where S is the Seebeck coefficient, σ is the electrical conductivity and k_t is the thermal conductivity, or the dimentionless figure of merit ZT, where T is the absolute temperature, are commonly used to express the thermoelectric potential of a material, which is high in materials with high Z values. However, high Seebeck coefficient, high σ and low k_t (thus high Z) are not the only properties to be considered, because a material for a large scale application of TEG devices must be available, not-toxic, easily disposable; technological aspects related to the fabrication of good electrical contacts, interconnections, and so on, need to be considered. Furthermore, both the mechanical and thermoelectric properties of the material should be stable on a temperature range as large as possible, because the efficiency of a TEG is bounded above by the Carnot limit. Thus, a TEG based on a material whose properties are stable on a large temperature range can allow the exploitation of high thermodynamic efficiencies. Tellurium-based compounds, such as the well known Bi_2Te_3 [1], show very good thermoelectric characteristics, but in a limited temperature range centered around room temperature. Even if the temperature range can be increased, for example by using lead-tellurium compounds [2,3], tellurium abundance on the lithosphere is comparable with that of platinum (very rare), and furthermore it is a "dirty" element (environmental pollutant), thus the production and disposal of tellurium-based devices would involve significant environmental problems. Silicon would be an excellent material in view of its Seebeck coefficient and electrical conductivity, both of which can be optimized using standard doping processes. In terms of abundance, it is the second most common element on the Earth's surface and it is considered a biocompatible material. Technological know-how concerning silicon devices is consolidated and widespread owing to the pervasiveness of the electronics material market, and furthermore silicon is very stable for temperatures in excess of 900 K. For these reasons, several research efforts are currently dedicated to the investigation of techniques to reduce the thermal conductivity of silicon, since this is the bottleneck limiting its thermoelectric capabilities, simultaneously maintaining its good electrical conductivity. Several theoretical and experimental studies have demonstrated the potentialities of nanostructuring in reducing the thermal conductivity. Several structural solutions, for example nanohollows [4,5] or nanograins [6], are being investigated. In particular silicon nanowires (SiNWs), which can be fabricated exploiting either bottom-up or top-down

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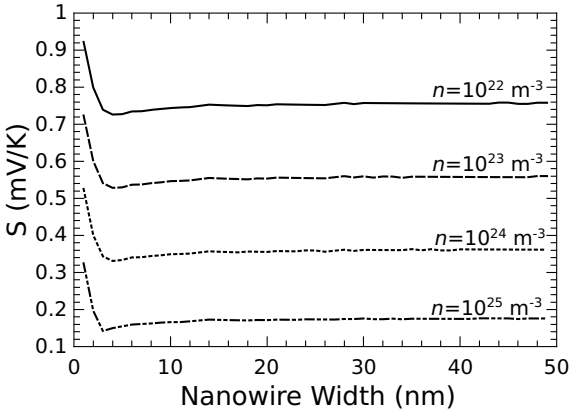

Fig. 1. Seebeck coefficient in silicon nanowires at room temperature, with square cross-section as a function of nanowire width, for different n-doping values. Standard thermoelectric expressions have been used and a huge number of eigenvalues, each giving a contribution to the transport with its 1D density of states, has been considered. For details of the calculation (see Ref. [10]), where results obtained for nanowires with triangular cross-section are reported.

techniques, have showed a strong reduction of the thermal conductivity [7–9] resulting from suppression of phonon propagation due to the surface scattering.

In this paper, after a review of the main theoretical and experimental aspects of thermoelectric phenomena in silicon nanowires (see Sect. 2), the key works on devices based on top-down fabricated silicon nanowires will be reviewed, with particular attention paid to solutions that could be suitable for thermoelectric generation (see Sect. 3). Prospective and future works will be addressed in Section 4.

2 Electrical and thermal transport in silicon nanowires

Several theoretical works [10–13] have demonstrated that the Seebeck coefficient increases in bidimensional [11] and, more significantly, in monodimensional [10,12] structures, such as nanowires. This increase is due to the reshaping of the density of states in low dimensional systems with respect to bulk materials, that spreads charge carriers to higher energies. As an example, Figure 1 shows the Seebeck coefficient in silicon nanowires with rectangular (square) cross-section at room temperature as a function of the cross-section width W, for several n-doping concentrations. The Seebeck coefficient has been numerically evaluated by solving the standard thermoelectric equations, taking into account the contribution of each transverse eigenvalue as a channel with its 1D density of states. For more details on the calculation of the Seebeck coefficient and of the others transport parameters see our previous theoretical work on silicon nanowires [10], where triangular cross-sections have been considered. As reported by several theoretical papers, the Seebeck coefficient shows a noticeable increase for nanowires narrower than 5 nm. Regrettably, the fabrication of nanowires with widths of only a few nanometre is still far beyond our current technological capabilities, at least for practical, large scale applications. Moreover, the electrical conductivity in very narrow nanowires is strongly reduced by the electron (or hole, if p doped) scattering on the nanowire walls. Figure 2a shows the electron mean free path in bulk silicon, as a function of the doping concentration. The mean free path has been evaluated by means of the semi-empirical model of Masetti [14,15]; this model is widely employed for simulations of electrical transport in electronic devices. Parameters for phosphorous doping have been considered. It is intuitive that the electrical conductivity is strongly affected by the surface scattering in nanowires whose width is comparable with the mean free path, which is of the order of several nanometre even for high doping concentrations. In Figure 2b the room temperature electrical conductivity in a silicon nanowire with square cross-section is reported as a function of the cross-section width, for different values of the nanowire doping. The electrical conductivity is normalised with respect to its bulk value for the same doping value. The scattering on the nanowire side walls has been taken into account using a completely diffusive model, corresponding to the worst case scenario if nanowire surfaces are rough. Surface scattering strongly affects (reduces) the electrical conductivity, in particular for moderately low doping values for which the bulk mean free path is longer. In general, it is convenient to work with high doping concentrations because high values of the electrical conductivity are obtained (even if this reduces the Seebeck coefficient, see Fig. 1). For high doping values, the bulk electron mean free path is small (see Fig. 2a), because it is mainly determined by the impurity scattering. Thus, the surface scattering is less effective. However, even with high doping concentrations ($>10^{24} \div 10^{25}$ m^{-3}) the nanowire width/diameter should be greater than 20/30 nm in order to preserve a good electrical conductivity, comparable with the bulk. Comparing Figures 1 and 2, it is evident that the improvement of the Seebeck coefficient as the nanowire shrinks is counterbalanced by the deterioration of the electrical conductivity due to the surface scattering. Therefore, the numerator of the Z factor (the so-called power factor $S^2\sigma$) in narrow nanowires with a diameter/width of few nanometres is, on the one hand, enhanced by the increasing of S, but on the other hand is penalised by the reduction of σ. Conversely, the reduction of the thermal conduction, due to the phonon scattering on the nanowire walls is a very beneficial factor that increases the Z factor (k_t in the denominator). The total thermal conductivity k_t is the sum of two contributions, $k_t = k_e + k_{ph}$, where k_e is the thermal conductivity related to the electron (or hole for p type semiconductors) flux, and k_{ph} is the thermal conductivity due to the phonon propagation. k_{ph} is reduced by phonon surface scattering, while k_e is related to the electrical conductivity through the Wiedemann-Franz law (q is the elementary charge):

$$\frac{k_e}{\sigma T} = \frac{\pi^2}{3}\left(\frac{k}{q}\right)^2 = \left(156\ \mu\mathrm{V} \times \mathrm{K}^{-1}\right)^2. \qquad (1)$$

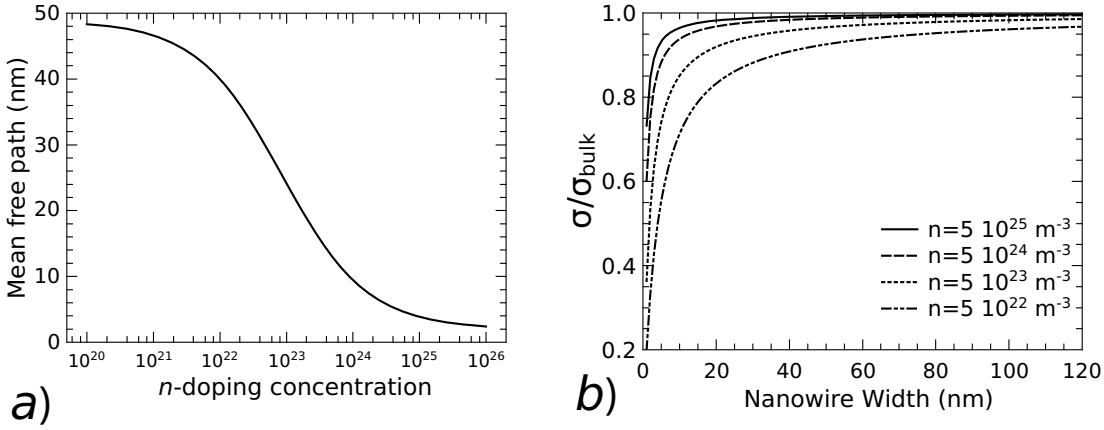

Fig. 2. (a) Electron mean free path in bulk silicon at room temperature, as a function of the n-doping (phosphorous) concentration. (b) Electrical conductivity σ as a function of the nanowire width, normalized with respect to the bulk silicon conductivity σ_{bulk}. The scattering on the nanowire walls has been considered by implementing a simple diffusive model.

In bulk silicon $k_t = 148$ W/mK, where k_e is smaller than 1 W/mK even for high doping values. Thus, most of the silicon thermal conductivity is driven by phonon propagation. In the hypothetical case of $k_{ph} = 0$, the parameter $Z = \frac{S^2\sigma}{k_e}$ could be optimised by reducing the doping, since the factor $\frac{\sigma}{k_e}$ remains constant while S increases as the doping decreases [10]. A reduction of an order of magnitude of k_t (k_{ph}) has been theoretically demonstrated by Balandin and co-workers [16,17], where they made use of a reduced Callaway formalism [18] taking in account the effects of umklapp, impurity and surface scattering of phonons, and also the modification of the acoustic phonon modes due to spatial confinement. Following on from this, several theoretical works [19] have reported on the effect of spatial confinement on the phonon dispersion, which is important in nanowires narrower than 20 nm. All of these theoretical works confirmed a strong reduction of k_{ph}. The thermal conductivity of silicon nanowires has been measured for the first time by Li et al. [7], who reported a reduction of k_t down to 8 W/mK for nanowires 22 nm wide. They used silicon nanowires synthesised by the vapor-liquid-solid (VLS) method, and developed a technique for positioning a single nanowire between microfabricated suspended plates, where Pt resistors are integrated and used both as heating elements and as temperature sensors. In a successive work, Hochbaum et al. [9] used nanowires fabricated by Metal-assisted Chemical Etching (MaCE, see the following section), and measured a very small k_t of 1.6 W/mK for nanowires 50 nm wide, estimating a phonon thermal conductivity k_{ph} of about 1 W/mK. Their measured values are five to eight times smaller than those obtained with VLS nanowires of the same diameter. This has been interpreted as an effect of phonon surface scattering, because MaCE nanowires have a higher surface roughness with respect to VLS nanowires. This strong reduction of k_t has been observed by several groups, using different fabrication processes for nanowires and different techniques for the measurement of the thermal conductivity. Boukay et al. [8] measured k_t of the order of 1 W/mK for 10 nm wide nanowires fabricated on a micro hot-plate by a top-down process based on superlattice nanowire transfer [20]. The work of Chen et al. [21] confirmed the reduction of the thermal conductivity for MaCE nanowires at low temperatures. Silicon nanowires, fabricated on a silicon-on-insulator (SOI) wafer by electron beam lithography and etch have been used by Hippalgaonkar et al. [22]. Nanowires have been fabricated between hot plates with Cr/Pt heater- temperature sensors. Park et al. [23] used VLS-grown nanowires; they achieved different surface roughness by a suitable control of the radial growth, and confirmed that k_t decreases more in rougher nanowires. Feser et al. [24] fabricated SiNW arrays by a two-step MaCE process: an initial metal-assisted etching step is used for the generation of smooth vertical nanowires, and then a second MaCE step is used for inducing a controlled surface roughness.

They measured the thermal conductivity of the whole array by time domain thermoreflectance. The work of Lim et al. [25] reports a quantitative correspondence between surface roughness and thermal conductivity. They fabricated smooth nanowires by VLS growth and roughened them by using an etching process based on MaCE. Pennelli et al. [26] measured the thermal conductivity of smooth, top-down fabricated SiNWs by improving a self-heating/self-measuring measurement technique.

The effect of rough surfaces on the thermal conductivity in nanostructures was discussed by Ziman [27] on the basis of the Casimir theory [28]. Ziman derived a simple expression for the phonon mean free path λ due to the scattering on a rough surface:

$$\lambda = \frac{1+p}{1-p}\lambda_0, \tag{2}$$

where p is the probability of a specular scattering ($1-p$ is the probability of diffusive scattering) on the nanowire wall, and λ_0 is the average distance between each pair of points taken on the perimeter of the nanowire cross-section. In other words, λ_0 is the surface scattering mean free path for perfectly rough lateral surfaces. λ_0 is of the order of the nanowire width, and its exact value depends

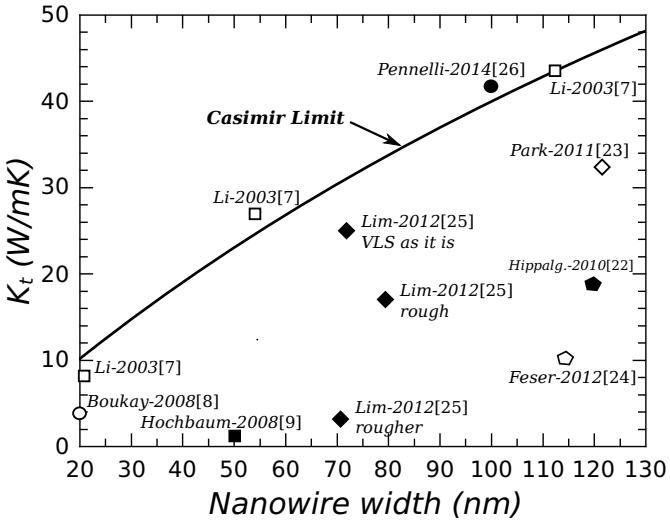

Fig. 3. Thermal conductivities of silicon nanowires, obtained by several experimental works, compared with the Casimir limit (i.e. thermal conductivity obtainable by considering fully diffusive phonon surface scattering). The curve for the Casimir limit has been evaluated by a Callaway model [18,30,31] (see text). The experimental measurements are as follows: Li-2003, from the work of reference [7] about VLS (smooth) nanowires; Pennelli-2014 from reference [26], about top-down fabricated smooth nanowires; Hochbaum-2008 from reference [9], about MaCE rough nanowires; Lim-2012 from reference [25], about nanowires with different roughness; Park-2011 from reference [23]; Boukay-2008 from reference [8]; Hippalgaonkar-2010 from reference [22]; Feser-2012 from reference [24].

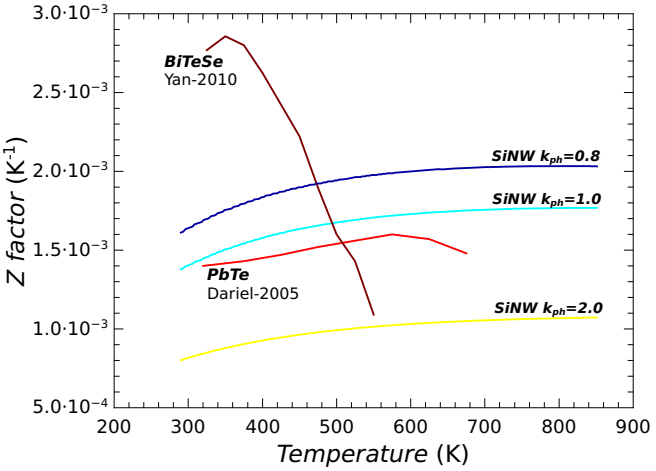

Fig. 4. The estimated Z factor of a silicon nanowire 50 nm wide is reported as a function of temperature, and compared with measured Z values of some tellurium-based compounds taken from the literature. In particular, curve BiTeSe has been taken from the experimental data in reference [32], and curve PbTe has been taken from reference [3]. For the silicon nanowires, different values of the phonon thermal conductivity k_{ph} have been considered.

on the cross-section shape [29]. The so-called Casimir limit is the thermal conductivity of the nanostructure obtained by considering $p = 0$, i.e. all of the phonon scattering events on the side surfaces are diffusive.

Values of k_t measured by different experimental papers are reported in the graph of Figure 3 for several nanowire widths. These experimental results are compared with the thermal conductivity evaluated with a theoterical model that is a modified version of the Callaway-Holland [18,30,31] formalism. The model considers both longitudinal and transverse acoustic phonon modes, and it takes into account normal phonon scattering, umklap phonon-phonon scattering, impurity scattering and surface scattering. For the surface scattering, it has been assumed that all of the phonon scattering events on the nanowire walls are diffusive (Casimir limit), so that the mean time between resistive boundary scattering events is given by $\frac{\lambda_0}{v_s}$, where $\lambda_0 \simeq W$ and v_s is the sound velocity of the longitudinal (or transverse) phonon branch. Parameters for all of the other phonon scattering events have been taken from reference [30], and Matiessen's rule [29] has been used for combining the different scattering times. Figure 3 shows that Li et al. [7], on smooth VLS grown silicon nanowires, and also Pennelli et al. [26], on top-down smooth nanowires, found experimental values which are in satisfactory agreement with this model. Several other experimental works used rough nanowires, and found a thermal conductivity well below the Casimir limit. It is worth noting in Figure 3, that the work of Lim et al. [25] demonstrated the decreasing of k_t, well below the Casimir limit, with increasing roughness.

These intriguing experimental results stimulated the theoretical modelling of phonon "rough" surface scattering. Several theoretical works have taken into account coherent effects between reflected phonons [33–38]. It has been demonstrated that, for an appropriate scale of surface roughness, these coherent effects can produce a strong phonon suppression. Even if further modelling is needed for a complete agreement with experimental results, these theoretical works demonstrated that a phonon thermal conductivity below the diffusive limit can be obtained in rough nanowires.

In Figure 4 the estimated Z factor of a silicon nanowire 50 nm wide is reported as a function of temperature, for different values of the phonon thermal conductivity k_{ph}. The thermoelectric parameters $S(T)$, $\sigma(T)$ and $k_t(T)$ have been obtained by numerical solution of the thermoelectric equations [10]. Curves taken from experimental works on tellurium-based materials are also reported for comparison. In particular, BiTeSe compounds [32] showed an enhanced Z factor for temperatures up to 500 K. PbTe compounds [3] have a smaller Z factor, but it is almost constant (high ZT for high T) on a large temperature range (up to 700 K). Silicon nanowires can work on a very large temperature range, because uniformly doped silicon is a very stable material. The Z factor can become very competitive if reliable fabrication of rough silicon nanowires with phonon thermal conductivity of the order of 1 W/mK becomes possible.

3 Silicon nanowire devices for thermoelectricity

Silicon nanostructures and nanowires can be fabricated either by bottom-up or top-down approaches. Bottom-up approaches are based on crystalline growth of nanowires obtained by means of chemical vapour deposition (CVD) techniques. The most common CVD technique for silicon nanowires is Vapor Liquid Solid (VLS) growth [39,40], largely investigated by the group of Lieber at Harvard [41–45]. VLS growth exploits the catalytic effect of metal nanoparticles deposited on a silicon substrate. At high temperatures, silicon, supplied by a silane (SiH_4) flux, forms an eutectic alloy with the metal. Correct calibration of the temperature and the silane flux allows the supersaturation of the silicon/metal alloy, so that silicon crystallises under each metal nanoparticle. Thus, silicon nanowhiskers grow perpendicular to the silicon substrate. In general, bottom-up approaches are capable of massive fabrication of nanostructures on large areas. The crucial point of bottom-up approaches is to develop procedures and processes both for the positioning of the the nanowires with respect to contacts and connections, and for the improvement of the electrical contacts between metal contacts and nanostructures. A thermoelectric device based on bottom-up silicon nanowires has been developed by Davila et al. [46]. They used the CVD-VLS technique to grow nanowires between bulk silicon and a suspended silicon mass, microfabricated on a SOI substrate. A temperature gradient along the nanowires is generated by an heater, fabricated on the suspended mass. A similar thermoelectric device, based on silicon strips fabricated between suspended silicon masses, has been developed by Perez-Martin et al. [47].

It is somewhat more complex to achieve silicon nanostructures [48,49] and nanowires [50–57] by top-down processes, which start from macroscopic structures, such as crystalline silicon wafers, and rely on advanced, high resolution, lithography for nanoshape patterning. Standard processes for integrated circuit (IC) fabrication, such as silicon etch and oxidation, are then used to transfer the patterns onto the substrate and to define the nanostructures. Despite the difficulty of the lithographic step, the main advantage of the top-down approach is that nanostructures are fabricated simultaneously with contacts, connections and control gates, so that complete, functional devices are easily achieved. Moreover, high quality monocrystalline silicon (Czochralsky quality) can be used as a starting material, so that, at the end of the process, nanowires exhibit excellent electrical transport properties. Furthermore, top-down processes are in general compatible with standard IC fabrication techniques; several works have fabricated (and fully characterised) transistors, based on silicon nanowires, exploiting C-MOS processing [58–60]. Therefore, the large-scale exploitation of nanowire-based devices could take advantage of the pre-existing silicon IC infrastructure.

Patterns for top-down nanowire fabrication have been produced by several advanced lithographic tools, such as atomic force lithography [54,55,61] and high resolution electron beam lithography [50,51,62,63]. Relaxed lithography, with pattern resolution wider than 50 nm, can be employed if silicon oxidation is exploited for nanowire width reduction [53,56]. Processes that are based on reduction by silicon oxidation [64,65] offer interesting possibilities for large-scale production of top-down silicon nanowires, since advanced optical lithography (with length scales under 100 nm) is becoming a standard in conventional C-MOS IC processing.

Figure 5 shows a sketch of a typical top-down process [51–53] for the fabrication of devices based on silicon nanowires. The starting substrate is a Silicon-On-Insulator (SOI) substrate, ⟨100⟩ oriented. The process can be adapted and optimised for different thicknesses of the top silicon layer in the range 100−300 nm. The top silicon layer can be either n or p doped. Doping concentration can be tailored by using standard silicon doping techniques. A top silicon dioxide (SiO_2) layer that is a few tens of nanometre thick (30−80 nm) is grown by dry thermal oxidation (see Fig. 5a). A pattern is then defined by electron beam lithography on a Poly Methyl Methacrylate (PMMA) resist layer (not shown in the sketches), and transferred to the top SiO_2 layer by means of a calibrated buffered HF (BHF), etc. Figure 5b shows the patterned oxide (after resist strip). The flexibility in pattern design is exploited for the definition not only of the silicon nanowire itself, but also of all the structures needed for the fabrication of the device, for example leads for interconnections, large silicon areas to be used as pads, and so on. The patterned SiO_2 top layer is used as a mask for the anisotropic etching of the top silicon layer. Even if plasma etching/Reactive Ion Etching (RIE) can be used for this process step, a simpler, cheaper and more convenient technique is wet silicon anisotropic etching in alkaline solutions [65,66], typically based on KOH (potassium hydroxide) or TMAH (tetramethylammonium hydroxide). The alkaline etching of silicon is very slow on ⟨111⟩ crystallographic directions with respect, for example, to ⟨100⟩ ones: for a typical KOH aqueous solution 35% in volume, at a temperature of 43 °C, the reaction rate ratio between ⟨111⟩ and ⟨100⟩ directions is more than 1/100. A few minutes of etching are enough to remove all of the unmasked top silicon layer that is ⟨100⟩ oriented (see Fig. 5c), meanwhile the etching is practically negligible in the ⟨111⟩ directions, and it stops on the buried oxide. Therefore, {111} crystalline planes, tilted at about 34° with respect to the vertical direction, are preserved, so that the final silicon structures have sloping walls. After the etching process step, the top SiO_2 layer can be removed (see Fig. 5d) and eventually the metal contacts for external connections can be fabricated by metal evaporation and shaped by another lithographic step (see Fig. 5e). It should be noted that metal contacts are not fabricated directly on the silicon nanowire (even if the process allows us to eventually do that), but on large silicon areas where microbonded wires can be applied for external connections. Typically, pads larger than $150 \times 150\ \mu m^2$ can be used for this purpose. The nanowire is positioned between large silicon areas which have crystalline continuity with the nanowire ends.

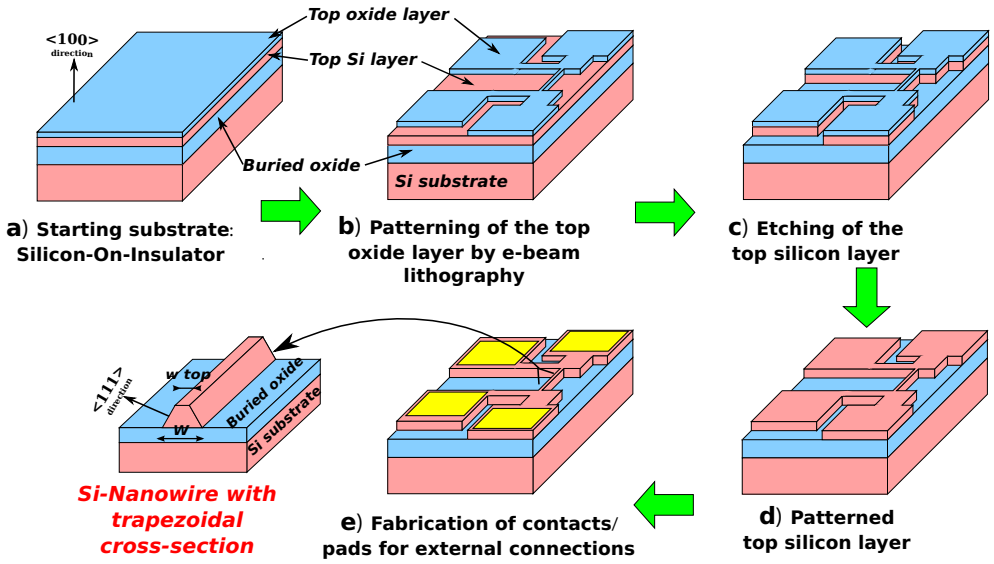

Fig. 5. Sketches of the steps of a top-down process for the fabrication of devices based on a silicon nanowire.

In this way, there is no metal/nanostructure contact, and electrical measurements are not affected by any barrier phenomena. Furthermore, it also avoids any thermal contact resistance. At the end of the etching process (see the last sketch of Fig. 5, showing a magnification of the nanowire), the nanowire has a trapezoidal cross-section, whose minor base at top is a {100} plane with a width w determined by the lithographic resolution; the sloping walls are {111} crystalline planes, where the anisotropic etching stopped; the major base at the bottom has a width W which depends on w and on the top silicon layer thickness. The main advantage in the use of silicon alkaline etching is that this trapezoidal cross-section is very uniform even on very long structures (nanowires), because they are defined by crystalline planes where the etch stops (is very slow). This high uniformity of the cross-section allows a well controllable reduction of the nanowire width by silicon oxidation, without the formation of a sausage-like structure [51,52]. Furthermore, a correct choice of the minor base width w with respect to the top layer thickness t_h allows the formation of a triangular cross section during the oxidation process because the oxidation rate is faster on the sloping sides, corresponding to {111} planes, with respect to the top plane, corresponding to a {100}. At this point, the grown silicon dioxide, with volume more than twice of the original silicon, generates a mechanical stress. As the oxidation rate is reduced by the mechanical stress, a well controlled nanowire width reduction, down to few nanometres, can be easily performed by oxidation (see Fig. 6). Figure 7 exibits SEM and AFM images of a typical device, whose active part is a silicon nanowire. The bottom left image is a low magnification SEM photo showing the aluminium pads to be used for external connections. The main SEM image shows the nanowire, carved in the top silicon layer together with silicon structures that act as leads for the electrical signal. The AFM image shows the profile of the top silicon layer, where the nanowire and the other silicon structures are carved. The three small

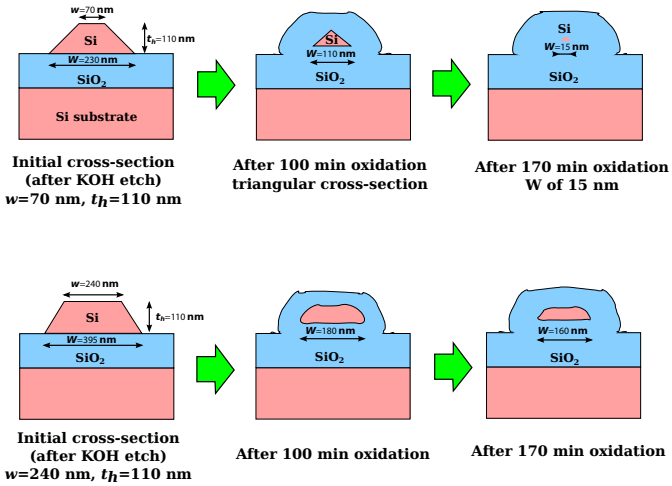

Fig. 6. Oxidation, at 1000 °C, of silicon nanowires with different cross sections. The sketches are based on numerical simulations reported in reference [52], obtained by the ATHENA process simulator. If w of the top base is smaller than t_h (see the top row), the cross-section becomes triangular and then a well controlled shrinking of the nanowire width can be performed. Conversely, an incorrect choice of w with respect to t_h (see the bottom row), does not allow a controlled reduction of the cross-section width.

SEM images in the bottom show three silicon nanowires fabricated with different oxidation times. The silicon core, which is narrower for higher oxidation times, is embedded in silicon dioxide. The silicon dioxide shroud can eventually be removed by a final BHF etch, as the nanowire can be suspended between the large silicon areas at its extremities by an underetching of the buried oxide.

This top-down process allows the reliable fabrication of nanowires 20 nm wide and more than 10 μm long. This length can be sufficient for thermoelectric generators working on a micrometric scale. However, longer

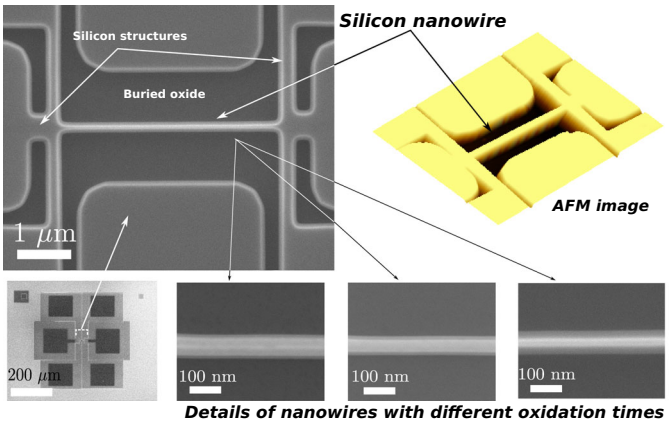

Fig. 7. SEM and AFM images of silicon nanowires. The small bottom-left image is a low-magnification SEM photo of a typical device: metal (aluminum) pads for external connections are visible. The main SEM image shows the silicon nanowire, positioned between contacts (large silicon areas), designed for electrical characterisation. The four lateral leads allow both four-contact and Hall measurements. The AFM image shows the profile of the top silicon layer. The three SEM images on the bottom show the detail of three silicon nanowires, with different oxidation times, thus with different width of the silicon core embedded in silicon dioxide.

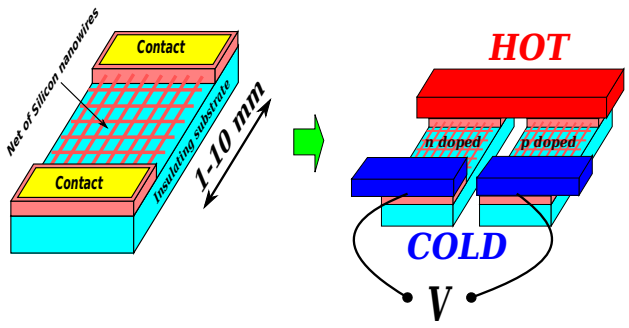

Fig. 8. (Left) A sketch of a network made of a huge number of nanowires, placed between contacts that can be several millimetres distant. (Right) A pictorial sketch of a thermoelectric generator element, made of two nanowire networks of different doping, connected in a suitable way.

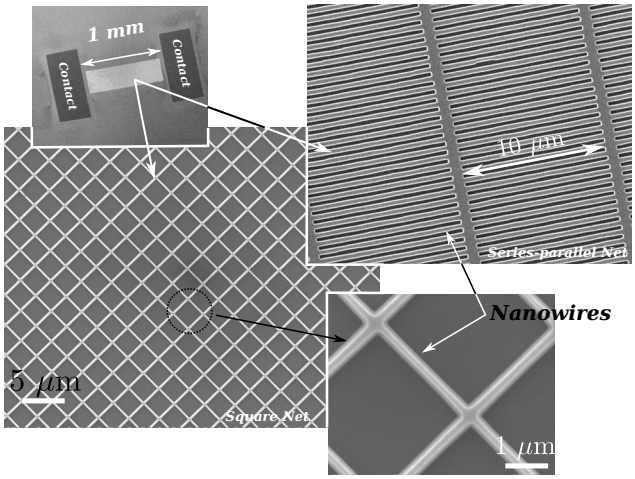

Fig. 9. SEM images of nanowire networks. In the top left a low magnification photo of a typical device is shown; the net is fabricated between two large-area pads (contacts) covered by aluminium. In the main images, two different possible net textures are shown. The main image in the middle is a SEM photo of a square net, made up of 3 μm long nanowires. A detailed close-up of a nanowire is shown in the enlargement at the bottom right. The top right image is a SEM photo of a net formed by placing several groups in series, each made up of huge number of parallel silicon nanowires 10 μm long.

nanowires are needed for maintaining a temperature gradient between macroscopic hot sources and cold sinks. Mechanical assembly of macroscopic hot-cold parts requires devices with at least millimetric dimensions. The reliable fabrication of nanowires with lengths of the order of millimetres is still beyond the capabilities of the currently available technologies. Moreover, a single silicon nanowire, even if heavily doped, cannot handle high current values because it has a very small cross section. Therefore, a thermoelectric generator must be based on a huge number of parallel, very long, nanowires. An advantage of top-down techniques is that they are very flexible as pattern design. Therefore, they can be easily adapted for the fabrication of well-organised networks, formed by a large number ($>10^5$ nanowires/mm^2) of very small nanowires [67,68]. Figure 8 (left) shows a sketch of a silicon nanowire network. The net is fabricated between two contacts, whose distance can be on the order of several millimetres. It is easy to demonstrate (see below) that this network is electrically and thermally equivalent to many parallel silicon nanowires that are several millimetres long. Therefore, it is very easy to mechanically clamp these networks, which can be either n or p doped, between the heat sources. These networks can be interconnected in a suitable way (series or parallel) as shown in the right panel of Figure 8, where the basic module of a thermoelectric generator, based on silicon nanowire networks, is represented.

Figure 9 shows SEM images of silicon nanowire networks made by top-down processing. The top left inset is an overall image of a net, fabricated between two large silicon areas covered by aluminium, that act as contacts for external connections between different networks. The two main photos show two nets fabricated with different textures. The square net (central image) is made up of nanowires 3 μm long. The inset in the right shows an enlargement of a square side, made of a nanowire 60 nm wide. The top left image shows a net made up of many groups of nanowires placed in series; each group comprises many nanowires, 10 μm long, placed in parallel (series-parallel nanonet). This second texture allows the fabrication of a higher number of nanowires: more than 10^5 nanowires, 10 μm long and narrower than 60 nm, can be fabricated within a single millimetre square.

A net of silicon nanowires is equivalent, both from the electrical and from the thermal point of view, to a resistor network, as schematically shown in the sketch of Figure 10a. If all the nanowires are intact, then the horizontal branches (parallel to the contacts) are

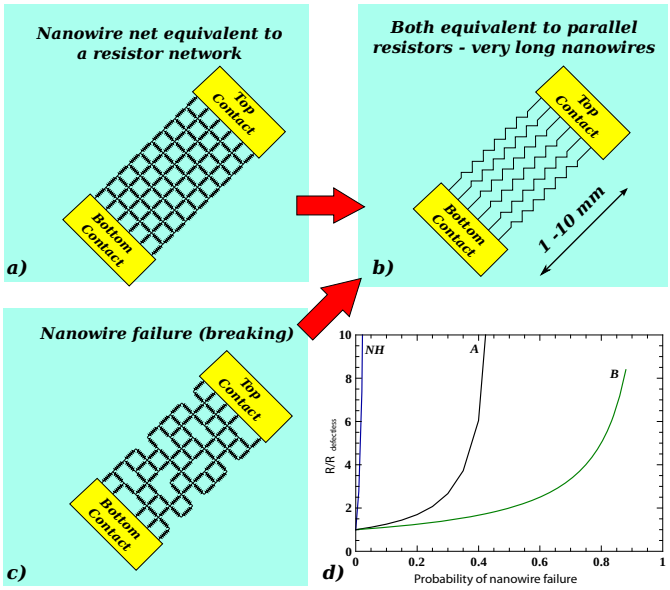

Fig. 10. (a) Electrical (or thermal) equivalent resistor network for a silicon nanowire net. (b) If all the nanowires are intact, the network is equivalent to a parallel arrangement of very long nanowires. (c) Nanowire failure can be simulated by removing resistors from the network. (d) Simulations of random nanowire failures, (see text); the reliability without horizontal connection (no horizontal, curve NH) is very low. Figure adapted with permission from reference [68], Copyright 2013 American Chemical Society.

ineffective, thus the resistor network is equivalent to the parallel arrangement of very long resistors/nanowires, as represented in Figure 10b. In reality, random nanowire failure (breaking) can happen both during the fabrication and/or during device operation (see the sketch in Fig. 10c). However, the total electrical and thermal resistivity of the network remains unchanged (or it changes only slightly) because of the high number of interconnections, due to the horizontal branches. Figure 10d shows the top-to-bottom resistance of a nanowire network, as a function of the nanowire failure probability, evaluated by Monte Carlo simulations [68]. The resistance is normalised with respect to the resistance value of the defectless network. Curve A shows the reliability of a square net; curve B, shows the reliability for the series-parallel strategy, which allows a higher number of nanowires on the same area. It can be seen that the reliability is very good, because the network resistance only doubles for a nanowire failure percentage of about 50% (one out of every two nanowires is broken). In the graph, the top-to-bottom resistance of a network without horizontal branches (curve no-horizontal, NH) is also shown as a function of nanowire failure; in this case, the reliability is very low, because even a few breaks are sufficient to compromise the overall resistance, which increases very quickly for very low nanowire failure probabilities.

Alkaline wet etching leaves very clean and smooth surfaces, and a further contribution to the smoothness arises from the oxidation process. Therefore, nanowires fabricated with these techniques are in general very smooth, and the thermal conductivity of nanowires fabricated by the top-down process, is very close to the Casimir limit [26] (see Fig. 3). However, the planar configuration of the nanowire networks makes them easy to implement and to improve the etching processes devoted to increasing the nanowire roughness. For example, several experimental works [9,24,25] have demonstrated that controlled roughness can be obtained by means of a well-calibrated metal-assisted chemical etching (see below).

Once fabricated, a SiNW net can be removed from the silicon substrate and placed on another substrate that must be a good thermal and electrical insulator. The main limitation of top-down nanowire networks is that they are made of only one thin layer of many parallel nanowires placed in a plane. The total number of parallel nanowires can eventually be increased by stacking several nets, separated by dielectric layers, on the same substrate.

A huge number of parallel nanowires can be fabricated following the principle illustrated in Figure 11. The philosophy of this top-down process is that silicon nanowires, which are perpendicular to the substrate, are carved in a bulk silicon crystalline wafer by using vertical, highly anisotropic, silicon etching. This technique has significant potential because, in principle, it allows the simultaneous fabrication of a huge number of parallel nanowires (more than 10^7 nanowires/mm^2, with diameter smaller than 100 nm), oriented perpendicular to the silicon surface (silicon pillars). The main drawback of this technique is that the silicon nanowires cannot be very long, because the aspect ratio achievable with the available processes for vertical etching is limited. Moreover, the nanowire length is also limited by the reduced mechanical stability of long and narrow structures.

Plasma etching, and in particular Deep Reactive Ion Etching (DRIE) [69] (see, for example, the review work of Wu et al. [70]), is a typical technique used in IC fabrication for achieving vertical structures with high aspect ratio. For silicon nanowire fabrication, a periodic pattern of a suitable material (metal, polymers as resist, or silicon dioxide) is defined by lithography on the top of a n or p doped silicon crystalline wafer. This pattern is then used as a mask for the deep plasma etching. Morton et al. [71] fabricated arrays of silicon nanowires (pillars) 50 nm wide and 3 μm long (aspect ratio greater than 50:1), using nanoimprinting lithography and DRIE. More recently, Zeniou et al. [72] fabricated nanowires perpendicular to the silicon substrate with aspect ratio greater than 100:1. They used electron beam lithography, or nanosphere lithography, for pattern definition and advanced DRIE processing for vertical etching. Stranz et al. [73,74] fabricated vertical SiNW arrays, with nanowire diameter between 220 and 270 nm and length of 7 μm, corresponding to the depth etch achievable with their DRIE low temperature process. They fabricated thermoelectric generators and demonstrated that the roughness induced by the DRIE process is sufficient for a good decrease in thermal conductivity. The aforementioned metal-assisted chemical

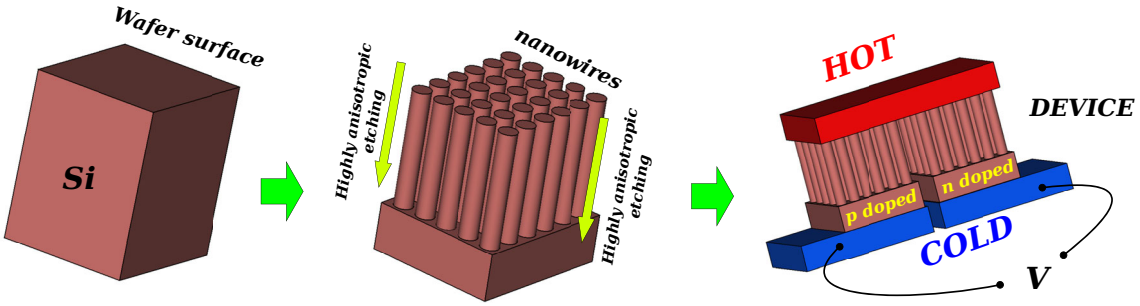

Fig. 11. Pictorial sketches of nanowires fabricated perpendicular to a silicon wafer surface, by a highly anisotropic vertical etching process.

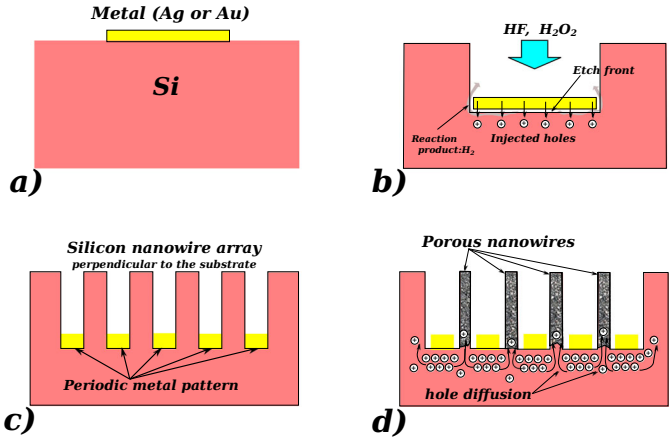

Fig. 12. Sketches showing the principle of the metal-assisted etching process. In (a) a metal is patterned on the surface of a silicon wafer. In (b), the metal acts as a catalyst injecting holes in the silicon, that then undergoes oxidative etching in the presence of HF. In (c) a periodic metal pattern is used for the fabrication of vertical nanowires. In (d) the effect of a hole generation rate that is too fast (due to excessive H_2O_2 concentration) is shown: holes diffuse toward the metal-free regions, generating undesided etching and/or porous silicon.

etching (MaCE) [75–77] technique is very promising as a valid alternative to plasma processing for vertical etching, possibly allowing higher aspect ratios (see the sketches presented in Fig. 12). It is well known that if holes are injected in silicon (electrons are withdrawn), then the silicon undergoes oxidative dissolution in a aqueous solution of hydrofluoric acid (HF). An oxidising agent in the solution, such as H_2O_2 or a metal salt (for example $AgNO_3$), can inject holes according to the reaction:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+. \quad (3)$$

However, this reaction has a very low efficiency at the silicon surface because the hole injection rate is limited by the electrochemical potential barrier between silicon and the solution. The potential barrier is lowered by an eventual metal-silicon (Schottky) junction, formed by depositing noble metals (most commonly silver or gold) on the silicon surface. The metal acts as a catalyst by injecting holes (withdrawing electrons) in the underlying silicon, according to the reaction (3). The excess of holes at the metal-silicon interface, in the presence of HF, produces a fast dissolution of silicon, while silicon on the uncovered surfaces (without metal) remains practically unetched. As for the effect of the etch at the metal-silicon interface, the metal structure sinks into the silicon (see the sketch in Fig. 12b), so that the Schottky junction is maintained and the reaction proceeds. Therefore, the metal penetrates deeper and deeper into the silicon, so that a very deep vertical trench is achieved [29,78,79]. A suitable metal patterning can be used as catalyst for the fabrication of well-ordered arrays of vertically etched silicon nanowires (see the sketch in Fig. 12c). The most critical parameter for MaCE processing is the ratio between the HF concentration, which determines the silicon oxidation/etching reaction rate, and the oxidant (H_2O_2) concentration, which determines the rate of hole generation. If the hole generation is faster than the silicon etching (i.e. H_2O_2 concentration is too high), then holes accumulate under the metal and tend to diffuse toward the metal-free regions [80]. The etch is no longer confined to beneath the metal structures, and/or porous silicon is generated around the metal patterns [78,81,82] (see Fig. 12d). Therefore, the pitch between neighbouring metal patterns must be increased to take into account the undesired etching. Moreover, vertical structures (nanowires) can become porous, with a strong degradation of their electrical conductivity. On the other hand, an excessive silicon oxidation/etching rate (due to high HF concentration) results in a non uniform etching and metal structure no longer sinks vertically. For example, metal nanoparticles [76,78,79,83] sink into the silicon following random paths, instead of taking paths perpendicular to the Si surface. A precise HF/H_2O_2 concentration rate must be found and optimised for every specific metal pattern.

Well organised metal patterns for MaCE vertical etching can be obtained by advanced e-beam lithography. For large scale applications, innovative and cheaper techniques have been developed: nanosphere lithography [84,85]; the evaporation of Au or Ag through a porous aluminum oxide membrane, yelding an almost regular pattern suitable for nanowire MaCe etching [82,86,87]. Arrays of nanowires narrower than 100 nm, and with length of the order of a few tens of micrometres, have been obtained by means of these techniques. Metal nanoparticles of gold or silver can be obtained on large surfaces without any lithographic

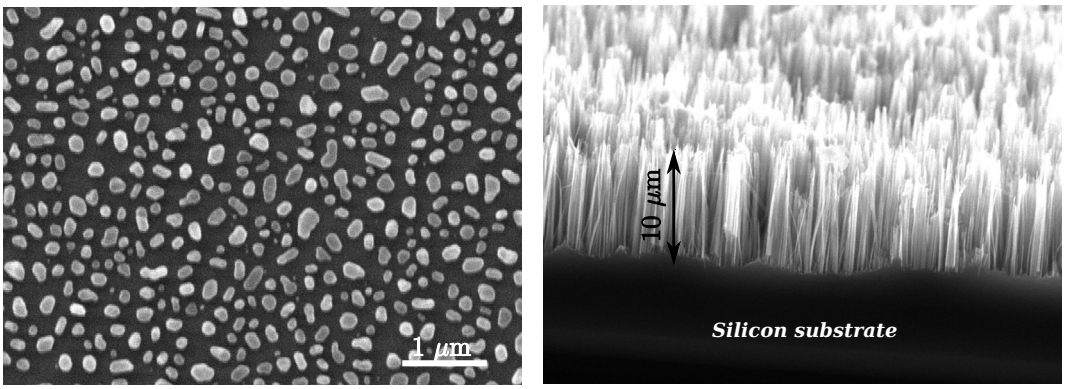

Fig. 13. (Left) SEM photo of gold nanoparticles, obtained by film deposition and thermal annealing, for MaCE nanowire definition. (Right) A forest of silicon nanowires, perpendicular to the substrate, obtained by $HF/AgNO_3$ etching.

tools by thermal treatment (annealing) of thin metal films (5−15 nm), deposited on the silicon surface by evaporation [88]. See, for example, the SEM photo on the left of Figure 13. The patterns so obtained are not very regular, and consequently MaCE etching defines vertical nanowires with random diameters. Even if the nanowires are not uniform in diameter, this technique is very interesting because it avoids the use of complex, and expensive, lithographic tools. Partial control of the average diameter of the nanowires and diameter dispersion can be obtained by optimisation of the initial metal film thickness and of the annealing time and temperature. Random metal nanoparticles can also be deposited on a surface by submerging the silicon substrate in an aqueous solution of HF and metal salts, such as $AgNO_3$ [89–92], for a very short time. MaCE can then be performed in a HF/H_2O_2 solution. As an alternative, extended immersion of a silicon substrate in an $HF/AgNO_3$ solution yields vertical silicon nanowires with random position and diameter, because $AgNO_3$ itself acts as oxidizing agent. Thus, an $HF/AgNO_3$ solution generates the metal nanoparticles that simultaneously etch the silicon. This technique is very simple because it requires only one solution for metal deposition and etching. However, the vertical silicon nanowires thus obtained have a large dispersion in terms of diameter distribution, because Ag is continuously deposited during the etch. Yen et al. [91] achieved a discrete control of the average diameter and dispersion by optimising both the $HF/AgNO_3$ concentration ratio and the reaction temperature. The SEM image on the right of Figure 13 shows a nanowire forest obtained by $HF/AgNO_3$ etching.

Improvement of the vertical etching for the fabrication of long nanowires is only one of the fundamental points that need to be addressed for the use of vertical nanowire arrays as TEGs. Another very important point is the fabrication of electrical and thermal contacts to connect the forest of silicon nanowires. The silicon substrate can be used as the bottom contact, but a metal structure into which the top of the forest can be embedded must be provided, to be used as the top contact. This is a very critical point, in light of the limited mechanical stability of narrow and long nanowires. One possible solution is to embed the vertical silicon nanowires in an insulating polymer [93,94], which first of all gives mechanical stability to the array, and moreover constrains the top of the array to a plane making it possible to perform the top deposition of a thick metal film, which can then be used as top contact. However, the polymer must be chosen carefully since it must be easy to deposit with good uniformity, and whilst simultaneously capable of withstanding the maximum working temperature of the TEG. Currently, only preliminary thermoelectric characterisation of devices based on vertical nanowire arrays has been performed [24,93–95], with very encouraging results. However, further experimental works are needed to improve the vertical etching aspect ratio, reliability and repeatability, and for improving the mechanical stability of vertical nanowires.

4 Prospective applications and future works

The limitation of phonon propagation in nanostructures due to surface scattering is a phenomenon currently under extensive investigation. Exploitation of this phenomenon could allow the use of abundant, technologically feasible and biocompatible materials with high bulk thermal conductivity, such as silicon, for thermoelectric purposes. Several experimental studies have demonstrated that the thermal conductivity of silicon nanowires can be strongly reduced by increasing the roughness of the nanowire surfaces. Surprisingly low thermal conductivity values of the order of few W/mK, well below the minimum theoretical value achievable by considering a completely diffusive surface scattering, have been measured by several groups (see Fig. 3). Conversely, the electrical resistance of nanowires wider than 20 nm is only slightly affected by surface roughness (see Fig. 2). In terms of prospective applications, the development of reliable technologies for large scale fabrication of rough silicon nanowires could make silicon competitive for thermoelectric applications with respect to other materials, such as tellurium based compounds that are rare, expensive and environmental pollutants (see Fig. 4).

Considerable experimental efforts are currently being dedicated to the development of techniques for massive top-down fabrication of silicon nanowires. Large-area nets

of silicon nanowires can be fabricated by lithography, anisotropic etching and stress-controlled oxidation in a top silicon layer of a SOI substrate. These nets are very reliable due to their high number of interconnections, and are equivalent to millimetres long, very narrow, nanowires. However, the nanowires are obtained in a very thin layer of a SOI substrate. The main point to be addressed in future works is how to increase the number of parallel nanowires that can be obtained, for example by stacking several nets on the same insulating substrate.

Highly anisotropic etching, such as plasma etching or metal-assisted etching, can be used for carving nanowires perpendicular to the surface of silicon crystalline wafers. Several millions of parallel vertical nanowires per millimetre square (i.e. a nanowire forest) can be obtained by this technique. However, at the present state of the art, the maximum length for vertical nanowires narrower than 100 nm is of few tens of micrometre (far smaller than 1 mm). Future experimental work should focus primarily on the improvement of anisotropic etching techniques, because the nanowire length relies on the achievable aspect ratio. Moreover, techniques for the fabrication of contacts on top of these nanowire forests need to be improved.

At the present state of the art, thermoelectric generators based on nanowires are very promising and can be applied to solve problems associated with energy scavenging, specifically in those applications where small amounts of electrical power (on the order of milliwatts) are required. A lot of experimental work and technological development is still required in order to make silicon-based thermoelectric generators suitable for high power applications.

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