= **REVIEWS** =

Memory Properties of SiO_x- and SiN_x-Based Memristors

V. A. Gritsenko^{*a,b,c*}, A. A. Gismatulin^{*a*,*}, and O. M. Orlov^{*d*,†}

^a Rzhanov Institute of Semiconductor Physics, Siberian Branch, Russian Academy of Sciences, Novosibirsk, 630090 Russia
 ^b Novosibirsk State University, Novosibirsk, 630090 Russia
 ^c Novosibirsk State Technical University, Novosibirsk, 630073 Russia
 ^d Molecular Electronics Research Institute, Zelenograd, Moscow, 124460 Russia
 *e-mail: aagismatulin@isp.nsc.ru

Received June 21, 2021; revised July 12, 2021; accepted July 12, 2021

Abstract—Silicon oxide and silicon nitride are the two key dielectrics used in modern silicon devices. The memory properties of SiO_x - and SiN_x -based memristors obtained by plasma-enhanced chemical vapor deposition, pyrolysis, and high-frequency reactive sputtering are reviewed. The nitrides obtained by high-frequency reactive sputtering have the best memory properties: a memory window of 10^2 , a memristor endurance of up to 10^9 cycles at the same memory window, and a memristor retention of up to 10^5 s at the same memory window.

DOI: 10.1134/S2635167621060070

CONTENTS

Introduction

1. Memristor-fabrication techniques

2. Results and discussion

2.1. Memory properties of pyrolytic silicon nitridebased memristors

2.2. Memory properties of memristors based on silicon nitride synthesized by plasma-enhanced chemical vapor and physical deposition

2.3. Memory properties of plasma-chemical silicon oxide-based memristors

Conclusions

INTRODUCTION

Development and implementation of the artificial intelligence (AI) concept are the priority directions of progress in science and technology. Among the problems to be solved by AI development is Big Data processing in cloud computing. In addition, AI and artificial neural networks are needed in machine learning and self-learning, computer vision, and voice recognition. These are tasks that represent a great difficulty for modern von Neumann-architecture computers, in which memory and information processing are physically separated, whereas the human brain solves these tasks in fractions of a second with energy consumption lower by 5–6 orders of magnitude.

AI development is occurring in three directions: (i) memory cells with multilevel (multi-bit) switching as artificial analogs of synapses in neural networks, (ii) high-speed nonvolatile energy-saving terabit flash memory that stores data for 10 years at 85°C, and (iii) universal memory combining high performance and an unlimited number of reprogramming cycles of RAM memory, nonvolatility of the flash memory, and high data capacity and low cost of magnetic hard disks. A computer based on universal memory will not need to download, as, immediately after being switched on, it will be ready to resume its operation from the very place at which it was interrupted. The speed and data capacity of universal memory-based computers will be gigantic.

A promising candidate for memory with the abovelisted characteristics is the memristor, i.e., resistive random-access memory (ReRAM). This memory is based on the reversible transition of a thin dielectric film between states with different resistances during a current pulse flow. A key challenge in the development of high-capacity ReRAM and multibit memristors is understanding the physics of the resistive switching of thin dielectric films and properties of different resistive states and searching for materials most suitable for the development of such memory [10, 11].

At present memristor memory is being developed using a wide class of materials. These are the high-permittivity dielectrics, including TaO_x [12], HfO_x [13], ZrO_x [14], TiO_x [15, 16], AlO_x [17], NbO_x [18], SiO_x [25], SiN_x [20, 21], GeO_x [22], perovskites [23, 24], and organic films [25].

In terms of the mechanism for memristor switching between the high-resistance state (HRS) and the lowresistance state (LRS), the filament model currently

[†] Deceased.



Fig. 1. HRS–LRS switching loop with 10 cycles for the Si_3N_4 -based ReRAM [31, 32].



Fig. 2. Room-temperature cycling in the MNOS memristor. The pulse length is 50 ms, the switch-on voltage is $V_{\text{set}} = 4.5$ V, the switch-off voltage is $V_{\text{reset}} = -3.5$ V, and the readout voltage is $V_{\text{read}} = 0.5$ V [6, 7].

dominates. In this model, the transition from HRS to LRS occurs via the formation of a conducting metal or semiconductor bridge. The filament diameter lies within 1-10 nm.

Amorphous silicon oxide (stoichiometric SiO₂ and nonstoichiometric SiO_x) and amorphous silicon nitride (stoichiometric Si₃N₄ and nonstoichiometric SiN_x) are the two key dielectrics in modern silicon devices. Thermal silicon oxide SiO₂ contains no traps and provides a high-quality interface with silicon. Silicon nitride, on the contrary, contains electron and hole traps in a high $(10^{19}-10^{21} \text{ cm}^{-3})$ concentration [26].

Silicon nitride exhibits the memory effect and is capable of localizing injected electrons and holes with a giant lifetime of localized electrons (10 years at 85° C). The memory effect in silicon nitride is used in modern terabit flash memory devices [27].

The advantage of silicon oxide- and nitride-based memristor memory is the technology of these materials developed in detail in modern silicon devices. This work provides a brief review of the memory properties of silicon oxide- and nitride-based memristors.

1. MEMRISTOR FABRICATION TECHNIQUES

There are several main techniques for synthesizing oxide and nitride films for silicon devices. The key technique for the synthesis of stoichiometric silicon oxide SiO_2 is the thermal oxidation of silicon in oxygen. However, such films are inapplicable as a memristor active medium, since the latter should contain oxygen vacancies acting as filament precursors. In oxide dielectric-based memristors, the active dielectric medium should be nonstoichiometric and contain oxygen vacancies in a high concentration [28].

As was shown in [29], the hydrogen plasma processing of thermal SiO_2 enriches the oxide with excess silicon, due to which it can exhibit memristive properties.

Another way to obtain the silicon-enriched nonstoichiometric silicon oxide SiO_x is plasma-enhanced chemical vapor deposition (PECVD) by the oxidation of silane in plasma.

Almost stoichiometric silicon nitride Si_3N_4 with a high concentration of Si–Si bonds [30] is obtained by the pyrolysis of a mixture of dichlorosilane SiH_2Cl_2 and ammonia NH_3 in a low-pressure reactor at temperatures in the range of 700–800°C.

Nonstoichiometric silicon nitride SiN_x enriched with excess silicon is obtained from a mixture of silane SiH₄ and ammonia NH₃ at temperatures in the range of 200–400°C by PECVD. In contrast to pyrolytic silicon nitride, plasma-chemical nitride contains Si–H and N–H hydrogen bonds in a high concentration. In this work, we discuss the memory properties of memristors based on SiN_x and SiO_x synthesized using different technologies.

2. RESULTS AND DISCUSSION

2.1. Memory Properties of Pyrolytic Silicon-Nitride-Based Memristors

The memory properties of pyrolytic siliconnitride-based memristors were studied in [31–35]. Figure 1 shows a hysteresis loop of a metal–nitride– oxide–semiconductor (MNOS) memristor with a $Si/SiO_2(2 \text{ nm})/Si_3N_4(5 \text{ nm})/Ni$ structure containing



Fig. 3. Charge storage in the MNOS memristor at 85°C in the HRS and LRS [31, 32].

a thin SiO_2 sublayer after several room-temperature switching cycles [31]. The memory window of such a memristor is about three orders of magnitude.

Figure 2 presents the dependence of the memristor window on the number of room-temperature reprogramming cycles and Fig. 3, the time dependence of the memory window of the $Si/SiO_2(2 \text{ nm})/Si_3N_4(5 \text{ nm})/Ni$ memristor at 85°C. The memristor memory does not decrease with time.

The charge transport in the Si/SiO₂(2 nm)/Si₃N₄ (5 nm)/Ni memristor was studied in the HRS and LRS at three temperatures. A quantitative analysis showed that the Frenkel effect does not describe the charge transport in a memristor in the HRS and LRS. Therefore, the mechanism of space charge-limited currents (SCLC) was analyzed. The theory of the SCLC between parallel flat electrodes was reported in [36].

The main equations of the SCLC model are

$$I = I_{\rm Om} + I_{\rm SCLC} = Se\mu n \frac{U}{d} + S \frac{9}{8} \mu \varepsilon \varepsilon_0 \theta \frac{U^2}{d^3}, \qquad (1)$$

$$n = \frac{2N_{\rm d}}{1 + \sqrt{1 + \frac{4gN_{\rm d}}{N_{\rm s}}}\exp\left(\frac{E_{\rm a}}{kT}\right)}, \quad N_{\rm s} = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2},$$

$$\theta = \frac{1}{1 + \frac{N_{\rm t}}{N_{\rm s}}}\exp\left(\frac{W_{\rm t}}{kT}\right),$$
(2)

where S is the area involved in charge transport, μ is the electron mobility, n is the density of free electrons in a dielectric, ε is the static permittivity, θ is the degree of trap filling, N_d is the donor concentration,



Fig. 4. I-V characteristics of the Si/SiO₂/Si₃N₄/Ni ReRAM in the HRS and SCLC modeling curves [31, 32].

g is the degeneracy coefficient, N_s is the effective density of states, E_a is the donor activation energy, N_t is the trap concentration, W_t is the trap energy, m^* is the electron effective mass, and h is Planck's constant.

Figure 4 shows the experimental I-V characteristics in the HRS at three temperatures and the corresponding calculations using the SCLC model. At the parameters indicated in the figure, good agreement between the experiment and theory is observed.



Fig. 5. I-V characteristics of the Si/SiO₂/Si₃N₄/Ni ReRAM in the LRS and SCLC modeling curves [31, 32].



Fig. 6. *I*–*V* characteristics of the plasma-chemical SiN_x -based p^{++} -Si/SiN_x(3.3 nm)/Ni memristor [45].

Figure 5 illustrates the experimental and calculated charge transport in the memristor in the LRS.

The SCLC model contains many parameters. To reduce the number of variable parameters, some of them were taken from the published data. The effective mass ($m^* = 0.5m_e$) and static permittivity ($\varepsilon = 7$) were taken from the values typical of Si₃N₄ [37–39]. Since the experiment showed that the MNOS memristor is not molded, in the HRS we take the parameter *S* as the entire contact ($r = 100 \mu$ m). We assume a model of the filament conductivity in the MNOS structure in the LRS, where the filament is amorphous silicon. Therefore, for the LRS case, we take the

mobility to be equal to the mobility in amorphous silicon ($\mu = 1 \text{ cm}^2/(\text{V s})$). The donor concentration determines the theoretical slope of the curve in the SCLC model at low voltages and the trap concentration determines the slope at high voltages. The *I*–*V* characteristics of the MNOS memristor in the HRS are well-described by the SCLC model with a donor concentration of $N_d = 1 \times 10^{19} \text{ cm}^{-3}$, an activation energy of $E_a = 0.91 \text{ eV}$, a trap concentration of $N_t = 5 \times 10^{18} \text{ cm}^{-3}$, and a trap energy of $W_t = 0.5 \text{ eV}$ (Fig. 6). Charge transfer occurs throughout the entire contact area and the mobility obtained using the SCLC model is $\mu = 2.5 \times 10^{-4} \text{ cm}^2/(\text{V s})$. A similar mobility value was obtained in [40].

The activation energy of donors from the SCLC model is fairly high. All this indicates that charge transfer occurs through silicon nitride. The I-V characteristics of the MNOS memristor in the LRS weakly depend on temperature; therefore, the degree of trap filling is $\theta = 1$ (Fig. 5), although the current in the ohmic section of the I-V characteristic increases with temperature, which indicates that the filament nature, is closer to semiconductor than to metal. When compared with the experiment, the SCLC model yields a donor concentration of $N_{\rm d} = 1 \times 10^{20}$ cm⁻³ and an activation energy of $E_{\rm a} = 0.06$ eV. If we take the mobility parameter analogous to that of amorphous silicon, then the effective radius of such a filament, according to the SCLC model, will be r = 50 nm. The chargetransfer mechanism and the properties of charge accumulation in the memristor strongly depend on a technique used for fabricating its active layer. The silicon oxide and nitride thicknesses are comparable with those in the MNOS from [41].

The investigated MNOS memristors do not require molding.



Fig. 7. (a) Cycling and (b) storage of data at 85°C in the plasma-chemical silicon-nitride-based p^{++} -Si/SiN_x(3.3 nm)/Ni memristor [45].



Fig. 8. I-V characteristics of the plasma-chemical silicon-nitride-based memristor in the double logarithmic scale measured in different memristor states at different temperatures; dots show the experiment and dashed lines, the SCLC modeling [20]. (a) Initial state (IS), (b) low-resistance state (LRS), (c) intermediate-resistance state (IRS), and (d) high-resistance state (HRS) of the plasma-chemical silicon-nitride-based memristor; charge transport is described by the SCLC model with different parameters.

2.2. Memory Properties of Memristors Based on Silicon Nitride Synthesized by Plasma-Enhanced Chemical Vapor and Physical Deposition

The memory properties of memristors based on plasma-chemical and physically deposited silicon nitride were studied in [42–45]. Figure 6 shows the I-V characteristic of the plasma-chemical silicon nitride-based p^{++} -Si/SiN_x(33 nm)/Ni memristor upon cycling. The memory window of the plasma-chemical nitride memristor is about an order of magnitude. Figure 7a shows cycling at room temperature and Fig. 7b, data storage at 85°C. The memristor with-stands up to 10⁴ reprogramming cycles and can store data for up to 10 years at 85°C.

Figure 8 presents the I-V characteristics of the plasma-chemical silicon nitride-based memristor in the double logarithmic scale measured at different temperatures in different memristor states [20]. According to the SCLC model, the energy of traps is 0.057 eV in the memristor initial state, 0.05 eV in the



Fig. 9. Data storage and time dependence of the memory window at 85°C for memristors based on plasma-chemical silicon nitride and silicon nitride obtained by the sputtering of a silicon-nitride target. The measured structure is p^+ -Si/SiN_x(25 nm)/ n^+ -Si [44].



Fig. 10. Dependence of the memory window on the number of cycles for memristors based on plasma-chemical silicon nitride and silicon nitride obtained by the sputtering of a silicon-nitride target in a p^+ -Si/SiN_x(25 nm)/ n^+ -Si structure [44].

LRS, 0.095 eV in the intermediate-resistance state, and 0.09 eV in the HRS. For comparison, we note that the energy of electron and hole traps in pyrolytic silicon nitride used as a storage medium in modern flash memory is 1.4 eV [32].

In [44], the memory properties of memristors based on plasma-chemical silicon nitride and silicon nitride obtained by the sputtering of a silicon-nitride target were compared (Fig. 9). The memory window in the latter is larger and more stable as compared with the parameters of pltheasma-chemical silicon nitridebased memristor. This is due to the fact that plasmachemical silicon nitride contains a large amount of hydrogen. Due to the great number of hydrogen bonds with nitrogen and silicon, which are formed during plasma-chemical synthesis, the plasma-chemical SiN_x-based memristor degrades faster than the memristor based on silicon nitride obtained by the sputtering of a silicon nitride target, where hydrogen is not used in the fabrication technology.

It can be seen in Fig. 10 that the plasma-chemical silicon nitride-based memristor withstands 10³ reprogramming cycles. The memristor based on silicon nitride obtained by the sputtering of a silicon-nitride target withstands at least 10⁵ reprogramming cycles.

Good memory properties of the memristor based on silicon nitride obtained by high-frequency reactive sputtering (Fig. 11) were demonstrated in [46]. The memristor withstands at least 10^9 reprogramming cycles without noticeable degradation and ensures stable data storage at 25 and 85°C.



Fig. 11. (a) Cycling and (b) time dependence of the memory window for the memristor based on silicon nitride obtained by high-frequency reactive sputtering in the $Ti/SiN_x(10 \text{ nm})/Pt/Ti/SiO_2/Si$ structure. The Pt electrode was grounded and the signal was supplied to the upper Ti electrode [46].

2.3. Memory Properties of Plasma-Chemical Silicon-Oxide-Based Memristors

The memory properties of plasma-chemical silicon-oxide-based memristors were studied in [47]. Figure 12a shows a high-resolution transmission-electron-microscopy image of a 130-nm-thick plasmachemical SiO_{1.1} film. The SiO_{1.1} film and SiO_{1.1}-based memristor synthesis modes were the same. The alternating dark and light stripes in the image are conductive channels formed during synthesis. The I-V characteristic in Fig. 12b confirms the presence of conducting channels, since the initial state of the memristor is highly conductive.

The trap energy in different states of the $SiO_{1.1}$ based memristor lies in the range of 0.05-0.42 eV (Fig. 13). For comparison, we note that the energies of electron [48] and hole [49] traps in silicon dioxide are 1.6 eV.



Fig. 12. Structure and storage properties of the plasma-chemical silicon-oxide-based p^{++} -Si/SiO_{1.1}(40 nm)/Ni memristor: (a) cross section of the SiO_{1.1} memory medium (the thickness is 130 nm) grown in the same modes as the SiO_{1.1}-based memristor and (b) *I*-*V* characteristic of the SiO_{1.1}-based memristor [47].



Fig. 13. (a) Si/SiO_{1.1}(40 nm)/Ni memristor structure, (b) I-V characteristic of the memristor at room temperature in different states: initial state (IS), low-resistance state (LRS), intermediate-resistance state (IRS), and high-resistance state (HRS). I-V characteristic at different temperatures in different states: (c) initial, (d) low-resistance, (e) intermediate-resistance, and (f) high-resistance [47].



Fig. 14. I-V characteristics of memristors based on (a) SiO_{0.4}, (b) SiO_{0.6}, (c) SiO_{0.7}, (d) SiO_{1.1}, (e) SiO_{1.2}, and (f) SiO_{1.8}.



Fig. 15. Charge storage in memristors based on (a) $SiO_{0.7}$, (b) $SiO_{1.1}$, (c) $SiO_{1.2}$, and (d) $SiO_{1.8}$ at a readout voltage of -1 V. Cycling of the memristors based on (e) $SiO_{0.7}$, (f) $SiO_{1.1}$, and (g) $SiO_{1.8}$ at a readout voltage of -1 V and switching voltages of +12 and -12 V.

To compare the memory properties of SiO_x -based memristors with different compositions, the I-V characteristics were measured for the first switching cycles (Fig. 14). The nonstoichiometric SiO_x films exhibit memristor properties in the range of x = 0.7-1.8.

Charge storage at 85°C in the HRS and LRS was measured for four compositions (Figs. 15a–15d). The curves were approximated up to 10 years using the charge-storage curve slope. The SiO_{1.1}-based memristor had the best charge-storage properties.

The on/off cycles were also measured for the four compositions (Fig. 15e–15g). The SiO_{1.2}-based memristor had no memory window in the pulsed mode. The SiO_{0.7}- and SiO_{1.8}-based memristors withstand $\sim 10^2$ switching cycles. The memristor based on plasma-chemical SiO_x with x = 1.1 has the best memory properties.

The best composition for a memristor is x = 1.1, taking into account the composition determination error (10%): $x = 1.1 \pm 0.1$. At the composition x < 1, the resistance in the HRS is higher than at the compositions with x > 1 due to strong enrichment in silicon; i.e., at x < 1, the memory window of the memristor is about an order of magnitude (SiO_{0.6}) or rapidly becomes about an order of magnitude (SiO $_{0,7}$). If the composition is x > 1, then the memory window in the plasmachemical SiO_x-based memristor is about two orders of magnitude. The composition with $x = 1.1 \pm$ 0.1 has the optimum silicon-to-oxygen ratio. With a decrease in the Si content in the SiO_x films, the write/read cycle resource decreases. This is apparently caused by a decrease in the number of defects due to the depletion of SiO_x films in Si.

CONCLUSIONS

The memory properties and charge-transport mechanisms in silicon-nitride- and silicon-oxidebased memristors were discussed. Such memristors provide an acceptable memory window, data storage, and number of reprogramming cycles. We note that, in contrast to memristors based on pyrolytic and plasmachemical silicon nitride, memristors based on silicon nitride obtained by physical deposition have a number of switching cycles significantly higher (10⁹) than the number of reprogramming cycles of modern flash memory (10⁴).

The charge transport in silicon-nitride- and silicon-oxide-based memristors is described by the model of space-charge-limited currents. The energies of the traps responsible for charge transport lie in the range of 0.05-0.5 eV, which is much lower than the energies of traps in silicon nitride (1.4 eV) and silicon oxide (1.6 eV).

FUNDING

This study was supported by the Russian Foundation for Basic Research, project no. 19-29-03018 (SiO_x-based memristors) and the Russian Science Foundation, project no. 19-19-00286 (SiN_x-based memristors).

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

- 1. E. M. Proidakov, Tsifrov. Ekon. 3 (3), 50 (2018).
- 2. H. Hu, Y. Wen, T.-S. Chua, and X. Li, IEEE Access. 2, 652 (2014).
- 3. J. Zakir, T. Seymour, and K. Berg, Iss. Inform. Syst. 16, 81 (2015).
- 4. F. M. Gafarov, *Artificial Neural Networks and Applications* (Kazan, Kazan, 2018) [in Russian].
- K. K. Abgaryan and E. S. Gavrilov, Inform. Primen. 14 (2), 104 (2020).
- G. S. Teplov and E. S. Gornev, Russ. Microelectron. 48, 131 (2019).
- 7. S. G. Bobkov and A. S. Basaev, *Methods and Means of Hardware for High-Performance Microprocessor Systems* (Tekhnosfera, Moscow, 2021) [in Russian].
- I. V. Ermakov and N. A. Shelepin, Izv. Vyssh. Uchebn. Zaved., Elektron. 106 (2), 31 (2014).
- J. S. Meena, S. M. Sze, U. Chand, and T.-Y. Tseng, Nanoscale Res. Lett. 9, 256 (2014).
- 10. M. A. Zidan, J. P. Strachan, and W. D. Lu, Nat. Electron. 1, 22 (2018).
- 11. D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, Nature (London, U.K.) **453**, 80 (2008).
- F. Miao, J. P. Strachan, J. J. Yang, et al., Adv. Mater. 23, 5633 (2011).
- H. Y. Lee, P. S. Chen, T. Y. Wu, et al., in *Proceedings of* the *IEEE International Electron Devices Meeting*, 2008, p. 297.
- 14. W. Y. Chang, Y. C. Lai, T. B. Wu, et al., Appl. Phys. Lett. **92**, 022110 (2008).
- 15. F. Argall, Solid State Electron. 11, 535 (1968).
- 16. D. S. Jeong, H. Schroeder, and R. Waser, Electrochem. Solid State Lett. **10**, 51 (2007).
- 17. J. Molina-Reyes and L. Hernandez-Martinez, Complexity 10, 8263904 (2017).
- T. V. Kundozerova, A. M. Grishin, G. B. Stefanovich, and A. A. Velichko, IEEE Trans. Electron Dev. 59, 1144 (2012).
- A. Mehonic, A. L. Shluger, D. Gao, et al., Adv. Mater. 30, 1801187 (2018).
- S. Kim, H. Kim, S. Hwang, and M. H. Kim, ACS Appl. Mater. Interfaces 9, 40420-7 (2017).
- 21. M. N. Koryazhkina, S. V. Tikhov, A. N. Mikhaylov, et al., J. Phys.: Conf. Ser. **993**, 012028 (2018).
- 22. A. V. Shaposhnikov, T. V. Perevalov, V. A. Gritsenko, et al., Appl. Phys. Lett. **100**, 243506 (2012).
- 23. M. H. Tang, Z. P. Wang, J. C. Li, et al., Semicond. Sci. Technol. **26**, 075019 (2011).

- X. Sun, G. Li, X. Zhang, et al., J. Phys. D: Appl. Phys. 44, 125404 (2011).
- 25. A. A. Minnekhanov, A. V. Emelyanov, D. A. Lapkin, et al., Sci. Rep. 9, 10800 (2019).
- 26. K. A. Nasyrov and V. A. Gritsenko, Phys. Usp. 56, 999 (2013).
- 27. V. A. Gritsenko, "Silicon nitride on Si: Electronic structure for flash memory devices," in *Thin Films on Si: Electronic and Photonic Applications*, Ed. by V. Narayanan (World Scientific, Singapore, 2016), p. 273.

https://doi.org/10.1142/9789814740487_0006

- 28. V. A. Gritsenko, V. Sh. Aliev, D. R. Islamov, and V. A. Voronkovskii, "A method of manufacturing an active layer for universal memory based on the resistive effect," RF Patent No. 2611580 (2017).
- V. A. Voronkovskii, T. V. Perevalov, R. M. H. Iskhakzay, et al., J. Non-Cryst. Solids 546, 120256 (2020). https://doi.org/10.1016/j.jnoncrysol.2020.120256
- V. A. Gritsenko, T. V. Perevalov, O. M. Orlov, and G. Ya. Krasnikov, Appl. Phys. Lett. **109**, 06294 (2016). https://doi.org/10.1063/1.4959830
- O. M. Orlov, A. A. Gismatulin, V. A. Gritsenko, and D. S. Mizginov, Russ. Microelectron. 49, 372 (2020). https://doi.org/10.1134/S1063739720050078
- A. A. Gismatulin, O. M. Orlov, V. A. Gritsenko, et al., Appl. Phys. Lett. **116**, 203502 (2020). https://doi.org/10.1063/5.0001950
- 33. A. A. Gismatulin, O. M. Orlov, V. A. Gritsenko, and G. Y. Krasnikov, Chaos, Solitons Fractals 142, 110458 (2021). https://doi.org/10.1016/j.chaos.2020.110458
- 34. S. Kim, S. Cho, and B.-G. Park, AIP Adv. 6, 015021 (2016). https://doi.org/10.1063/1.4941364
- 35. S. V. Tikhov, A. N. Mikhaylov, A. I. Belov, et al., Microelectron. Eng. 187–188, 134 (2018). https://doi.org/10.1016/j.mee.2017.11.002
- 36. M. A. Lampert and P. Mark, *Current Injection in Solids* (Academic, New York, 1970).

- 37. A. V. Shaposhnikov, I. P. Petrov, V. A. Gritsenko, and C. W. Kim, Phys. Solid State 49, 1628 (2007). https://doi.org/10.1134/S1063783407090041
- 38. V. A. Gritsenko, Phys. Usp. 55, 498 (2012). https://doi.org/10.3367/UFNe.0182.201205d.0531
- V. A. Gritsenko, E. E. Meerson, and Y. N. Morokov, Phys. Rev. 57, 2081 (1998). https://doi.org/10.1103/PhysRevB.57.R2081
- 40. R. Hattori and J. Shirafuji, Appl. Phys. Lett. 54, 1118 (1989). https://doi.org/10.1063/1.101478
- 41. X. F. Jiang, Z. Y. Ma, J. Xu, et al., Sci. Rep. 5, 15762 (2015). https://doi.org/10.1038/srep15762
- H.-D. Kim, H.-M. An, and T. G. Kim, Microelectron. Eng. 98, 351 (2012). https://doi.org/10.1016/j.mee.2012.07.052
- 43. H.-D. Kim, H.-M. An, and T. G. Kim, J. Appl. Phys. 109, 016105 (2011). https://doi.org/10.1063/1.3525991
- 44. T. J. Yen, A. Chin, and V. A. Gritsenko, Sci. Rep. 10, 2807 (2020). https://doi.org/10.1038/s41598-020-59838-y
- 45. A. A. Gismatulin, G. N. Kamaev, V. N. Kruchinin, et al., Sci. Rep. 11, 2417 (2021). https://doi.org/10.1038/s41598-021-82159-7
- 46. H.-D. Kim, H.-M. An, S. M. Hong, and T. G. Kim, Phys. Status Solidi A 210, 1822 (2013). https://doi.org/10.1002/pssa.201329021
- 47. A. A. Gismatulin, V. A. Voronkovskii, G. N. Kamaev, et al., Nanotechnology **31**, 505704 (2020). https://doi.org/10.1088/1361-6528/abb505
- D. R. Islamov, V. A. Gritsenko, T. V. Perevalov, et al., Appl. Phys. Lett. **109**, 052901 (2016). https://doi.org/10.1063/1.4960156
- 49. V. A. Gritsenko and H. Wong, Crit. Rev. Solid State Mater. Sci. 36, 129 (2011). https://doi.org/10.1080/10408436.2011.592622

Translated by E. Bondareva