DEVICES AND PRODUCTS BASED ON NANOMATERIALS AND NANOTECHNOLOGIES

Features of Creating Nanostructured TiO$_2$−Al$_2$O$_3$ Layers for Superdense Storage Media with an Addressing System Based on Crossbars

A. N. Belov[a,*], Yu. A. Demidov[b], D. V. Loktev[c], G. N. Pestov[a], and A. V. Solnyshkin[d]

[a] National Research University of Electronic Technology, Zelenograd, Moscow, 124498 Russia
[b] Limited Liability Company Research and Production Enterprise NanoInTech, Zelenograd, Moscow, 124489 Russia
[c] Limited Liability Company Microdatchik, Zelenograd, Moscow, 124498 Russia
[d] Tver State University, Tver, 170100 Russia
*e-mail: nanointech@mail.ru

Abstract—The results of studying the self-organization of TiO$_2$−Al$_2$O$_3$ memristive cells using the anodic oxidation of an aluminum−titanium structure are presented. Original approaches to this process make it possible to precisely control the thicknesses of the functional layers of aluminum and titanium oxides. To form the upper electrode, the use of catalytic chemical deposition is proposed, which allows the porous structure to be filled and an array of conductive buses to be organized on the surface. Measurements of the individual and group electrophysical properties of memristive cells confirm the operability of such structures as part of devices with crossbar addressing.

INTRODUCTION

Scientists around the world are showing interest in the phenomenon of resistive switching in thin metal and semiconductor films. This is due to the possibility of scaling memristive cells into a deep submicron region when using crossbar-type addressing systems [1, 2]. Another important quality is their energy independence. However, such structures containing only memristive cells between conductive buses are characterized by one big drawback: the presence of errors when reading and writing the state of a cell [3]. This is due to the flow of parasitic currents through three adjacent cells characterized by a lower electrical resistance [4]. To solve this problem, complex highly sensitive electronic processing circuits can be used; however, this negates the advantages of miniaturizing a memristive assembly. Many people use a combination of one memristor−one transistor (1T1R RRAM) to provide individual addressing [5]. However, this approach doubles the number of elements used and significantly complicates the architecture of the resulting device. More attractive is the use of combinations of one memristor−one diode (1D1R RRAM). Similar structures were proposed by researchers in 2003 to implement memory based on classical micro-integration technology [6, 7]. An interesting solution is the integration of a Schottky diode into each memristive cell [8]. This approach allows the passage of parasitic currents through adjacent cells to be avoided and ensures correct operations of writing and reading. The disadvantages are the limitation of the number of buses in the crossbar grid, as well as the difficulties when using a bipolar power supply. The most applicable method for ensuring the correct operation of a memristive crossbar is the use of diodes that operate on the effect of quantum mechanical tunneling [9]. They represent continuous dielectric layers with a thickness from 1 to 2 nm. Such layers are formed by atomic-layer deposition [10] or, for example, by magnetron sputtering [11].

Within the framework of this study, an original solution for the self-organization of memristive structures with nonlinear current−voltage characteristics (I−V characteristics) using anodic oxidation of aluminum−titanium structures is proposed. This is a simple and cheap process for producing metal oxides, which is carried out at room temperature and allows precise control of the geometry and composition of the resulting films.

EXPERIMENTAL

Ni/Al$_2$O$_3$/TiO$_2$/Ti memristive structures were formed as follows. A SiO$_2$ layer with a thickness of 0.4 μm was formed by thermal oxidation on the surface of a KDB-12 silicon wafer with the (100) orienta-
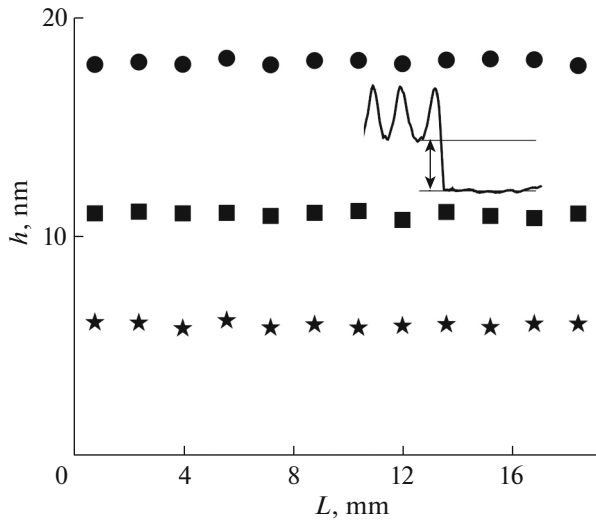
Fig. 1. Distribution of the thickness of the aluminum layer after selective removal of the oxide over the surface of the substrate.
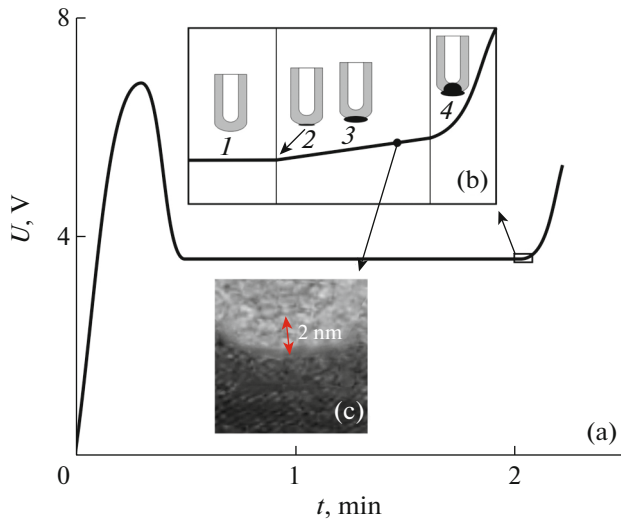
Fig. 2. Kinetic dependences of the voltage of the process of anodic oxidation of (a) two-layer aluminum–titanium structure, (b) the transition of the oxidation front across the interface, and (c) a TEM image of a two-nanometer layer of aluminum oxide.

tion. A titanium layer with a thickness of 0.3 μm was deposited on its surface using magnetron sputtering. The titanium layer was modified into an array of conductive 4-μm wide buses with contact pads using photolithography. An aluminum layer with a thickness of 2 μm was applied to the surface of the titanium buses. Anodic oxidation was carried out in sulfuric acid in the galvanostatic mode at a current density of 2 mA/cm^2. Double anodizing [12] and temperature compensation of the voltage [13] were used to order the structure, as well as to ensure the same pore shape throughout the

thickness of the oxide. Aluminum residues on the surface were removed with an etchant of copper chloride diluted in an aqueous solution of hydrochloric acid. To organize the upper conductive buses, a layer of nickel was applied to the pores of aluminum oxide and to its surface using chemical catalytic deposition. For this, the structures were sensitized for 1 min in a solution of 3 g/L of SnCl$_2$·2H$_2$O and 3 mL/L of HCl, and then activated for 3 min in a solution of 0.1 g/L of PdCl$_2$ and 0.1 mL/L of HCl. The nickel layer was deposited from an aqueous solution of NiSO$_4$ and NiCl$_2$ with the addition of sodium acetate and sodium hypophosphite. After that, the nickel layer was modified using photolithography and chemical etching into an array of conductive buses arranged perpendicular to the lower ones. The samples were examined using atomic force, transmission and scanning electron microscopies (TEM and SEM). Measurements of the electrophysical parameters were carried out using a previously created automated setup.

RESULTS AND DISCUSSION

It is known that porous ordered oxide nanostructures self-organize during the anodic oxidation of aluminum in electrolytes based on sulfuric, oxalic and orthophosphoric acids [13]. Under the same conditions, titanium and other valve metals form dense oxides [12]. Memristive layers are successfully fabricated on the basis of such oxides [14]. During the anodic oxidation of two-layer aluminum–titanium structures, the oxide of the latter penetrates into the pores of aluminum oxide and forms an array of nanowires. The mechanism of this process is described in detail in [12]. Within the framework of this work, the task was to study in detail the passage of the oxidation front through the aluminum–titanium interface. To accurately control the thicknesses of the obtained oxides, the oxidation front at any moment of the process must be parallel to the surface of the wafer, on which the functional layers are applied. This is ensured by the invariability of the main factors of anodic oxidation: voltage, current density and temperature [13]. To check the correctness of the method, the process of oxidation of aluminum deposited on the SiO$_2$ layer was carried out. Figure 1 shows the graphs of the thickness distribution of the aluminum layer over the surface of the wafer.

Figure 2 shows a schematic representation and the characteristic kinetic curves of the process including the passage of the oxidation front through the aluminum–titanium interface.

As noted above, aluminum oxidation is accompanied by constant voltage (*1*). When the oxidation front reaches the titanium surface, an increase in voltage (*2*) is observed increasing with an increase in the volume of titanium oxide (*3*). In this case, the dissolution of the barrier layer of aluminum oxide occurs [15]. The
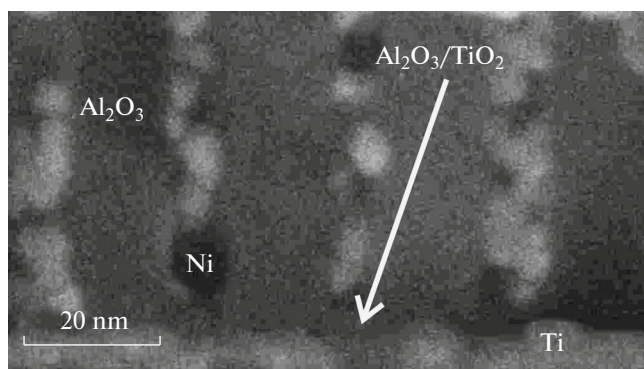
Fig. 3. SEM image of the Ni/Al$_2$O$_3$/TiO$_{2-x}$/Ti structure.

Fig. 4. (a) Current–voltage characteristic and (b) dependence of the resistive state on the number of pulses of the Ni/Al$_2$O$_3$/TiO$_{2-x}$/Ti memristive cell.

contact of the electrolyte with the titanium oxide surface also affects the behavior of the voltage curve (*4*). In fact, the ratio of the thicknesses of the layers of aluminum and titanium oxides is determined by the time when the oxidation process stops in the third stage.

Figure 3 shows a micrograph of the Ni/Al$_2$O$_3$/TiO$_{2-x}$/Ti structure. To simulate the functioning of the cells in a crossbar, four memristive cells with a contact area of 4 × 4 µm with different thicknesses of the aluminum-oxide layer were formed. It can be seen from the figure that nickel fills the porous layer of aluminum oxide and provides a stable electrical contact to the Al$_2$O$_3$/TiO$_{2-x}$ cell. The measurements were carried out both individually for each memristor and as part of a group with interconnections. Figure 4a shows the typical *I—V* characteristics of a memristive cell (*1*) without an Al$_2$O$_3$ layer and (*2*) with 2-nm- and (*3*) 8-nm-thick oxide layers. As one can see, when two-nanometer aluminum oxide appeared in the structure, the electrical resistance of the structure increased by at least an order of magnitude, while the character of the *I—V* characteristic remained unchanged on the whole. When the thickness of this layer is increased to 8 nm, the currents are units of nanoamperes, and the hysteresis loop is barely observed. Similar conclusions were reached in [9] during a detailed analysis of the potential barrier in a tunnel diode based on an ultrathin alumina film.

To test the operation of the formed structures as part of a crossbar, the resistive states of memristive cells were investigated both individually and as part of a cross connection. To increase the conductivity of the cell (potentiation), rectangular pulses of positive polarity with an amplitude of 2 V and duration of 5 µs were successively applied to it. The rising and falling fronts were 10 ns. To decrease the conductivity (depression), negative pulses were applied. To measure the current state, two pulses of different polarity were applied with a delay of 10 µs, and the magnitude of the current was measured. Figure 4b shows the characteristic dependence of the cell conductivity on the number of pulses.
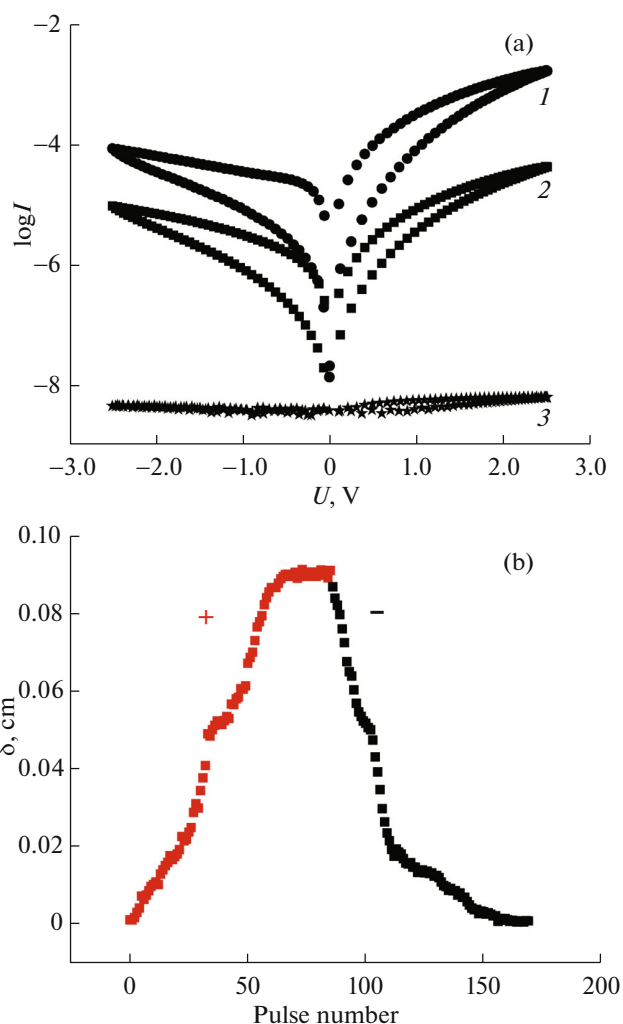
To check the stability of the states, four cells were switched to the minimum crossbar having previously written a state of ~10^{-5} S to one of them, and of 8 × 10^{-5} S in the other three. Next, 20 positive pulses were applied to the buses corresponding to the high-resistance cell and the conductivity of each one was measured separately. As a result, the conductivity of the low-resistance cells remained unchanged, while in the high-resistance cells it increased to 3 × 10^{-5} S. In the first approximation, this indicates the operation of such structures and the possibility of using them in new-generation memory devices, as well as in artificial neural networks.

CONCLUSIONS

An original method for the self-organization of a superdense storage medium containing an array of nanoscale TiO$_2$–Al$_2$O$_3$ memristive cells with an

addressing system of crossbar–conducting buses was demonstrated. The possibility of controlling the size of an ultrathin aluminum-oxide film in the process of anodic oxidation of a two-layer aluminum–titanium structure was shown. For this, the mechanism of anodic oxidation of these structures was studied in detail, in particular, at the interface between the metal layers. The method of the chemical catalytic deposition of nickel, which makes it possible to densely fill the pores of aluminum and form an upper metallization system, was proposed to be used. The results of studies of the I–V characteristics, as well as the resistive states of the cells, make it possible to confirm the operability of such systems and their applicability in nonvolatile memory devices of a new generation, as well as in artificial neural networks.

FUNDING

REFERENCES

1. M. S. Tarkov, Prikl. Diskret. Mat. Pril., No. 8, 151 (2015).

2. K. E. Nikirui, A. V. Emelyanov, V. V. Rylkov, A. V. Sitnikov, M. Yu. Presnyakov, E. V. Kukueva, Yu. V. Grishchenko, A. A. Minnekhanov, K. Yu. Chernoglazov, S. N. Nikolaev, I. A. Chernykh, M. L. Zanaveskin, and V. A. Demin, J. Commun. Technol. Electron. **64**, 1135 (2019).

3. A. Flocke and T. G. Noll, in *Proceedings of the ESSCIRC 2007 33rd European Solid-State Circuits Conference, 2007,* p. 328.
https://doi.org/10.1109/ESSCIRC.2007.4430310

4. E. Linn, R. Rosezin, C. Kugeler, et al., Nat. Mater. **9**, 403 (2010).
https://doi.org/10.1038/nmat2748

5. Chung-Cheng Chou, Zheng-Jun Lin, Pei-Ling Tseng, et al., in *Proceedings of the 2018 IEEE International Solid-State Circuits Conference, 2018,* p. 478.
https://doi.org/10.1109/ISSCC.2018.8310392

6. M. R. Stan, P. D. Franzon, S. C. Goldstein, et al., Proc. IEEE **91**, 1940 (2003).
https://doi.org/10.1109/JPROC.2003.818327

7. M. M. Ziegler and M. R. Stan, IEEE Trans. Nanotech. **2**, 217 (2003).
https://doi.org/10.1109/TNANO.2003.820804

8. F. Gül, Res. Phys. **12**, 1091 (2019).
https://doi.org/10.1016/j.rinp.2018.12.092

9. B. Govoreanu, A. Redolfi, L. Zhang, et al., in *Proceedings of the Electron Device Meeting IEDM'88,* 2013, p. 10.2.1.
https://doi.org/10.1109/IEDM.2013.6724599

10. C. Giovinazzo, C. Ricciardi, C. F. Pirri, et al., Appl. Phys. A **124**, 686 (2018).
https://doi.org/10.1007/s00339-018-2112-5

11. F. Zahari, F. Schlichting, and J. Strobel, J. Vac. Sci. Technol. B **37**, 061203 (2019).
https://doi.org/10.1116/1.5119984

12. A. N. Belov, S. A. Gavrilov, Yu. A. Demidov, and V. I. Shevyakov, Nanotechnol. Russ. **6**, 711 (2011).

13. A. N. Belov, S. A. Gavrilov, and V. I. Shevyakov, Ross. Nanotekhnol. **1** (1–2), 223 (2006).

14. V. Aglieria, A. Zafforaa, and G. Lulloa, Superlatt. Microstruct. **113**, 135 (2018).
https://doi.org/10.1016/j.spmi.2017.10.031

15. L. Berndt, M. Kleemeier, K. Thiel, et al., Int. J. Electrochem. Sci. **13**, 8867 (2018).
https://doi.org/10.20964/2018.09.11

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