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PHYSICS OF SEMICONDUCTOR DEVICES

Silicon Nanowire Parameter Extraction Using DFT and Comparative Performance Analysis of SiNWFET and CNTFET Devices

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Abstract—The performance and scalability of silicon nanowire field-effect transistor (SiNWFET) and carbon nanotube field-effect transistor (CNTFET) with surround gate geometry were studied using such tools as material exploration and design analysis (MedeA) and device modeling and simulation SilvacoTCAD. The SiNWFET and CNTFET with gate-all-around (GAA) structure offer good gate electrostatic control, high On-current and better suppression of short-channel effects with complete encirclement of the device channel. Rather than using the bulk properties of silicon, estimation of properties silicon nanowire (SiNW) was made using MedeA VASP tool based on density functional theory (DFT). In this study, the device input (I_D–V_{GS}) and output (I_D–V_{DS}) have been analyzed and parameters like threshold voltage, I_{On}/I_{Off} ratio, drain induced barrier lowering and sub-threshold slope extracted, and comparison is made between SiNWFET and CNTFET devices. The results point towards the DFT-based material parameter estimation to incorporate the quantum effects and use of SiNW/CNT-based GAA structure below 10 nm to meet scaling targets. The results suggest that the SiNWFET and CNTFET device with GAA geometry could be a better alternative to conventional MOSFETs and FinFET for numerous high-performance and low-power device applications.

Keywords: SiNWFET, CNTFET, FINFET, DFT, MedeA VASP, Silvaco TCAD

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1. INTRODUCTION

The conventional CMOS devices with planar technology face various problems with scaling down the technology for semiconductor device applications [1, 2]. The international roadmap for device and system development indicates that the fundamental limit of scaling has been reached using conventional MOSFETs [3, 4]. As the transistor count per unit area is increasing to accommodate more and more device in accordance with Moore's law, the power density and hence the power dissipation per unit area is increasing exponentially. This increase in power dissipation is like a hot plate and so severe that it may degrade the device performance or cause the complete device failure [5]. This drastic increase in power dissipation is the brick wall in the way of integrating more and more devices on the same chip/die. The scaling is to be done to minimize the power dissipation, area, cost and maximize the performance and reliability [4, 6, 7]. However, tradeoff among the different scaling and optimization parameters can be there for any device application in particular. Further, various short-channel effects in nanoscale devices hinder its optimal performance which again complicates the scaling process to meet the market requirements [8–11].

Scaling the technology nodes requires modifying the device technology and device physics to meet industry needs. The 3D silicon nanowire (SiNW) device geometry provides us many options for their usage in semiconductor industry for various applications including solar cells, storage elements, diodes and transistors [12]. Between source and drain terminal, the SiNW field-effect transistor (FET) uses a thin wire of silicon that acts as a channel responsible for current conduction. The SiNWFETs can effectively suppress the off-leakage current and provide high On-current with gate-all-around geometry, and has been good alternative device geometry for nanoscale CMOS devices [12, 13]. The CNTFET device threshold voltage V_{Th} can be given as [3, 14]:

$$V_{Th} \approx \frac{E_g}{2q} - \delta V'_{DS}, \quad (1)$$

where q is electron charge, δ is the coefficient of drain-induced barrier lowering (DIBL), $V'_{DS} = V_{DS} - I_D(R_D + R_S)$, where R_D and R_S are respective drain and source resistances of the device under consideration.

The sub-threshold swing (SS) of a FET is defined as the amount of change in input voltage needed to change the sub-threshold output current by one decade, which is given as [15]

$$\mathrm{SS} = \left(\frac{dV_{\mathrm{GS}}}{d(\log_{10} I_{\mathrm{D}})}\right), \quad (2)$$

where V_{GS} is gate–source voltage and I_{D} is drain current. Further, the increased SS indicates poor gate electrostatic control, which is primarily because of quantum mechanical tunneling of charges in the nanoscale channel [11, 16]. The conduction in SiNW is high because many conduction sub-bands contribute to the conduction with increase in gate voltage [17]. It is quite tedious to develop a compact model of SiNW device for its usage by circuit engineers, because of the reason that the device $I(V)$ characteristics of the FET using SiNW are sensitive and depend on its diameter, crystal orientation, band gap, and DoS, etc. [12]. Further, most of the TCAD tools like Silvaco's ATLAS use bulk material properties in their material library for modeling and simulation of semiconductor devices using these materials. However, the semiconductor materials could behave differently at sub-nano scale and material properties of nanowires and nanotube may be different than those of bulk, which could further influence the device performance at sub-nano scale. In this paper, the estimation of material parameters like band gap and DoS etc. using DFT has been done to incorporate the quantum effects and other properties at sub-nano scale. This technique could enhance the performance and reliability of the devices as compared to conventional MOSFETs, in which quantum and other effects have not been considered for device applications. In this work, we report DFT-based device parameter estimation and 3D TCAD simulation of GAAFETs, in which SiNW and CNT has been used as channel materials in SiNWFET and CNTFET devices, respectively.

2. THE SiNW CHANNEL MATERIAL FOR FET: AN ADVANTAGE

In this era, the device architectures are becoming more and more complex to incorporate the various features of the semiconductor device design, which demands for reliable and efficient modeling and simulation of the device to meet the industry basic or important need for various applications. In SiNWFET, a thin silicon nanowire acts as a channel that runs between source and drain regions of the device and is responsible for the current conduction in the device. The oxide material and the metal gate wrap around the channel in this device. The device structure is created by Silvaco TCAD ATLAS3D. The FETs using SiNW as a channel have certain advantages over bulk silicon planar devices for CMOS technology. First, high on-current can be expected due to quasi-one-dimension current conduction with very small angle of scattering of charge carriers [12, 18]. Second, due to the complete encapsulation of the channel by GAA structure, the off-leakage current and other short-channel effects can be effectively suppressed in SiNWFET. Third, the band structure of SiNW is quite different than that of bulk and additional sub-bands appears, which contribute to the current conduction and hence the On-current [19, 20]. Further, the existing CMOS process can be used to fabricate SiNWFET with minor tuning and developments in the process. This is one of the major advantages that minimize the risk in developing a new process technology and the cost involved in it. Also, the process steps involved in the fabrication of SiNWFET are less as there is no need of channel implantation including halo implant etc. because of its inherent feature of controlling short-channel effects due to GAA geometry [11, 18, 21, 22]. The SiNW FET with GAA configuration is expected to work in fully depletion mode, which further reduces the short-channel effects [23].

3. DFT-BASED MATERIAL PARAMETER EXTRACTION

The wave function of a many-body system by the solution of Schrödinger wave equation can be obtained by using quantum modeling density functional theory (DFT) method. The density of a system alone can be used to calculate every observable quantity of a quantum system [24]. The density of interacting particles can be calculated as the density of a system of non-interacting particles [25]. The Kohn–Sham (K–S) functional theory [25] for defining the energy of many-electron system is given as [25, 26]

$$E(n) = T_{\mathrm{s}}(n) + \int \nu(r)n(r)dr + U_{\mathrm{H}}(n) + E_{\mathrm{xc}}(n), \quad (3)$$

where n is particle density, T_{s} is kinetic energy of non-interacting particles, $\nu(r)$ is potential, $n(r)$ is density function, $U_{\mathrm{H}}(n) = 1/2\int\int \frac{n(r)n(r')}{|r-r'|}drdr'$ is classical electrostatic interaction energy approximated as Hartree energy [27], and $E_{\mathrm{xc}}(n) = \int n(r) \in_{\mathrm{xc}} (n(r))dr$ is energy due to exchange–correlation that can be estimated using various approximations. One of the versatile approximations for calculating exchange–correlation energy is generalized gradient approximation (GGA) defined as [28–30]

$$E_{\mathrm{xc}}^{\mathrm{GGA}}(n) = \int n(r) \in_{\mathrm{xc}} (n(r), \nabla n(r))d^3r. \quad (4)$$

The different GGAs have different choices of function $\in_{\mathrm{xc}}(n, \nabla n)$. The density functional for a system computation can be chosen based on the material, its properties, type of calculations, and numerical accuracy, etc. In this study, we have used GGA with Perdew–Burke–Ernzerhof (PBE), i.e., GAA-PBE functional [27, 28] for the DFT exchange-correlation. The GGA-PBE for creating projector augmented wave

(PAW) potentials is more efficient, easy to implement, and requires less computational effort than others like Perdew–Wang 1991 (PW91) [30], Becke–Lee–Yang–Parr (BLYP), local density approximation (LDA) [31], etc. and serves the purpose as well.

The MedeA tool uses a module named Vienna Ab-initio Simulation Package (VASP) as a DFT solver for investigating different properties including optical, electrical, chemical, thermal, mechanical, etc. of various materials [32–34]. This tool has been designed to compute various properties of novel materials where experimental data is scare or partly available for numerous investigations. The electrical conductivity of semiconductor material is dictated by electrical properties like band gap E_g and DoS that can be estimated using MedeA VASP tool [3, 32, 33].

The relationship between nanotube diameter and E_g can be expressed as [14, 35, 36]

$$E_g = \frac{2a_0E_{pi}}{D_{CNT}}, \quad (5)$$

where $a_0 = 0.142$ nm is the bond length of C–C atoms and $E_{pi} = 3.03$ eV is binding energy parameter for $C_{\pi-\pi}$ bond.

The DoS is the number of states present in a system and is essential to determine the concentration and distribution of carriers in semiconductor material. The effective DoS for 1D nanowire/tube can be expressed by mathematical expression as below [37–39]:

$$N_C^{1D} = \sqrt{\frac{m_e^* kT}{2\pi\hbar^2}} \text{ (for electrons)}, \quad (6)$$

$$N_V^{1D} = \sqrt{\frac{m_h^* kT}{2\pi\hbar^2}} \text{ (for holes)}, \quad (7)$$

where $\hbar = h/2\pi$, h is Plank's constant, k is the Boltzmann's constant, and m_e^* and m_h^* are effective mass of electrons and holes, respectively.

The nanowire/tube diameter that further influence the band gap of the material plays dominant role in determining the electrical conductivity of device channel so we have to be very careful to optimize the nanowire/tube diameter for the better gate control and hence the gate electrostatics of the nano scale devices for numerous applications [3, 14, 15, 22, 40, 41].

The VASP parameters were set during calculations for geometry optimization (atom positions), estimation of density of states and band structure of material. This calculation is based on DFT using GGA-PBE exchange-correlation for describing the iterations. Since no magnetic moments are in the model, this is a non-magnetic calculation with errors less than 1 meV/atom. The electronic iterations convergence (self-consistent field convergence, SCF) is 1.00E–05 eV using Normal (blocked Davidson) algorithm [42], in which several bands are optimized at the same time. The band structure contains 40 k-points. The k-spacing is 0.5 per Å, which leads to a $2 \times 2 \times 3$ mesh corresponding to actual k-spacings of $0.264 \times 0.457 \times 0.485$ per Å. The integration scheme used is first order Methfessel–Paxton smearing with a width 0.2 eV. The plane wave cutoff energy is 245.00 eV (for Si), 400.00 eV (for C).

The SiNWs and CNTs with semiconducting properties have been simulated and investigated for their use in SiNWFET and CNTFET devices. The research flow from material parameter computation to final device performance evaluation is illustrated in Fig. 1.

The DoS and band gap of SiNWs and CNTs has been estimated using MedeA VASP tool. These estimated parameters were used to define new material to model and simulate devices using SilvacoTCAD.

While extracting the parameters using DFT-based technique, a general trend of decrease in band gap with increase in diameter has been observed in both the SiNWs and CNTs. For SiNW of 1.40-nm diameter and 14-nm length, the band gap was estimated as 1.27 eV, which is slightly more than that of bulk silicon (1.1 eV) at room temperature. This increase in band gap is because of quantum phenomenon occurring at sub-nano scale. For CNTs with semiconducting properties, the decrease in threshold voltage has been observed with increase in tube chirality. The band gap also decreases with increase in the tube chirality of semiconducting CNT which results in increase of leakage current [3, 43]. The estimated material parameters for SiNW and CNT using DFT-based tool were used both in SiNWFET and CNTFET to model and simulate the device in Silvaco TCAD.

4. DEVICE STRUCTURES OF GAAFETs

The GAA SiNWFET and CNTFET devices of channel length 14 nm, stacked gate dielectric thickness 5 nm, metal gate work function 5.22 eV, and other parameters at temperature 300 K are modeled and simulated using SILVACO ATLAS3D. Both the SiNWFET and CNTFET have the same dimensions and materials except the channel material, which is SiNW in former and CNT in latter.

The device parameters used to model and simulate GAA-FETs are given in Table 1.

The GAA-FETs are modeled and simulated by Silvaco ATLAS 3D tool as illustrated in Fig. 2.

In order to enhance the numerical effectiveness and properly simulate the device behavior, boundary conforming meshing have been applied. The complete encapsulation of the SiNW/CNT channel by metal gate with GAA geometry is used for better electrostatic control and near ballistic transport of charge carriers. The concept of equivalent oxide thickness (EOT) and dielectric materials with high K are used to minimize the gate tunneling and hence the leakage [41, 44, 45]. The palladium (Pd) metal because of its process com-

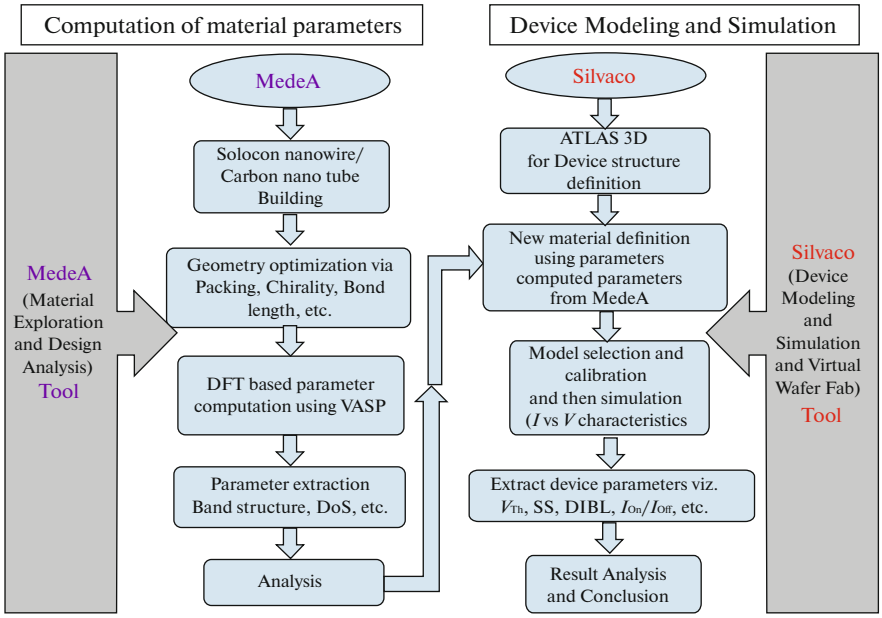

Fig. 1. The research process flow for material parameter computation and device modeling and simulation.

patibility and wettability has been used as source, drain, and gate contacts in the GAA-FET structures [17, 46]. Also, the heavily-doped source/drain n^+-regions (1E+18 cm^{-3}) for ohmic contacts and $SiO_2|HfO_2$ dielectric stack provide better coupling for optimum device performance in GAA-FETs for numerous applications.

5. THE DEVICE MODEL AND SIMULATION RESULTS

The semiconducting SiNWs and CNTs and their usage in GAA-FETs have been investigated in this research. The Silvaco TCAD device simulator has been used to model semiconductor devices and study the charge transport mechanism in these devices. The

Table 1. The parameters used in structure definition and simulation of GAA-FET devices

GAA-FETs		
Device parameters	Brief description	Values
L	Channel length	14 nm
D_C	Channel diameter	1.40 nm
E_g	Band gap	1.21 eV (SiNW), 0.61 eV (CNT)
DoS (N_C)	Density of states in CB	9.28E+12 cm^{-2}/eV (SiNW), 8.88E+20 cm^{-2}/eV (CNT)
DoS (N_V)	Density of states in VB	8.54E+12 cm^{-2}/eV (SiNW), 7.36E+20 cm^{-2}/eV (CNT)
T_{oxi}	Inner oxide thickness (SiO_2)	2 nm
K_{oxi}	Inner oxide dielectric constant	3.9
T_{oxt}	Stacked outer gate oxide (HfO_2) thickness	3 nm
K_{oxt}	Stacked outer gate oxide dielectric constant	25
N_{SD}	S/D doping	1E+18 cm^{-3}
E_{ea}	Electron affinity	4.7 eV (SiNW), 3.2 eV (CNT)
Φ_m	Metal gate work function	5.22 eV
T	Temperature	300 K

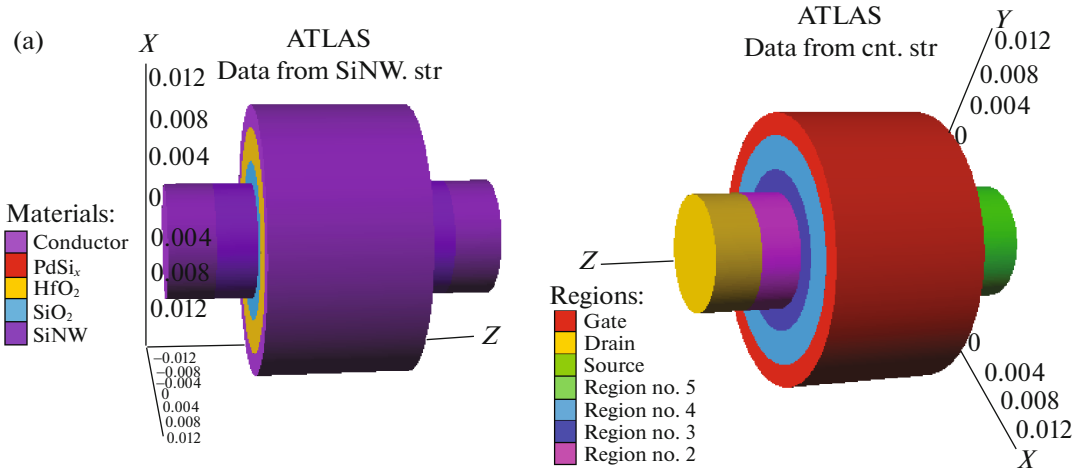

Fig. 2. Cylindrical ($\Theta = 360°$) gate-all-around FETs modeled by Silvaco ATLAS 3D, SiO_2–HfO_2 dielectric stack, Pd as contacts metal, (a) GAA-SiNWFET structure; (b) GAA-CNTFET depicting different regions of the device.

drift–diffusion (D–D) model is the simplest and adequate for studying charge transport mechanism in conventional semiconductor devices. The current equations in the D–D model are given as [47]

$$\mathbf{J}_n = qD_n\nabla n - qn\mu_n\nabla\psi - \mu_n n(kT_L\nabla(\ln n_{ie})) \text{ (for electrons)}, \quad (8)$$

$$\mathbf{J}_p = -qD_p\nabla p - qp\mu_p\nabla\psi + \mu_p p(kT_L\nabla(\ln n_{ie})) \text{ (for holes)}, \quad (9)$$

where ψ is wave function, T_L is lattice temperature, μ_n, D_n and μ_p, D_p are the mobility's and diffusion coefficient of electrons and holes respectively, and n_{ie} is effective intrinsic concentration.

However, the advanced models are in demand for modeling and simulation of short-channel devices for incorporating the various effects at sub nano-scale. The Silvaco's ATLAS TCAD tool incorporates both the D–D and advanced transport models for modeling and simulating 3D devices with different silicon/non-silicon and planar/non-planar geometries [48]. The quantum effects in the semiconductors are included and implemented in Silvaco's ATLAS TCAD tool by modifying the D–D transport equations with the position-dependent Bohm quantum potential (BQP). In BQP model, the current expressions (8) and (9) can be modified as [3, 49]

$$J_n' = qD_n\nabla n - qn\mu_n\nabla(\psi - Q) - \mu_n n(kT_L\nabla(\ln n_{ie})) \text{ (for electrons)}, \quad (10)$$

$$J_p' = -qD_p\nabla p - qp\mu_p\nabla(\psi - Q) + \mu_p p(kT_L\nabla(\ln n_{ie})) \text{ (for holes)}. \quad (11)$$

In expression (10) and (11), Q represents the BQP and can be given as [3, 49]

$$Q = -\frac{\hbar^2}{2}\frac{\gamma\nabla[\mathbf{M}^{-1}\nabla(n^\alpha)]}{n^\alpha}, \quad (12)$$

where $\hbar = h/2\pi$ is the Dirac constant, n is density of carriers (electrons/holes), $\mathbf{M}$ is effective mass tensor. This model provides us a flexibility to calibrate and set the values of γ and α as fitting parameters which increases its accuracy and numerical stability. Further, this BQP model has better convergence properties and can be used for 1D, 2D and 3D device geometries. In this research, this BQP model and parameter estimation using novel DFT-based technique to incorporate the quantum and other sub-nano scale effects has been used for modeling and simulation of GAA-FETs for low-power and high-performance applications.

5.1. The I(V) Performance of GAA SiNWFET

The modeled device has been investigated via $I(V)$ characteristics. The input (I_D–V_{GS}) and output (I_D–V_{DS}) of GAA SiNWFET device are illustrated in Fig. 3.

The device operating at 0.8 V gives drain current 155.8 μA, high On-current I_{On} 56 μA, and very low Off-current I_{Off} (2.87 pA). The device with GAA structure shows better device performance as compare to conventional MOSFET devices.

The GAA-SiNWFET exhibits threshold voltage V_{Th} = 0.24 V, DIBL = 74 mV/V, I_{On}/I_{Off} ratio = 1.95E+07, and SS = 83 mV/dec.

5.2. The I(V) Performance of GAA CNTFET Device

The input (I_D–V_{GS}) and output (I_D–V_{DS}) characteristics device are illustrated in Fig. 4.

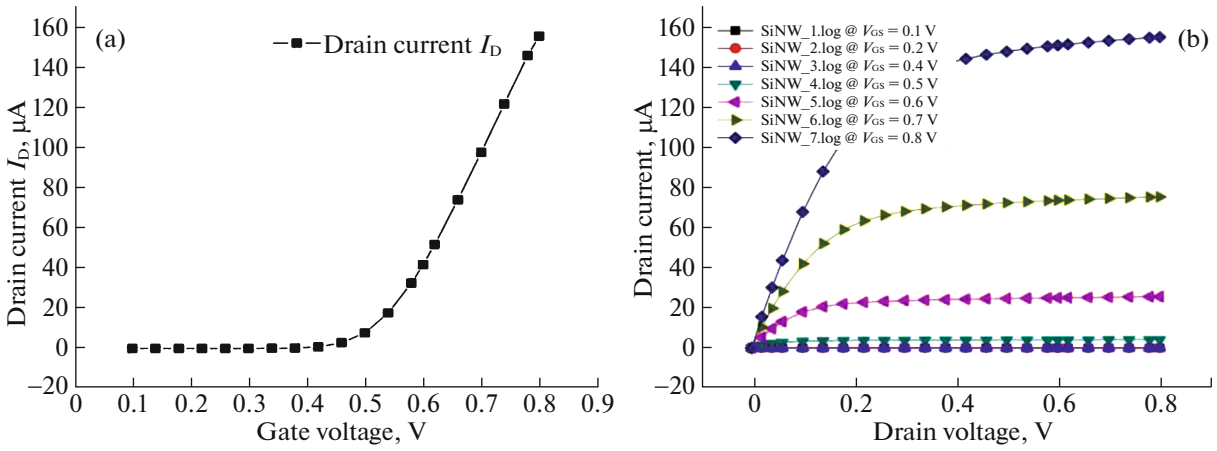

Fig. 3. The $I(V)$ characteristics of GAA SiNWFET. (a) Input characteristics I_D versus V_{GS} at V_{DS} = 0.8 V; (b) Output characteristics I_D versus V_{DS} at different gate voltages V_{GS}.

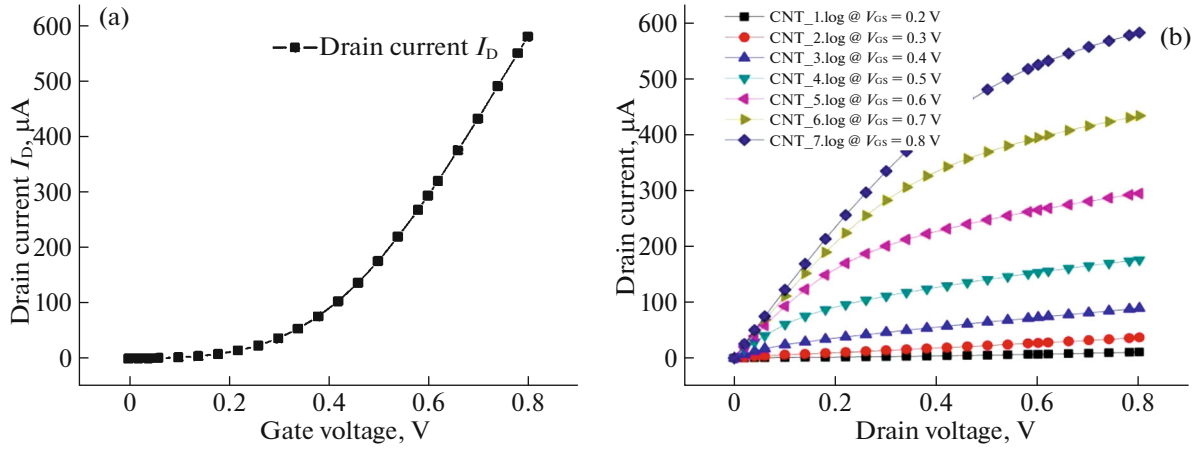

Fig. 4. Input and output performance of GAA CNTFET. (a) Input characteristics I_D versus V_{GS} at V_{DD} = 0.8 V; (b) Output characteristics I_D versus V_{DS} at different gate voltages V_{GS}.

The device operating at voltage $V_{DS} = V_{DD} = 0.8$ V gives drain current 582 μA and high I_{On}/I_{Off} ratio and exhibits better performance than conventional MOSFETs and even FinFETs. The GAA-CNTFET exhibits V_{Th} = 0.26 V, DIBL = 66 mV/V, I_{On}/I_{Off} ratio = 4.46E+06 and SS = 72 mV/dec. The device $I(V)$ characteristic shows that drain current in GAA CNTFET is greater than that of GAA SiNWFET; this is due to ballistic transport of charge carriers through the CNT as channel in CNTFETs. However, high I_{On}/I_{Off} ratio of SiNWFET as compared to CNTFET is due to better suppression of off-leakage and quantum confinements in silicon nanowire devices with surround gate geometry. The results of our research work have also been compared for their performance parameters with the published work as reported [3, 12, 16, 46, 50].

6. CONCLUSIONS

The scaling needs and performance enhancement goals envisaged in the IRDS roadmap were kept in mind to model and simulate GAA SiNWFET and GAA CNTFET devices. The parameters obtained using DFT-based simulator MedeA VASP were used for modeling and simulation of GAA-FET structures in SilvacoTCAD. The devices using the GAA geometry exhibits lower SS, increased V_{Th}, lower sub-threshold leakage and better I_{On}/I_{Off} ratio. The novel devices such as silicon nanowire field-effect transistors (SiNWFETs) and CNTFETs with GAA structure with their quasi-ballistic charge transport could be better choice for scaling the technology and to minimize short-channel effects for future semiconductor technology beyond 2025. Even though CNTFET gives better performance in terms of DIBL and SS, etc.

However, SiNWFET does not involve major changes in the existing process technology and is better than the conventional MOSFETs. The results point towards the DFT-based material parameter estimation to incorporate the quantum effects and use of SiNW/CNT-based GAA structure below 10 nm to meet scaling targets for ultralow power and robustness for high-performance applications.

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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