Analytical Drain Current Modeling and Simulation of Triple Material Gate-All-Around Heterojunction TFETs Considering Depletion Regions

C. Usha[a],* and P. Vimala[a]

[a] *Department of Electronics and Communication, Dayananda Sagar College of Engineering, Bangalore, Karnataka, India*
*e-mail: usha.chintu.dec14@gmail.com

Abstract—This paper deals with electrostatic behavior of triple-material gate-all-around hetero-junction tunneling field-effect transistors (TMGAA-HJTFET) device. The model is advantageous in apprehending a comparative study with the single-material gate-all-around hetero-junction tunneling field-effect transistors (SMGAA-HJTFET) in terms of surface potential, electric field, drain current, transconductance, and threshold voltage. The surface-potential distribution in partition regions along the channel is solved by using two-dimensional Poisson's equation. By using the drift and diffusion current, drain current is derived, and I_{On}/I_{Off} ratio of 10^{11} is gained from analytical modeling and TCAD simulation. Transconductance and threshold voltage are derived from the tunneling current. The proposed model results are validated by the ATLAS TCAD simulation tool.

1. INTRODUCTION

Tunnel field-effect transistors (TFETs) have drawn attention of semiconductor academic researchers and industry for their loftier performance in subthreshold region. TFET devices operate based on band-to-band tunneling principle, which significantly improves the switching of On and Off states at lower voltages. Compared with the metal oxide–semiconductor field-effect transistor (MOSFETs), TFETs has low subthreshold swing (i.e., below 60 mV/dec), high I_{On}/I_{Off} ratio, low Off-state current, low leakage power consumption, and better immunity of short-channel effects [1–3]. The On-current performance of the TFET device is low due to small tunneling efficiency of electrons in larger band gap than the conventional MOSFET devices [4]. Thus, to improve On-current performance many device models are proposed and analytically explored. Based on source, depletion charge and mobile charges are analyzed for the device double-gate TFET (DG-TFET) [5, 6]. Gate engineering with materials having different work function contributed significant control over short-channel effects, some studies dealt with dual material and triple material [7–10] in recent years.

Gate-all-around nanowire TFETs lead to steeper subthreshold slope due to high-level control of gate as field lines get originated from the drain that can't penetrate into the channel, and get terminated at the gate [11, 12]. Nanowire TFETs with efficient gate along with channel engineering of different work function materials are proposed to improve the On-current performance; steep subthreshold slope, reduced DIBL, and threshold voltage roll-off [13–15]. Hetero-junction TFETs lead to increased On-drain current performance due to shorter tunneling width at source-to-channel junction [16]. The electrostatic parameters such as channel potential, electric field, drain current using band-to-band tunneling generation rate, and shortest channel length, transconductance, and threshold voltage of SiO_2|high-k stacked DG-TFET by considering the depletion regions. High-k is stacked over SiO_2 assumed as the dielectric to avoid the lattice mismatching between silicon and high-k dielectric below the gate electrode [17].

Furthermore, it has been analyzed that I_{On} current performance can be improved using the nanowire device. Hence, in this view, the proposed device TM GAA-HJTFET has been modeled by using three different materials gate engineering as different regions along with depletion regions. This paper captures the salient features such as surface potential derived from Poisson's equation using parabolic approximation method, electric field, drain current using Kane's Model, transconductance, and threshold voltage.
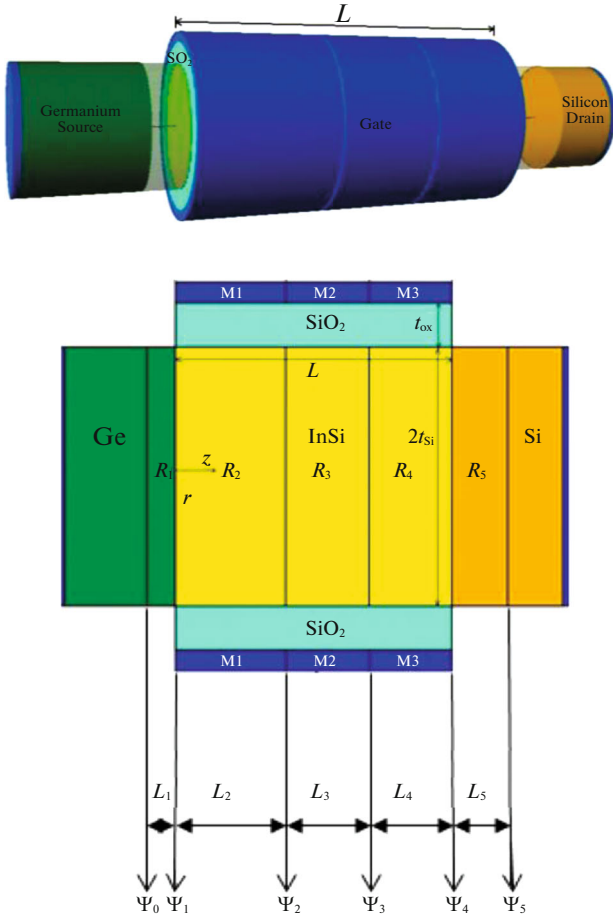
Fig. 1. 3D structure of triple-material GAA-HJTFET and schematic cross-sectional view of triple-material GAA-HJTFET.

2. DEVICE STRUCTURE

Figure 1 represents the three dimensional structural view of Triple Material GAA-HJTFET (TMGAA-HJTFET).

Source length of 20 nm and material used is germanium with a doping concentration of $N_1 = 1 \times 10^{20}$ cm^{-3}, channel length is 50 nm with a doping concentration of $N_2 = 1 \times 10^{16}$ cm^{-3}, drain length is 20 nm and material used is silicon with doping concentration of $N_3 = 5 \times 10^{18}$ cm^{-3}, which is assumed in this model. In the cross-sectional schematic view of the TMGAA-HJTFET device, regions are considered for depletion regions and the three materials used for gate which are represented as R_1, R_2, R_3, R_4, and R_5 with respective lengths of L_1, L_2, L_3, L_4, and L_5.

3. MODEL FORMULATION

For analytical modeling, the cross-sectional schematic view of TMGAA-HJTFET is considered due to its potential distribution in r-direction which is same

as the DG-TFET shown in Fig. 1. z and r quantities are considered along the channel length; other parameters include oxide thickness (t_{ox}). Silicon thickness ($2t_{Si}$), work functions of three materials (ϕ_{m1}, ϕ_{m2}, ϕ_{m3}). ψ_0, ψ_1, ψ_2, ψ_3, ψ_4, and ψ_5 are the junction potentials are $z = 0$, $z_1 = L_1$, $z_2 = L_1 + L_2$, $z_3 = L_1 + L_2 + L_3$, $z_4 = L_1 + L_2 + L_3 + L_4$, and $z_5 = L_1 + L_2 + L_3 + L_4 + L_5$.

3.1. Analytical Modeling of Surface Potential

The surface potential distribution function along the channel regions R_i is considered as $\psi_i(r, z)$, where $i = 1, 2, 3, 4, 5$. The two-dimensional (2D) Poisson's equation for the gate-all-around is given as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z)}{\partial r}\right) + \frac{\partial^2 \psi_i(r,z)}{\partial z^2}$$
$$= -\frac{qNi}{\varepsilon_{Si}}, \quad i = 1,2,3,4,5. \tag{1}$$

The doping concentrations of source ($N_{Src} = 1 \times 10^{20}$ cm^{-3}), channel ($N_{Ch} = 1 \times 10^{16}$ cm^{-3}), and drain ($N_2 = 5 \times 10^{18}$ cm^{-3}) are assumed, respectively, to improve the I_{On}/I_{Off} current ratio. q is the electron charge and ε_{Si} is the silicon permittivity. 2D potential distribution $\psi_i(r, z)$ in region R_i can be approximated using parabolic approximation method given as

$$\psi_i(r,z) = a_{0i}(z) + a_{1i}(z)r + a_{2i}(z)r^2,$$
$$\text{where} \quad i = 1,2,3,4,5. \tag{2}$$

$a_{0i}(z)$, $a_{1i}(z)$ and $a_{3i}(z)$ are arbitrary functions of z, defined by the boundary conditions [18]:

$$1. \ \psi_i(r,z)|_{r=R} = \psi_s(z), \tag{3}$$

$$2. \ \frac{\partial \psi_i(r,z)}{\partial r}\bigg|_{r=0} = 0, \tag{4}$$

$$3. \ \frac{\partial \psi_i(r,z)}{\partial r}\bigg|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}R}\left[\frac{\psi_G - \psi_s(z)}{\ln\left(1 + \frac{t_{ox}}{R}\right)}\right], \tag{5}$$

where $\psi_G = V_{GS} - \phi_m + \chi + E_g/2$ and $i = 1, 2, 3, 4, 5$ for five different regions, gate work function $\phi_{m1} = 4.05$ eV (Zr), $\phi_{m2} = 4.2$ eV (Al), and $\phi_{m3} = 4.6$ eV (Cu), electron affinities χ of 4.0 eV (Ge) and 1.12 eV (Si), energy band gaps E_g are 0.67 eV (Ge) and 1.12 eV (Si), V_{GS} is the gate-to-source voltage, t_{ox} is the oxide thickness, t_{Si} is the silicon thickness ($R = t_{Si}$), and ε_{ox} is the silicon dioxide permittivity.

Using Eq. (3) to solve Eq. (5), we obtain

$$a_{0i} = \psi_s(z) - \frac{\varepsilon_{ox}}{2\varepsilon_{Si}}\left[\frac{\psi_G - \psi_s(z)}{\ln\left(1 + \frac{t_{ox}}{R}\right)}\right], \tag{6}$$

$$a_{1i} = 0, \tag{7}$$

$$a_{2i} = \frac{\varepsilon_{ox}}{2\varepsilon_{Si}R^2}\left[\frac{\psi_G - \psi_s(z)}{\ln\left(1 + \frac{t_{ox}}{R}\right)}\right]. \tag{8}$$

The channel potential $\psi_i(r, z)$ and surface potential $\psi_{s,i}(z)$ are related as $\psi_{s,i}(z) = \psi_i(\pm t_{Si}/2, z)$.

From Eqs. (6)–(8), we can deduce that

$$\psi_i(r, z) = \psi_{0i}(z) + \left(\frac{r^2}{\lambda^2 R^2} - \frac{1}{\lambda^2}\right)(\psi_G - \psi_{0i}(z)), \tag{9}$$

$$\psi_{s,i}(z) = \psi_{0i}(z) + \left(\frac{t_{Si}^2}{4\lambda^2 R^2} - \frac{1}{\lambda^2}\right)(\psi_G - \psi_{0i}(z)), \tag{10}$$

where $\psi_{0i}(z) = \psi_i(0, z)$, i.e., when radius $r = 0$.

At $r = 0$, 2D Poisson's equation (1) is written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r, z)}{\partial r}\right)\bigg|_{r=0} + \frac{\partial^2 \psi_i(r, z)}{\partial z^2}\bigg|_{r=0} = -\frac{qN_i}{\varepsilon_{Si}}\bigg|_{r=0}. \tag{11}$$

Substituting Eq. (2) in Eq. (11), differential equation is gained in terms of center potential as

$$\frac{\partial^2 \psi_{0i}(z)}{\partial^2 z} - \eta_i^2 \psi_{0i}(z) = -\eta_i^2 P_i, \tag{12}$$

where

$$P_i = \frac{qN_i}{\eta_i^2 \varepsilon_{Si}} + \psi_G,$$

and $\eta_i^2 = \dfrac{4}{\lambda^2 R^2}$.

The general solution of Eq. (12) is

$$\psi_{0i}(z) = A_i \exp(\eta_i(z - z_{i-1})) + B_i \exp(-\eta_i(z - z_{i-1})) + P_i, \tag{13}$$

where

$$A_i = \frac{1}{2\sinh\eta_i L_i}[\psi_{i-1}(z)\exp(-\eta_i L_i) - \psi_i(z) - P_i(\exp(-\eta_i L_i) + 1)], \tag{14}$$

$$B_i = \frac{1}{2\sinh\eta_i L_i}[\psi_{i-1}(z)\exp(\eta_i L_i) - \psi_i(z) - P_i(\exp(\eta_i L_i) + 1)], \tag{15}$$

$L_i = z_i - z_{i-1}$ is the length of region R_i ($i = 1, 2, 3, 4, 5$) and $i = \psi_{s,i}(z_i)$ is surface potential at $z = z_i$ as shown in Fig. 1. By applying the boundary conditions, the surface potential across the regions is obtained [18]

$$\psi_0 = \psi_1(r, 0) = V_{bis}, \tag{16}$$

$$\psi_5 = \psi_5(r, L_1 + L_2 + L_3 + L_4 + L_5) = V_{bis} + V_{DS}, \tag{17}$$

where

$$V_{bis} = -\frac{1}{q}[(\chi_1 - \chi_2) + 0.5(E_{g1} - E_{g2}) + qV_T\ln(N_1/n_i)]$$

is built-in potential.

ψ_0, ψ_1, ψ_2, ψ_3, and ψ_4 are intermediate surface potentials obtained by using continuity of lateral electric field property such as [18]

$$\psi_{s,i}(z)\big|_{z=z_i} = \psi_{s,i+1}(z)\big|_{z=z_i}, \tag{18}$$

$$\frac{\partial \psi_{s,i}(z)}{\partial z}\bigg|_{z=z_i} = \frac{\partial \psi_{s,i+1}(z)}{\partial z}\bigg|_{z=z_i}. \tag{19}$$

Using Eqs. (18) and (19) in (10) along with (13)–(15), we obtain the intermediate potentials

$$\psi_i = \frac{1}{y_i}\left[\frac{(x-1)}{\sinh\eta iLi}\{\eta_i\psi_{i-1} + \eta_i P_i(1 + \cosh\eta_i L_i) - P_{i+2}\sinh\eta_i L_i\} + x\psi_G\right], \tag{20}$$

where

$$x = \left(\frac{t_{Si}^2}{4\lambda^2 R^2} - \frac{1}{\lambda^2}\right),$$

$$y_i = \lfloor 1 - \eta_i(x-1)\coth\eta_i L_i\rfloor, \quad i = 1, 2, 3, 4.$$

3.2. Modeling of Electric Field

The vertical and lateral electric field $E_{ri}(r, z)$ and $E_{zi}(r, z)$ are obtained by differentiation of potential Eqs. (2) and (13)

$$E_{ri}(r, z) = 2ra_{2i}(z), \tag{21}$$

$$E_{zi}(r, z) = -\frac{\partial \psi_i(r, z)}{\partial z} = \eta_i[-A_i\exp(\eta_i(z - z_{i-1})) + B_i\exp(-\eta_i(z - z_{i-1}))]. \tag{22}$$

3.3. Lengths of Depletion Regions

The lengths of regions R_1 and R_5 denoted as L_1 and L_5 can be calculated by $E_r = 0$ at $r = r_0$ and $r = r_2$ before deriving potentials ψ_2 and ψ_3. Due to the complexity of the calculations, simple approximation can be done separately by considering source–channel and drain–channel regions shown below using [18] and [20]

$$L_1 = \sqrt{2\varepsilon_{Si}(P_2 - \psi_0)/(qN_1)}, \tag{23}$$

$$L_5 = \sqrt{2\varepsilon_{Si}(\psi_5 - P_2)/(qN_3)}. \tag{24}$$

Since P_2 is dependent on V_{GS}, L_1 and L_5 values are smaller than the DG-TFET and also dependent on V_{GS}.

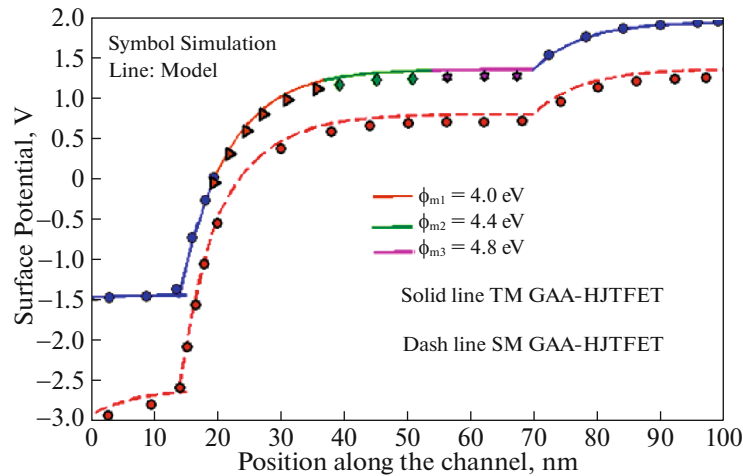

Fig. 2. Comparision of surface potential distribution $\psi_{s,i}$ along the lateral length of the channel (z) for TM GAA-HJTFET with SM GAA-HJTFET at $V_{DS} = 1$ V.
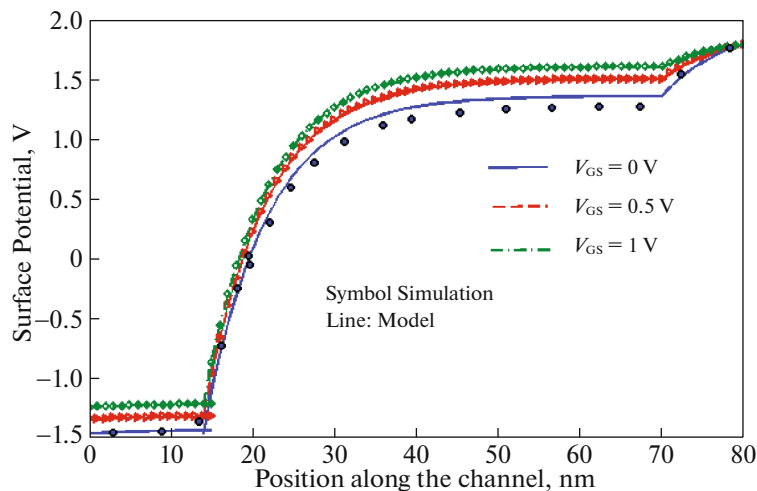

Fig. 3. Surface potential distribution $\psi_{s,i}$ along the lateral length of the channel (z) for different $V_{GS} = 0$, 0.5, and 1 V at $V_{DS} = 1$ V.

tance, and threshold voltage are validated by using the TCAD SILVACO tool. The procedure followed to obtain the results for the device simulation is (1) Defining mMesh points with spacing, (2) Defining regions, (3) Defining physics models, (4) Defining method of solution (Newton), (5) Defining bias voltages (gate and drain voltages), 6) Extracting and plotting the data. The following models are used in defining physics models: BOLTZMANN, FERMI, BGN, CONMOB, CVT, SRH, CONSRH, IMPACT SELB, BBT.STD, KANE, and BBT.KL.

Figure 2 shows the surface potential distribution along the channel comparision plot, the surface potential of TM GAA-HJTFET is high compared to the SM GAA-HJTFET, we observe that the tunneling width across the source–channel junction is less for TM GAA-HJTFET.

Thus, the surface potential gets increased due to increase in the tunneling rate of electrons at source–channel junction.

Figure 3 represents the surface potential distribution along the channel for different gate biases at $V_{DS} = 1$ V.

It is observed that when gate bias is applied, surface potential from the source increases linearly and becomes steeper with increase in biasing due to decrease in the tunneling width of the source channel junction. Linear increase at the source channel junction improves the electric field and band-to-band tunneling generation rate.

Figure 4 depicts the surface potential variation along the channel for drain control regime at $V_{GS} = 1$ V, it is studied that increase in drain to source voltage
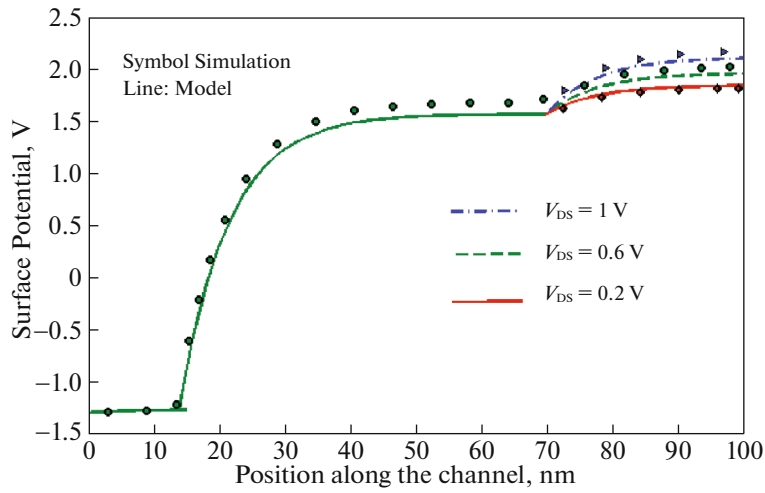
Fig. 4. Surface potential distribution along the channel for different V_{DS} = 0.2, 0.6, and 1 V at V_{GS} = 1 V.
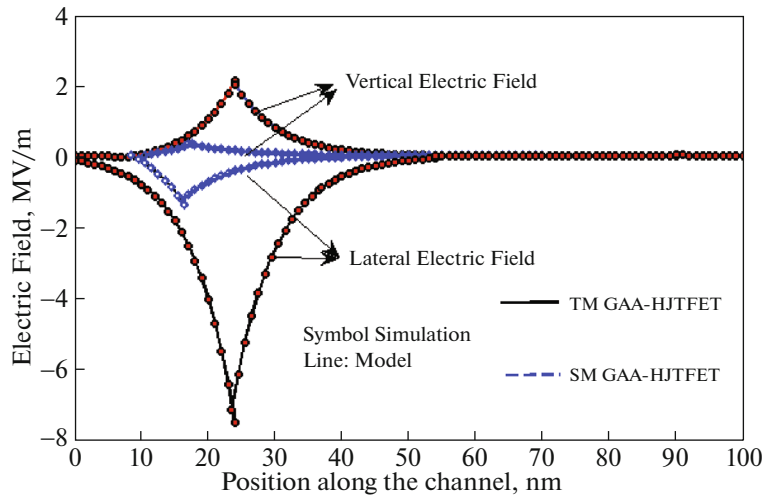

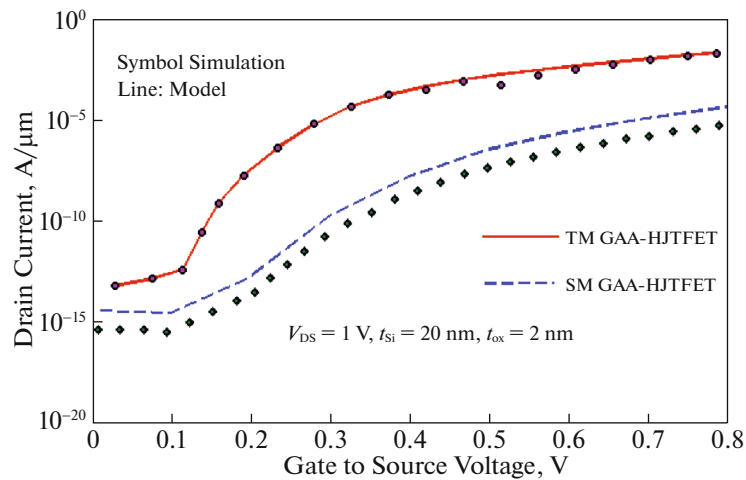**Fig. 5.** Electric field profile comparision plot of TM GAA-HJTFET and SM GAA-HJTFET.

Fig. 6. Comparision of the drain current I_D vs. V_{GS} of TMGAA-HJTFET and SMGAA-HJTFET.

increased the potential at drain channel junction, there by increasing the electric field and band to band tunneling generation rate at drain channel junction.

Figure 5 shows the comparison plot of lateral and vertical electric field of the proposed model with SM GAA-TFET, it is observed that the electric field profile of the proposed model device is high at the source channel junction due to the increase in tunneling rate of electrons from valence band to conduction band.

$I(V)$ characteristic of the proposed model is shown in Fig. 6.

It is studied that the Off current I_{Off} is low due to the barrier created by the forbidden gap that prevents the tunneling of electrons at Off state. On-state current is high due to enhanced electrostatic control of cylindrical gate which reduces the short channel effects and subthreshold swing.

5. CONCLUSIONS

A two-dimensional analytical model of TMGAA-HJTFET is modeled for different parameters such as surface potential, electric field, drain current, transconductance, and threshold voltage by derivative method by considering five depletion regions. The surface potential is modeled using parabolic approximation method for five regions. The electric field components are used to calculate drift and diffusion current. It is observed that the I_{On}/I_{Off} ratio is improved high compared with SMGAA-HJTFET. The proposed model of TMGAA-HJTFET predicts the device electrostatic characteristics on different parameters to gain intuition on device physics. Results obtained are found to be in good agreement with TCAD ATLAS-based simulation results of the proposed device.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. A. C. Seabaugh and Q. Zhang, Proc. IEEE **98**, 2095 (2010).

2. Y. C. Woo, B.-G. Park, J. D. Lee, and T.-J. King Liu, IEEE Electron Dev. Lett. **28**, 743 (2007).

3. K. K. Bhuwalka, J. Schulze, and I. Eisele, IEEE Trans. Electron Dev. **52**, 909 (2005).

4. G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh, G. Q. Lo, D.-L. Kwong, and M.-F. Li, in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)* (2009), p. 741.

5. A. Pan and C. O. Chi, IEEE Electron Dev. Lett. **33**, 1468 (2012).

6. L. Zhang, X. Lin, J. He, and M. Chan, IEEE Trans. Electron Dev. **59**, 3217 (2012).

7. C. Usha and P. Vimala, in *Proceedings of the International Conference on Innovations in Information, Embedded and Communication Systems, Coimbatore, Tamilnadu, India, 2015*, p. 72.

8. R. Vishnoi and M. J. Kumar, IEEE Trans. Electron Dev. **61**, 1936 (2014).

9. P. Pandey, R. Vishnoi, and M. J. Kumar, J. Comput. Electron. **14**, 280 (2015).

10. T. S. A. Samuel and S. Komalavalli, J. Nano Res. **54**, 146 (2018).

11. Q. Shao, C. Zhao, C. Wu, J. Zhang, L. Zhang, and Z. Yu, in *Proceedings of the International Conference on Electron Devices and Solid State Circuit (EDSSC), 2013*, p. 1.

12. R. Vishnoi and M. J. Kumar, IEEE Trans. Electron Dev. **61**, 2599 (2014).

13. A. Zhan, J. Mei, L. Zhang, H. He, J. He, and M. Chan, in *Proceedings of the International Conference Electron Devices, Solid State Circuit (EDSSC), 2012*, p. 1.

14. R. Vishnoi and M. J. Kumar, IEEE Trans. Electron Dev. **61**, 2264 (2014).

15. C. Usha and P. Vimala, J. Nano Res. **55**, 75 (2018).

16. C. Usha, P. Vimala, T. S. Arun Samuel, and M. Karthigai Pandian, J. Comput. Electron. **19**, 1144 (2020).

17. C. Usha and P. Vimala, AEUE Int. J. Electron. Commun. (2019).
https://doi.org/10.1016/j.aeue.2019.152877

18. S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar, and S. Jit, IEEE Trans. Electron Dev. **63**, 3291 (2016).

19. S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).

20. M. Garcia Bardon, H. P. Neves, and R. Puers, and C. van Hoof, IEEE Trans. Electron Dev. **57**, 827 (2010).

21. Md. Arafat Mahmud and S. Subrina, J. Comput. Electron. **15**, 525 (2016).

22. Y. Tsividis, *Operation and Modelling of The MOS Transistor*, 2nd ed. (McGraw-Hill, New York, 1989).

23. A. Akers, Solid State Electron. **23**, 173 (1989).