ISSN 1063-7826, Semiconductors, 2016, Vol. 50, No. 7, pp. 924–928. © Pleiades Publishing, Ltd., 2016.
Original Russian Text © M.M. Sobolev, F.Yu. Soldatenkov, V.A. Kozlov, 2016, published in Fizika i Tekhnika Poluprovodnikov, 2016, Vol. 50, No. 7, pp. 941–945.

SEMICONDUCTOR STRUCTURES, LOW-DIMENSIONAL SYSTEMS, AND QUANTUM PHENOMENA

Study of Deep Levels in GaAs p–i–n Structures

M. M. Sobolev[a], F. Yu. Soldatenkov[a, b], and V. A. Kozlov[a, b, c]

[a] *Ioffe Physical–Technical Institute, Russian Academy of Sciences, Politekhnicheskaya ul. 26, St. Petersburg, 194021 Russia*
[b] *OOO Silovye Poluprovodniki, St. Petersburg, 195220 Russia*
[c] *ZAO NPO FID-Tekhnologiya, St. Petersburg, 195220 Russia*
e-mail: m.sobolev@mail.ioffe.ru

Submitted December 22, 2015; accepted for publication December 28, 2015

Abstract—An experimental study of the capacitance–voltage (C–V) characteristics and deep-level transient spectroscopy (DLTS) of p^+–p^0–i–n^0 structures based on undoped GaAs, grown by liquid-phase epitaxy at two crystallization-onset temperatures T_o (950 and 850°C), with optical illumination switched off and on, are performed. It is shown that the p^0, i, and n^0 layers of epitaxial structures are characterized by the presence of defects with deep donor- and acceptor-type levels in concentrations comparable with those of shallow donors and acceptors. Interface states are found, which manifest themselves in the C–V characteristics at different measurement temperatures and optical illumination; these states form an additive constant. A distinct temperature dependence of the steady-state capacitance of the structures is revealed. It is found that the injection of minority carriers under an applied positive filling pulse and optical recharging lead to modification of the structure and, correspondingly, the DLTS spectra of the p^+–p^0–i–n^0 structures. It is revealed that the p^+–p^0–i–n^0 GaAs structures grown at T_o = 850°C are characterized by a lack of interface states and that the recharging of acceptor-type deep traps under illumination does not change the C–V characteristics. The conventionally measured DLTS spectra reveal the presence of two hole traps: $HL5$ and $HL2$, which are typical of GaAs layers.

DOI: 10.1134/S1063782616070241

1. INTRODUCTION

The problems facing developers of high-speed high-voltage power devices for subnanosecond-pulse semiconductor electronics motivate them to search for new wide-gap materials, which are able to operate at higher temperatures in comparison with Si-based structures and are more resistant to radiative irradiation. An example of such materials is 4H-SiC. To date, analogs have been developed based on this material for all high-power Si devices [1], including those for subnanosecond pulse semiconductor electronics [2, 3]. At present, researchers are paying much attention to GaAs, which is a high-temperature radiation-resistant material. A technology for the epitaxial growth of Ga–As structures with p–i–n junctions from limited solution-melt has been developed. Based on these structures, one can design high-voltage diodes, which can work at frequencies of several megahertz at crystal temperatures up to 300°C [4–8], whereas the upper limit of the reliable operation of 4H-SiC Schottky diodes is below 200°C [8]. Recently a fundamental difference was revealed between high-voltage GaAs diodes and similar silicon devices upon ultrafast switching under conditions of delayed avalanche breakdown [9]. This switching mode made it possible to improve (by several orders of magnitude) the parameters of pulsed high-power semiconductor systems by forming kV voltage drops with a rise time as short as 100 ps. The time characteristics of GaAs diodes (minority-carrier lifetime and voltage-drop rise time) and the voltage blocked by diode structures are significantly affected by defects and interface states with deep levels, formed during the epitaxial growth of p–i–n structures.

In this paper, we report the results of studying deep-level defects in the layers and at the interfaces of GaAs p–i–n diodes, fabricated by liquid-phase epitaxy (LPE) from a limited Ga–As solution-melt, at two crystallization-onset temperatures, 850 and 950°C. The study is performed by methods of capacitance spectroscopy: the capacitance–voltage (C–V) method and deep-level transient spectroscopy (DLTS).

EXPERIMENTAL

The objects of our study were p^+–p^0–i–n^0–n^+ structures based on homoepitaxial GaAs. They were grown by LPE on p-GaAs substrates with the (111) orientation, doped with zinc to (2–10) × 10^{18} cm^{-3}. Epitaxial growth was performed from a limited Ga–As solution-melt in a hydrogen atmosphere in quartz or graphite boats at crystallization-onset temperatures of

850–950°C, with subsequent cooling to room temperature. The donor concentration in the n^+ layer was $N_d = 10^{18}$ cm^{-3}. Ni–Ag and Au–Ge–Ag ohmic contacts were thermally deposited onto the surfaces of the p^+ and n^+ layers, respectively. Under the aforementioned growth conditions, the compensation and doping of epitaxial layers are determined by the content of background impurities in the melt and the growth system, the content of deep-level lattice point defects, the temperature and duration of preliminary flux annealing, and the consumption of hydrogen and its humidity. They also depend on the epitaxial-film crystallization conditions upon forced cooling of the system. One can form thick GaAs i layers with a free-carrier concentration $n < 10^{13}$ cm^{-3} in these structures. The i-layer thickness, depending on the technological growth conditions, can be varied from 10 to 85 μm, due to which blocking voltages as high as 2000 V can be obtained. Hall measurements of the p^+–p^0–i–n^0 structures by the van der Pauw method revealed that the distribution profiles of the carrier concentration and mobility in the p^0 and n^- layers tend to decrease towards the i layer [10]. The formation of an ensemble of deep-level defects is determined by the crystallization-onset temperature T_o. As was shown in [10, 11], the LPE growth of GaAs layers from a solution-melt of limited volume at low crystallization-onset temperatures (T_o = 650–800°C) led to the formation of an undoped n^0-type layer with two deep levels: $HL2$ (E_v + 0.72 eV) and $HL5$ (E_v + 0.38 eV) [10–13].

These two deep levels are hole traps; they are typical of LPE-grown GaAs layers. An increase in T_o led to an exponential increase in the concentrations of the $HL2$ and $HL5$ levels [10–13]. At a high crystallization-onset temperature ($T_o \geqslant 850$°C), an i region is formed, where compensation occurs due to the background impurity and deep-level defects. Layer compensation may involve (along with the well-known $HL2$ and $HL5$ levels [10–13]) two more levels, E_c – 0.82 and E_v + 0.56 eV ($HM1$) [10, 11, 14–16], which belong to two charge states (D^{2+}/D^+ and D^+/D^0) of the $EL2$ defect. The values of the thermal activation energy, referenced, respectively, to the valence band (E_v) and conduction band (E_c), are given in parentheses.

3. RESULTS AND DISCUSSION

We investigated the C–V characteristics and DLTS spectra of chips of two p^+–p^0–i–n^0 structures based on homoepitaxial GaAs by a DL4600 DLTS spectrometer (BIORAD, England) equipped with a Boxcar integrator. The first (commercial) structure, with unknown technological growth conditions, was fabricated by Voitovich (AS Clifton, Tartu) [7]. Apparently, this structure was grown at a crystallization-onset temperature T_o = 950°C. The second p^+–p^0–i–n^0 structure, based on undoped GaAs, was fabricated at the Ioffe Physical–Technical Institute [5]. This structure was grown at T_o = 850°C. The C–V characteristics of the diodes were analyzed at different temperatures and different measurement conditions (either in darkness or exposed to white light) (Fig. 1). The first structure exhibited a thick i layer, located in the space-charge layer (SCL) even at zero reverse bias: $U_0 = 0$. The thickness of this layer was about 45 μm at a measurement temperature of 300 K. We found a strong temperature dependence of the steady-state capacitance of the sample (C_0), which decreased by a factor of 1.3–1.5 with a change in the measurement temperature from 100 to 300 K; this change is much larger than that related to the temperature behavior of the diffusion potential. This circumstance should lead to a nonexponential dependence of capacitance relaxation when measuring the DLTS spectra. It can be seen in Fig. 1 that the C–V characteristic also depended on exposure to light during measurements. Illumination led to an increase in capacitance (this occurred both at 100 and 300 K), and the C–V characteristics shifted parallel to themselves. This means that the SCL thickness increases with a decrease in measurement temperature and, correspondingly, decreases under illumination. The most likely reason for this temperature behavior of the SCL thickness is the presence of interface deep states of the donor and acceptor types at the p–n junction. The influence of the density of interface states, N_{ss}, on the C–V characteristic of p–n junctions was investigated in [17–20]. Interface deep levels have a charge, which is an additive constant (dependent on temperature and optical illumination) for C–V measurements. The density of charged interface states decreases with a decrease in temperature and increases under illumination, which leads, correspondingly, to a

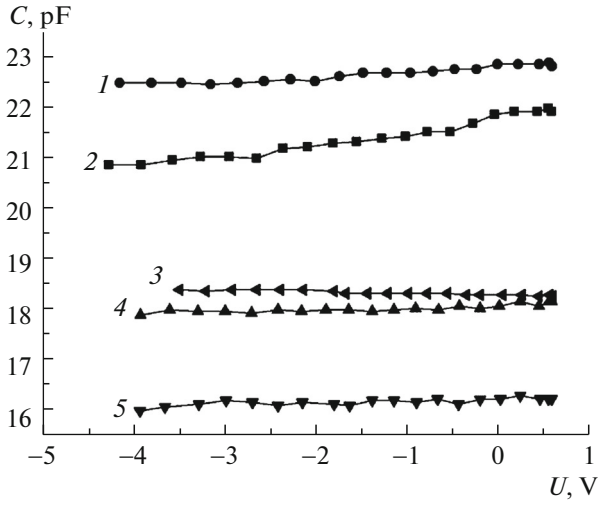

Fig. 1. C–V characteristics of GaAs p^+–p^0–i–n^0 diodes grown by LPE at T_o = 950°C, recorded at different temperatures T: (*1*, *2*) 300, (*4*) 200, and (*3*, *5*) 100 K, either in darkness (*2*, *4*, *5*) or under illumination (*1*, *3*).

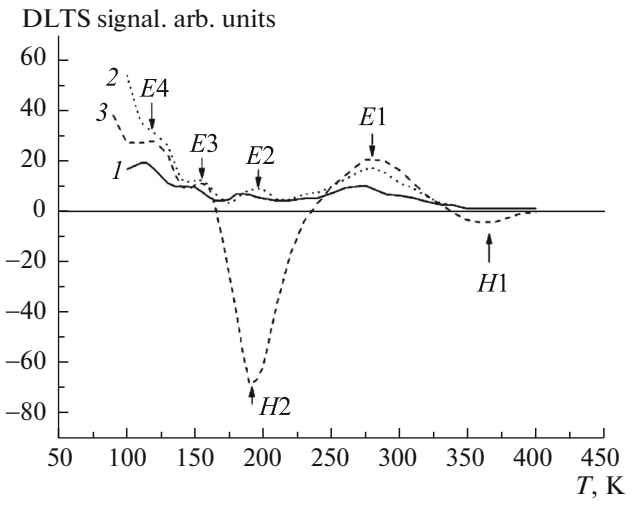

Fig. 2. DLTS spectra of GaAs p^+–p^0–i–n^0 diodes grown by LPE at T_o = 950°C, recorded with a window rate of 200^{-1} s, at a reverse bias of V_r = –2.11 V, under illumination, and with filling pulses of V_f = (*1*) –0.12, (*2*) +1.14, and (*3*) +1.88 V.

change in capacitance C. Another specific feature of the C–V characteristics was that the capacitance of the p–n junction barely changed with an increase in reverse bias U across the structure. These C–V characteristics with a plateau are generally typical of structures with the spatial localization of deep states, for example, quantum dots [21, 22] or quantum wells. Deep-level defects, localized in the interface region, may also facilitate the formation of such dependences. The plateau width in the C–V characteristic for these structures depends on the level occupancy. The observed behavior of the C–V characteristics of the diodes under study (Fig. 1), measured at different temperatures and under different conditions (in darkness or under illumination), shows also that the p^0 and n^0 layers contain a rather large number of deep traps of donor and acceptor types. The recharging of these traps under illumination may significantly change the effective carrier concentration in the conduction and valence bands of these layers and, in particular, reduce the SCL thickness. The optical recharging of deep levels in the i layer in the presence of traps located in the middle of the band gap, for example, the *EL*2 trap, may change (due to filling of the *EL*2 trap, which compensates for shallow acceptor impurities) the conductivity type of the semi-insulating layer: from the n type to the weak p type. This recharging may facilitate the formation of a second depletion region at the interface between the i and n^0 layers [23]. The reverse situation may also occur, where the acceptor-type trap *HL*2 plays the role of this trap and compensates shallow and deep donors in the p-type semi-insulating layer [23]. Illumination may lead to the capture of light-excited electrons and holes to deep donor and acceptor traps. With allowance for the fact that $N_{ta} > N_{td}$ (here N_{ta} and N_{td} are the concentrations of deep acceptor and donor traps, respectively), the concentration of uncompensated donors increases, the capacitance increases, the Fermi level shifts to the conduction band, and the occupancy of deep levels increases. The carrier concentration in the conduction band increases as well, and the p-type semi-insulating layer is transformed into a weak-n-type layer.

Generally, the DLTS spectra of semiconductor structures exhibit only a negative peak when the probability of main-carrier trap occupancy changes after a negative filling pulse ($V_f < 0$) and under reverse bias (V_r) [12]. When studying the DLTS spectra of p–i–n-diode structures similar to that described above, optical illumination during DLTS scanning of the main-carrier traps under reverse bias and with a filling pulse $V_f < 0$ may facilitate the formation of a positive DLTS signal, which is due to minority-carrier traps. In the case of DLTS scanning with a filling pulse $V_f > 0$, one should observe an increase in the amplitude of the positive DLTS signal [12]. However, such DLTS signals are difficult to identify: their position under temperature scanning may significantly differ from the true one. The trap parameters (capture cross section and, especially, trap concentration), determined by the DLTS method, in principle cannot be determined exactly for the structures under study. One can only trace the changes in the amplitudes of the DLTS signals related to electron and hole traps. Deep levels can be identified by comparing measured the Arrhenius dependences with published data. The capture cross section, which is determined from the cutoff value, does not greatly affect the Arrhenius plot. The main parameter in this case is the slope of the Arrhenius dependence. If the nature of deep levels is known from publications, one can speak about the nature of traps. In standard DLTS measurements, a forward bias pulse ($V_f > 0$), which injects minority carriers, is used to scan minority-carrier traps; however, the standard DLTS method does not always reveal traps in the structure studied. It was shown in [24, 25] that a positive DLTS peak can also be observed for asymmetric p^+–n and n^+–p junctions. These junctions are characterized by the presence of an extended tail of minority-carrier traps in the interface region, the occupancy of which is determined by the intersection point of the Fermi level with the energy level of the trap tail. The capture of minority carriers to the trap tail in the interface region with their subsequent emission gives rise to a positive peak in the DLTS spectra. Figure 2 shows the DLTS spectra of GaAs diodes based on p^+–p^0–i–n^0 structures, measured at a reverse bias of V_r = –2.1 V and different filling-pulse amplitudes V_f, both in darkness and under illumination.

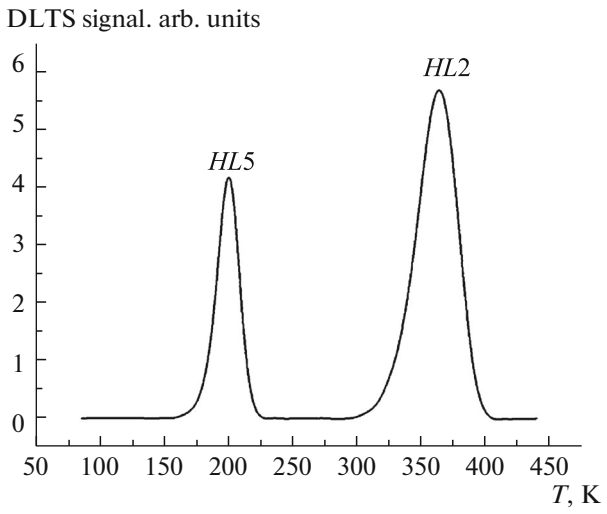

Fig. 3. DLTS spectra of GaAs p^+–p^0–i–n^0 diodes grown by LPE at T_o = 850°C, recorded with a window rate of 200^{-1} s, at a reverse bias of V_r = –2.72 V, in darkness, and with a filling pulse of V_f = 0.44 V.

DLTS signals were found to be absent in the measurements performed in darkness at V_r = –2.1 V. At the same time, four positive DLTS signals were observed under illumination at V_r = –2.1 V and filling pulses of V_f = –0.12 and 1.14 V (Fig. 2); they are denoted as $E1$, $E2$, $E3$, and $E4$. At V_f = +1.88 V, two more DLTS signals (both negative and high-amplitude) arose (Fig. 2); they were attributed to majority carrier traps: $HL2$ and $HL1$. Above we noted the possibility of the occurrence of a positive signal in the DLTS spectra of p^+–p^0–i–n^0–n^+ structures at $V_f < 0$ when discussed possible recharging mechanisms for the deep levels of donor and acceptor types in the vicinity of the p^0–i and i–n^0 interfaces in the structure studied under illumination. The amplitudes of the $E1$–$E4$ peaks depended on the filling-pulse amplitude; this dependence is generally related to the increased filling of minority carrier traps. Arrhenius dependences were plotted for the observed DLTS signals on the assumption that donors are minority-carrier traps and acceptors are majority-carrier traps; i.e., it was taken into consideration that the changes in the space-charge region observed in the DLTS measurements occur in the p-type semi-insulating layer. The Arrhenius plots made it possible to determine the parameters of deep donor levels. The thermal activation energies for deep donor levels were $E1$ (E_c – 440 meV), $E2$ (E_c – 277 meV), $E3$ (E_c – 0.175 meV), and $E4$ (E_c – 66 meV).

An attempt was made to identify deep levels by comparing the Arrhenius plots for these levels with published data. The levels found for the first time in [26–28] (where DLTS data on LPE-grown GaAs layers irradiated with 1-MeV electrons were reported) turned out to be the closest to the observed deep donor levels. These levels are most likely due to As-vacancy–As-interstitial complexes. Concerning the majority carrier peaks $H1$ and $H2$, they turned out to be spurious, being independent of the width of the emission-rate window (a typical feature of deep-level traps). As was shown in [23], optical recharging of deep-level traps in p–i–n structures (provided that $N_{ta} > N_{td}$) may lead to the formation of a second depletion region at the p^0–i interface and thus increase the resistance connected in series with the space-charge-layer capacitance. In this case, the relaxation of series resistance upon thermal scanning may manifest itself in the DLTS spectrum in the form of spurious majority carrier peaks, the temperature position of which may differ from the true ones. These spurious peaks and corresponding optical recharging were determined by the presence of $HL5$ and $HL2$ traps (in a concentration exceeding the concentration of deep-level donor traps) in the structures under study.

We investigated the C–V characteristics and DLTS spectra of the GaAs p^+–p^0–i–n^0–n^+- diode structures grown at T_o = 850°C (Fig. 3) [10, 11]; the measurements were performed in darkness and under illumination. It was shown that the observed changes in the C–V characteristics are related to the temperature behavior of the diffusion potential rather than to the interface states at the p–i and i–n interfaces. The thickness of the i layer at a measurement temperature of 300 K was about 3.5 μm. The observed behavior of the C–V characteristics of these structures, measured at different temperatures and under different conditions (with optical illumination switched off and on), shows that the light-induced recharging of acceptor-type deep traps in the i layer and adjacent p^0 and n^0 layers does not change significantly the effective carrier concentration in the conduction band of the epitaxial layers, in contrast to the p^+–p^0–i–n^0–n^+ structures grown at T_o = 950°C. The DLTS spectra of the GaAs p^+–p^0–i–n^0–n^+-diode structures grown at T_o = 850°C exhibited two hole traps: $HL5$ and $HL2$ (Fig. 3); these traps are characteristic of lightly doped GaAs layers of high structural quality, grown by LPE in a hydrogen atmosphere [10, 11]. No interface defects with donor- or acceptor-type deep levels were observed in the DLTS spectra.

4. CONCLUSIONS

The C–V characteristics and DLTS spectra of p^+–p^0–i–n^0- and p–i–n- structures based on undoped GaAs, grown by LPE at crystallization-onset temperatures of 950 and 850°C, respectively, were investigated, both in darkness and under illumination. The results of this study suggest that the p^+–p^0–i–n^0–n^+ structures are characterized by the presence of deep-level defects of donor and acceptor types in the epitaxial p^0, i, and n^0 layers, the concentrations of which are

comparable with the concentrations of shallow donors and acceptors involved in the compensation of epitaxial layers. Interface states were revealed, which manifest themselves under illumination at different measurement temperatures in the $C-V$ characteristics and are an additive constant. In view of the aforesaid, the steady-state capacitance of the structures depends heavily on temperature, which hinders determination of the deep-level defect concentration. Both the injection of minority carriers under a positive filling pulse and optical recharging, which are intended to expand the potential of DLTS spectroscopy, may lead to modification of the $p^+-p^0-i-n^0$ structures and, correspondingly, their DLTS spectra; this circumstance must be taken into account when identifying DLTS signals. Interface states were lacking for the $p^+-p^0-i-n^0$ GaAs structures grown at T_o = 850°C, and the recharging of acceptor-type deep traps under illumination did not change the $C-V$ characteristics. The DLTS spectra were measured in the standard way, which made it possible to easily determine the presence of two hole traps in them: *HL*5 and *HL*2; these traps are typical of GaAs layers.

ACKNOWLEDGMENTS

This study was supported in part by the Russian Foundation for Basic Research, project no. 16-08-00954-a.

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Translated by Yu. Sin'kov