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SEMICONDUCTOR STRUCTURES, LOW-DIMENSIONAL SYSTEMS, AND QUANTUM PHENOMENA

Degradation of the Electrical Characteristics of MOS Structures with Erbium, Gadolinium, and Dysprosium Oxides under the Effect of an Electric Field

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Abstract—The degradation of the characteristics of silicon metal–oxide–semiconductor (MOS) structures with oxides of rare-earth elements under the effect of electric fields with intensities of 0.1–4 MV/cm during the course of electroforming is studied. A specific feature of electroforming consists in the possibility of multiple switching of the structures from the insulating state to the low-resistivity one and back. The temporal characteristics of the degradation of MOS structures during the course of electroforming are exponential. The current–voltage characteristics follow the power law in the range of 0.2–3 V; the effect of an electric field brings about a variation in the distribution of the energy density of traps responsible for currents limited by space charge. It is established that multiple cycles of electroforming lead to an increase in the density of surface states at the Si–oxide interface and to a variation in the energy position of the trap levels, which affects the charge state of the traps.

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1. INTRODUCTION

Metal–oxide–semiconductor (MOS) structures represent a necessary component of MOS transistors, energy-independent memory components, charge-coupled devices, and so on. Most attention is typically focused on the thickness of the oxide film and on the quality of the oxide–semiconductor interface. The thickness of a gate-oxide film is considered optimal if it provides the necessary high capacitance and, at the same time, a low through leakage current. The tendency to satisfy these requirements has led to a situation where the traditional gate oxide SiO_2 is replaced in MOS structures with oxides with a larger permittivity, i.e., with so-called *high-k* insulators.

The technology of the fabrication of MOS structures with the SiO_2 gate oxide has been studied for rather a long time and allows the formation of a fairly perfect Si–SiO_2 interface. However, even with respect to such a structure, there is at present no complete understanding of the pattern of degradation of the electrical properties, which occurs under different conditions of MOS-structure use. The surface electron states (SESs) present at such an interface, i.e., P_b centers, arise due to the difference between the lattices of the bulk Si and the oxide [1, 2]. The main paramagnetic defect in the SiO_2 bulk is the oxygen vacancy, which traps a hole (the E' center) [3–6].

Oxides of rare-earth elements (REEs) are the preferred candidates for the material of gate insulators in the near future [7–9]. Due to their relatively high permittivity these materials belong to the class of *high-k* insulators. One of the main problems in the application of REE oxides is a high concentration of charged defects, which induces a shift in the threshold voltage of the transistor. These charged defects are typically intrinsic defects, such as oxygen vacancies and interstitials. In addition, it is established that a layer of silicate is generally formed at the REE–silicon interface; the thickness of this layer amounts to 0.7–2 nm [10]. Also, the formation of an intermediate SiO_2 layer (or the formation of a SiO_2 layer only) in many cases is observed between the silicate and the REE oxide. Defects in the oxide film and at the interfaces give rise to degradation of the electrical properties of MOS structures. Consequently, a decrease in the concentration of charged defects and a study of the conditions of their formation are important problems, which require solution.

In this work, we report the results of our studies of silicon MOS structures, in which films of REE oxides are used. The prospects for the use of MOS structures with *high-k* insulators, which have been considered in recent years, are fairly promising; this fact gives rise to new challenges related to studies of *high-k* insulators and devices on their basis. In connection with this, studies of the reliability and service life of devices based on MOS structures with *high-k* insulators are topical. The aim of this study is investigation into degradation of the electrical characteristics of MOS structures with REE oxides under the effect of an electric field.

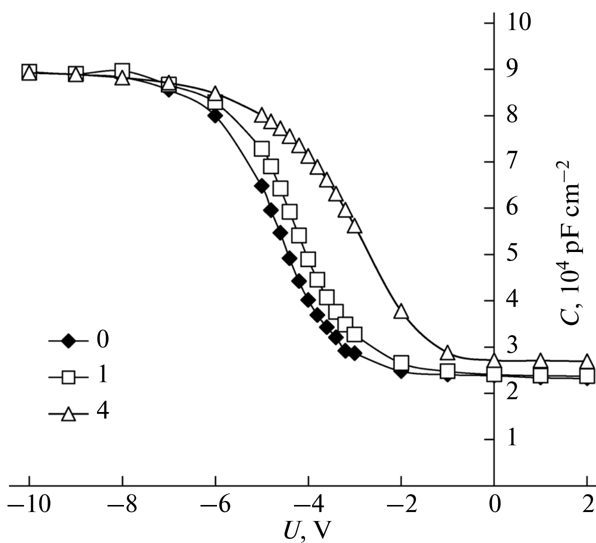

Fig. 1. Capacitance–voltage characteristics of an Al–Gd_2O_3–*p*-Si structure in the initial state and after several cycles of electroforming (the number of cycles is indicated).

2. EXPERIMENTAL

Single-crystalline *n*-Si or *p*-Si wafers with a resistivity of 4.5–5 Ω cm and the orientations (111) or (100) were used as substrates for the MOS structures. The thermal evaporation of rare-earth elements was performed using a setup for vacuum deposition; the initial materials for deposition were provided by substances with a purity of 99.6–99.98%. The oxidation of metallic REE films was conducted in a flow of dry oxygen or in air in a laboratory-type furnace at temperatures of 500–700°C for 20–30 min. Prior to the deposition of a rare-earth metal layer, all of the silicon wafers were subjected to treatment in acetone in an ultrasound bath and were then treated in a dilute solution of hydrofluoric acid. The obtained REE-oxide films with thickness of 0.1–0.3 μm were polycrystalline; their composition was nearly stoichiometric. The permittivity of the Dy_2O_3 and Er_2O_3 thin films was ~11; in the case of Gd_2O_3, the permittivity was equal to ~(13–14). In order to obtain MOS structures by the method of thermal evaporation in vacuum through a stencil, aluminum electrodes were deposited with an area of ~0.2 mm^2. The lower aluminum electrode was deposited as a continuous layer.

We studied the effect of electric fields on the obtained structures under conditions where these fields gave rise to the electroforming effect. The process of electroforming consists in that, under the effect of electric fields, ~(0.1–4)MV/cm), a local inhomogeneous region (a conducting channel with metallic-type conductivity) is formed in the initially homogeneous oxide film. However, this state is not irreversible; at reverse polarity of the applied voltage, there is the possibility of transforming the studied structures back to the insulating state via a conducting current. We used the possibility of multiple switching of the structures from the high-resistivity state to the low-resistivity one and back; since the MOS structures under investigation with films of REE oxides feature the property of bistable switching [11, 12].

3. EXPERIMENTAL RESULTS

3.1. Experimental Capacitance–Voltage Characteristics

We studied the effect of an electric field on the sample during the course of electroforming with subsequent monitoring of the parameters of the structures after each cycle of electroforming. These data were obtained from an analysis of the high-frequency (1 MHz) capacitance–voltage (*C–V*) characteristics of the MOS structures with REE oxides in the high-resistivity state.

Upon consideration of the *C–V* characteristics, we can note that electroforming gives rise to degradation of the electrical parameters of MOS structures with REE oxides as insulators. The *C–V* characteristics are more extended along the voltage axis after several electroforming cycles, which is indicative of an increase in the density of surface states and a variation in the flat-band voltage (Fig. 1).

The flat-band voltage U_{FB} is the voltage at which the surface potential acquires zero value:

$$U_{FB} = \Phi_{ms} + \left(-\frac{Q_f}{C_D}\right), \quad (1)$$

where Φ_{ms} is the difference between the work functions for the metal and the semiconductor, C_D is oxide capacitance, and Q_f is the effective charge. By the effective charge here is meant the total density of the charge of traps at the oxide–silicon interface (Q_{it}) and in the oxide bulk (Q_f^*):

$$Q_f = Q_f^* + Q_{it}. \quad (2)$$

The distribution of the energy density of surface states D_{it} in the band gap of silicon was obtained from the dependence of the surface potential on the voltage *U* using the formula

$$D_{it} = \frac{C_D}{e^2}\left(\frac{dU}{d\phi_s} - 1\right) + \frac{C_s}{e^2}, \quad (3)$$

where C_s is the capacitance of the space-charge region, Φ_s is the value of the surface potential, and *e* is the elementary charge. This method yields a U-shaped energy distribution of D_{it} in the band gap of silicon for the structures under study. In this study, the value of D_{it} was taken equal to that at the minimum of the distribution.

For all studied structures, the charge varies in a complicated way; however, experimental results show that, while an increase in the density of surface states

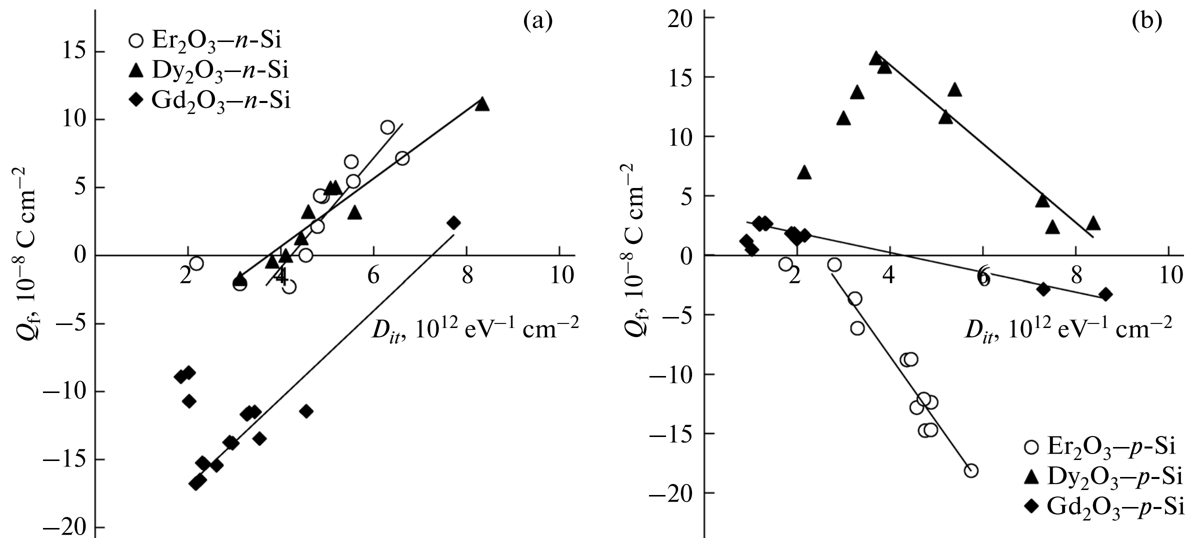

Fig. 2. Variation in the effective charge in relation to a variation in the density of surface states in the case of multiple cycles of electroforming for MOS structures with REE oxides based on (a) *n*-Si and (b) *p*-Si.

is observed during the course of electroforming, a tendency toward an increase in the negative charge is observed for structures based on *p*-Si whereas positive charge increases in the structures based on *n*-Si. Since the structures were switched from the high-resistance state to the low-resistance one at a voltage polarity corresponding to the inversion mode this possibly indicates that charge carriers from the inversion channel are involved in degradation of the structures.

The dependence of the effective charge Q_f on the density of surface states D_{it} in the case of multiple cycles of electroforming can be approximated by straight lines as is shown in Figs. 2a and 2b for MOS structures based on *n*-Si and *p*-Si, respectively. The proportional dependence indicates that the variation in the charge in MOS structures based on REE compounds as a result of electroforming is mainly caused by a variation in the SES density at the oxide–silicon interface. Starting with the values of ~(2–4) × 10^{12} eV^{-1} cm^{-2}, a tendency toward a decrease in the absolute value of Q_f is observed as the value of D_{it} tends to zero.

3.2. Experimental Current–Voltage Characteristics

We studied the mechanisms of conduction by measuring the current–voltage (*I–V*) characteristics in a number of successive cycles of electroforming. The conductance of the MOS structures with REE compounds can be controlled by the introduction (injection) of excess free charge carriers into these structures.

In the case of an insulator, which does not contain traps for electrons, and also in the case of an insulator with shallow-level monoenergetic traps, the current density is described by the dependence

$$j = \frac{\varepsilon_0 \varepsilon \mu U^2}{d^3}, \tag{4}$$

where μ is the mobility of charge carriers in the oxide, ε is the permittivity of the oxide, and *d* is the oxide thickness. Such characteristics were observed by Jinesh et al. [13] (in the range from 1 to 3 V) for silicon MOS structures with erbium-oxide films obtained by layered atomic deposition.

If charge carriers injected from the contacts are trapped by local centers and form space charge in the insulator, then the currents passing through the insulator are currents limited by space charge. In the case of capacitance-based consideration of this issue, the charge density Q_i is related to the specific capacitance of the capacitor C_D and applied voltage as

$$Q_i = C_D U = \frac{\varepsilon_0 \varepsilon U}{d}. \tag{5}$$

The current through the insulator is given by

$$j = e\mu n E_{ox} = e\mu n \frac{U}{d}, \tag{6}$$

where *n* is the concentration of electrons in the oxide conduction band. E_{ox} is the field intensity in the oxide and *U* is the voltage drop across the oxide layer. The presence of traps leads to a decrease in the current since the corresponding levels trap an overwhelming portion of injected electrons and form space charge

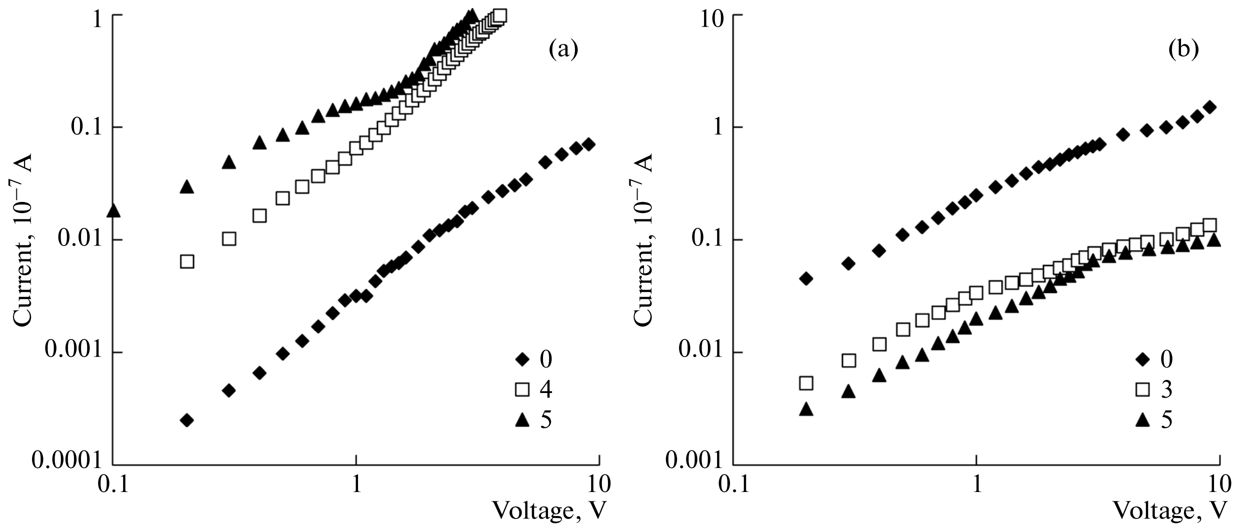

Fig. 3. Forward portions of the *I*–*V* characteristics under the effect of multiple cycles of electroforming for (a) an Al–Dy_2O_3–*n*-Si structure and (b) an Al–Dy_2O_3–*p*-Si structure. The number of cycles is indicated.

near the oxide–semiconductor interface. The concentration of electrons n_t in the traps is given as

$$n_t = \frac{Q_i}{ed} \approx \frac{\varepsilon_0 \varepsilon U}{ed^2}. \tag{7}$$

According to Boltzmann statistics, the concentration of electrons in the conduction band of the insulator is given by

$$n = N_c \exp\left(-\frac{\mathscr{E}_c - \mathscr{E}_F}{k_B T}\right), \tag{8}$$

where N_c is the effective density of states in the conduction band of the insulator, $\mathscr{E}_c$ is the energy of the conduction-band bottom in the insulator, $\mathscr{E}_F$ is the Fermi-level energy, k_B is the Boltzmann constant, and T is the absolute temperature.

Due to considerable structural disorder of the lattice, especially near the insulator–semiconductor interface, local electron centers of any type, both those related to impurities and those attributed to intrinsic defects can be markedly spread in energy. In this case, the distribution of trap levels over energy can be quasi-continuous with the bottom of the conduction band blurred. The so-called tail of the conduction band penetrates deep into the band gap; the states in the tail are localized and act as traps for electrons. The tail of the traps, the energy density of which $\rho(\mathscr{E})$ increases exponentially as the conduction-band bottom is approached is described as

$$\rho(\mathscr{E}) = \rho_0 \exp\left[-\frac{(\mathscr{E}_c - \mathscr{E})}{gk_B T}\right], \tag{9}$$

where ρ_0 is the energy density of traps at the conduction-band bottom, and g is the distribution factor related to the specific features of traps.

Almost all injected electrons are immobilized in traps, the total concentration of which is given by

$$n_t = \int_{\mathscr{E}_F}^{\infty} \rho(\mathscr{E}) d\mathscr{E} = N_t \exp\left[-\frac{(\mathscr{E}_c - \mathscr{E})}{gk_B T}\right], \tag{10}$$

where N_t is the concentration of traps near the conduction-band bottom. Removing the Fermi level from expressions (8) and (10), we obtain

$$j = e\mu N_c \left(\frac{\varepsilon_0 \varepsilon}{eN_t}\right)^g \frac{U^{g+1}}{d^{2g+1}}. \tag{11}$$

In coordinates $\log j$ versus $\log U$ the *I*–*V* characteristic is bound to be expressed by a straight line with the slope $g + 1$. The *I*–*V* characteristics of the studied MOS structures were practically symmetric. Figure 3 shows the forward branches of the *I*–*V* characteristics of silicon MOS structures with dysprosium oxide in the initial state and after several cycles of electroforming. These dependences are fairly well linearized in double logarithmic coordinates, which is indicative of the power-law dependence of the current on voltage. Similar power-law dependences with an exponent of 3–4 were reported by Rozhkov and Petrov [12] for MOS structures with a film of gadolinium oxide obtained by the method of high-frequency ion–plasma deposition on silicon.

In this study, the exponent (the slope of the *I*–*V* characteristic) for the Al–Dy_2O_3–*n*-Si structures was found to be $g + 1 = 1.5$–2.5 in the range of voltages 0.2–1.3 V and the conductance sequentially increased with an increase in the number of electroforming

cycles (Fig. 3a). As the voltage was further increased, the slope increased to the values $g + 1 = 2.2–2.9$. In contrast, for the Al–Dy_2O_3–p-Si structures, the conductance decreased as the number of the electroforming cycles was increased. The exponent was $g + 1 = 0.7–1.1$ in the range of voltages 0.2–3 V; with a further increase in voltage, the exponent decreased to $g + 1 = 0.35–0.65$ (Fig. 3b). The reverse portions of the $I–V$ characteristics featured similar behavior, i.e., the current sequentially increased with an increase in the number of electroforming cycles for structures based on n-Si and sequentially decreased for structures based on p-Si.

Although the studied films of REE oxides in general featured a polycrystalline structure, a thin transition layer, whose structure is close to amorphous, can be observed, at the REE oxide–silicon interface. In addition, a transition layer of silicate or SiO_2 with an amorphous nature is often observed at this interface [10]. Therefore, we may assume the presence of the tail of traps whose energy density is described by an exponential law (9).

In the context of this approach, we can also explain a variation in the $I–V$ characteristic as a result of electroforming. If we assume, in the first approximation, that $n_t = \text{const}$ in expression (10), then, to retain constancy, the value of N_t is bound to decrease as the factor g is increased and vice versa. Then, for MOS structures based on n-Si, where the g factor tends toward an increase with increasing number of electroforming cycles, the value of N_t is bound to decrease, which, according to formula (11), leads to an increase in the current density. In contrast, for structures based on p-Si, the factor g tends to a decrease with an increase in the electroforming cycles; in this case, the value of N_t increases and, consequently, the current density decreases.

Thus, the effect of electric field during the course of electroforming brings about a variation in the g factor, i.e., it varies the distribution of the energy density $\rho(\mathcal{E})$ of the traps responsible for currents limited by space charge.

4. DISCUSSION OF RESULTS

In order to study the effect of the degradation of MOS structures with REE oxides, we investigated the kinetic characteristics of electroforming. The characteristic parameter of the kinetic characteristics of electroforming was investigated. The characteristic parameter of the kinetic characteristic of electroforming is the presence of a specific delay time τ_{del} after which the sample rapidly transforms from one state to another in the time τ_s (the intrinsic electroforming time). The delay time decreases as the amplitude of the applied voltage pulse is increased, the intrinsic switching time is practically independent of the applied voltage pulse. For the studied structures with REE films, the time τ_s amounted to ~0.2 μs. Figure 4 shows the dependences of the delay time of electroforming τ_{del} on the electric-field strength. These dependences are well linearized in semilogarithmic coordinates and are described by the formula

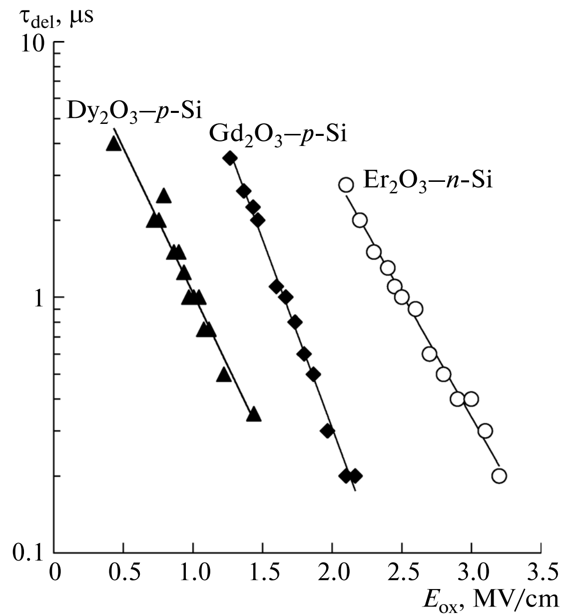

Fig. 4. Dependence of the delay time τ_{del} in the structures subjected to electroforming on the electric-field strength.

$$\tau_{del} = \tau_0 e^{-\gamma E_{ox}}, \quad (12)$$

where τ_0 is a constant for the structure under investigation, E_{ox} is the field strength in the oxide, and γ is the parameter of field acceleration.

During the course of electroforming, the electric field can facilitate the formation of defects at the interface and in the bulk of the insulator. This field strengthens bonds at the interface and thus reduces the strength of bonds in the bulk of the insulator. These weakened bonds can be additionally excited or catalyzed by interaction with either the induced current of electrons, or holes, or hydrogen ions.

Analysis of the experimental data shows that a dominant contribution to a variation in the charge state of MOS structures with REE oxides, which occurs during the course of electroforming, is provided by a change in the SES charge. This is indicated by the fact that the variation in the effective charge is proportional to the density of the SESs. According to their charge status, the surface states can be of two types, i.e., of the donor and acceptor types. The states of the donor type are positively charged if their level is located above the Fermi level and are neutral if the level is below the Fermi level. The states of the acceptor type are neutral if their level is above the Fermi level and are negatively charged if this level lies below the

Fermi level. In the majority of cases, as the experiment shows, SESs of the acceptor type have their levels in the upper half of the band gap while SESs of the donor type have their levels in the lower half of the band gap [14].

It can be assumed that, as the density of SESs increases, the traps change their energy $\mathscr{E}_t$, i.e., in an n-type semiconductor, for newly formed or already existing traps, the difference

$$\Delta\mathscr{E}_t = \mathscr{E}_c - \mathscr{E}_t, \quad (13)$$

decreases; here, $\mathscr{E}_c$ is the energy corresponding to the bottom of the semiconductor conduction band. In this case, an acceptor trap becomes shallower and becomes located higher with respect to the Fermi level $\mathscr{E}_{\rm F}$ and loses its negative charge. For the upper half of the silicon band, the charge formed by acceptors is given by

$$Q_{it}^a = e\left[\int_{\mathscr{E}_{\rm F}}^{\mathscr{E}_c} D_{it}(\mathscr{E}) f(\mathscr{E}) d\mathscr{E} + \int_{\mathscr{E}_i}^{\mathscr{E}_{\rm F}} D_{it}(\mathscr{E}) f(\mathscr{E}) d\mathscr{E}\right], \quad (14)$$

where $f(\mathscr{E})$ is the function determining the extent of the involvement of surface states in changes in the capacitance and $\mathscr{E}_i$ is the Fermi level in an intrinsic semiconductor. As the density of surface states decreases, the absolute value of the contribution of the second term in (14) to the total sum and, consequently, the total measured charge Q_{it}^a of all surface traps becomes more positive.

We can similarly describe the processes taking place at the interface between p-Si and a REE oxide. As the SES density increases, the difference

$$\Delta\mathscr{E}_t = \mathscr{E}_t - \mathscr{E}_v, \quad (15)$$

decreases; here, $\mathscr{E}_{\rm v}$ is the energy of the valence-band top. Crossing the level $\mathscr{E}_{\rm F}$, the trap loses positive charge; in this case, the total charge of all surface traps becomes more negative as the density of surface states is increased.

In the range of SES ~(2–4) × 10^{12} eV^{-1} cm^{-2}, a kink in the behavior of the dependences shown in Fig. 2 is observed; this can also be explained in terms of the above approach. It should be assumed that, before the kink point is attained, the energy position of the newly formed traps is below the Fermi level for acceptor traps and above the Fermi level for donor traps (i.e., closer to the midgap of silicon).

As was shown by Ang et al. [15], the physical structure of defects in a gate *high-k* oxide depends on the applied voltage; in this case, new energy states of the trap can be formed, both stable and metastable.

Consequently, multiple cycles of electroforming lead to an increase in the SES density at the Si–(REE oxides) interface and to a change in the energy position of the levels of traps, which, as a result, brings about a change in their charge state. In addition, the fixed charge in the REE oxide is bound to introduce specific features into the general pattern of variation in the charge state of a MOS structure in each case.

5. CONCLUSIONS

We studied silicon MOS structures, in which the films of oxides with a large permittivity, namely, of oxides of gadolinium, erbium, and dysprosium. We studied the effect of electric fields ~(0.1–4) MV/cm, at which the effect of electroforming is observed, on the process of their electrical degradation.

The temporal characteristics of degradation upon electroforming are described by exponential dependences. The electric field, which is in effect during the course of electroforming, serves to strengthen and weaken bonds, which can be additionally excited or catalyzed by interaction with the induced current of electrons, or by holes, or by hydrogen ions.

The current–voltage characteristics of the studied MOS structures are practically symmetric. Assuming that there is a tail of traps, whose energy density increases exponentially as the bottom of the conduction band is approached, we found that the I–V characteristics under the condition of space-charge-limited currents, which is observed in the range of 0.2–3 V for various studied structures, are described by a power law. It was established that the effect of an electric field during the course of electroforming leads to a variation in the distribution of the energy density $\rho(\mathscr{E})$ of the traps responsible for currents limited by space charge.

An analysis of experimental data shows that multiple cycles of electroforming lead to an increase in the density of SESs at the silicon–(REE oxide) interface and to a variation in the energy position of levels of traps, which, as a result, brings about a change in their charge state. In the case of an n-type substrate, an increase in the density of SESs results in the formation of acceptor traps whose levels are above the Fermi level. Alternatively, some fraction of the traps with levels located previously below the Fermi level change their energy position to that above the Fermi level. Similarly, for a p-type substrate, a fraction of traps with levels located earlier above the Fermi level change their position and shifts to a position below the Fermi level (or new donor traps are formed with levels located below the Fermi level.

REFERENCES

1. P. H. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, J. Appl. Phys. **50**, 5847 (1979).

2. G. J. Gerardi, E. H. Poindexter, P. J. Caplan, and N. M. Johnson, Appl. Phys. Lett. **49**, 348 (1986).
3. D. L. Griscom, E. J. Friebele, and G. H. Sigel, Solid State Commun. **15**, 479 (1974).
4. S. Ling, A. El-Sayed, F. Lopez-Gejo, M. B. Watkins, V. V. Afanas'ev, and A. L. Shluger, Microelectron. Eng. **109**, 310 (2013).
5. D. L. Griscom, J. Appl. Phys. **58**, 2524 (1985).
6. V. A. Gritsenko, Yu. N. Novikov, A. V. Shaposhnikov, and Yu. N. Morokov, Semiconductors **35**, 997 (2001).
7. B. L. Yang, H. Wonga, K. Kakushima, and H. Iwai, Microelectron. Reliab. **52**, 1613 (2012).
8. A. N. Nazarov, Y. V. Gomeniuk, Y. Y. Gomeniuk, H. D. B. Gottlob, M. Schmidt, M. C. Lemme, M. Czernohorsky, and H. J. Osten, Microelectron. Eng. **84**, 1968 (2007).
9. H. J. Quah and K. Y. Cheong, Mater. Chem. Phys. **130**, 1007 (2011).
10. M. Kouda, PhD Thesis (Tokyo Inst. of Technology, 2011).
11. M. B. Shalimova, V. S. Afanaskov, and E. N. Khavdei, Vestn. Samar. Gos. Univ. **104**, 107 (2013).
12. V. A. Rozhkov and A. I. Petrov, Sov. Tech. Phys. Lett. **11**, 21 (1985).
13. K. B. Jinesh, Y. Lamy, E. Tois, and W. F. A. Besling, Appl. Phys. Lett. **94**, 252906 (2009).
14. D. K. Schroder and J. A. Babcock, J. Appl. Phys. **94**, 1 (2003).
15. D. S. Ang, C. J. Gu, Z. Y. Tung, A. A. Boo, and Y. Gao, Microelectron. Reliab. **54**, 663 (2014).

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