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PHYSICS OF SEMICONDUCTOR DEVICES

Control over Carrier Lifetime in High-Voltage *p–i–n* Diodes Based on $In_xGa_{1-x}As/GaAs$ Heterostructures

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Abstract—The possibility of controlling the effective lifetime of nonequilibrium carriers by varying the lattice mismatch between the interfaced materials of a heterostructure has been studied on the example of InGaAs/GaAs heterostructures. It was found that, at a given composition (thickness) of a lightly doped layer of the InGaAs alloy, the nonequilibrium carrier lifetime depends on its thickness (composition), which enables variation of the nonequilibrium carrier lifetime from several nanoseconds to a microsecond without any significant change in the concentration of mobile carriers. The results obtained were used to fabricate pulse p^+–p^0–π–n^0–n^+ diodes with blocking voltages of up to 500 V, which can switch currents of ≳10 A and have recovery times no longer than 10 ns.

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1. INTRODUCTION

To raise the operation speed of numerous types of semiconductor devices, and especially high-power pulse devices, it is necessary to shorten the lifetime of nonequilibrium carriers in the base layers of the device without loss of working blocking voltages or any noticeable increase in the forward-voltage drops. The previously developed method for fabrication of GaAs-based high-voltage *p–i–n* structures with controlled distribution of residual impurities [1] gives no way of simultaneously making their operation speed faster and reverse voltages higher.

Previously, attempts have been made to raise the operation speed of structures of this kind by creating additional effective recombination centers in lightly doped parts of the structure by (i) irradiating *p–i–n* diodes with γ photons [2], (ii) introducing water vapor in a controlled way into hydrogen fed into the growth chamber during epitaxy [3, 4], and (iii) replacing hydrogen with argon during the growth process [5]. In the latter case, the spectrum of deep-level traps in lightly doped GaAs layers changes; specifically, the effect of the *EL*2 defect becomes predominant, which leads to a dramatic, by an order of magnitude, decrease in the effective lifetime of nonequilibrium carriers. However, despite the certain success of the methods listed above, the results obtained in improving the operation speed of these diodes (recovery times of 30–80 ns) fail to fully satisfy the needs of modern electronics.

Another technique for modifying the ensemble of intrinsic defects in epitaxial films is isovalent doping. As the content of isovalent impurities in layers gradually increases, the crystal quality of epitaxial films first improves and, as a rule, the content of electrically active deep-level impurities in these layers decreases [6]. Then, as the content of the isovalent component in elastically strained layers increases further, the concentration of the already existing active deep-level defects grows and new defects of this kind appear. For example, *EL*2 defects with large carrier capture cross-sections are frequently found in epitaxial layers of GaAs-based alloys [7]. As the lattice mismatch between the layer and the substrate increases further and the so-called critical strains are reached, there occurs partial relaxation of elastic strains, with the formation of misfit dislocations. At even larger mismatches, the alloy layer is strongly plastically strained, with the residual internal strains reaching their maximum values and the density of misfit dislocations sharply increasing.

The appearance of misfit dislocations in the layers stimulates the generation of additional defects and, accordingly, deep-level traps. It follows from a number of reports (e.g., [8]) that dislocations or intricate complexes of defects produced by the plastic strain may be responsible for the appearance of additional *EL*2 defects in GaAs. In addition, such additional excess defects as misfit dislocations can capture carriers (although their behavior differs somewhat from that of single traps). For example, the appearance of an electron trap with energy E_C – 0.68 eV in a plastically deformed GaAs has been attributed to 60° dislocations [9]. Similar results have been reported for GaAsSb/GaAs [10] and InGaAs/GaAs heterostructures [11].

The effect of the lattice mismatch in device structures on the operation speed of devices based on these structures is inadequatly understood. This study is con-

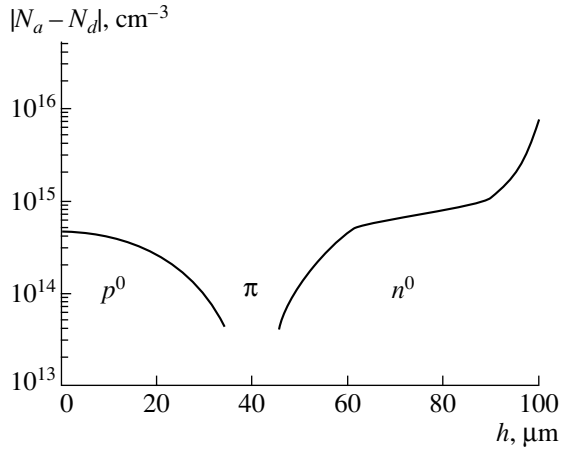

Fig. 1. Concentration profile of free carriers in a structure with a gradual p^0–π–n^0 junction.

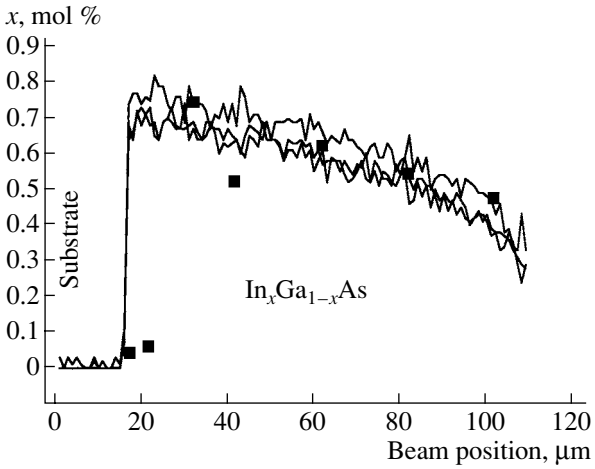

Fig. 2. InAs distribution across the thickness of the $In_xGa_{1-x}As$ layer. The lines correspond to continuous scanning; the points represent the results of local analysis of the chemical composition of the layer.

cerned with the possibility of reducing the effective lifetime of nonequilibrium carriers by controlled generation of intrinsic defects in the base layers of semiconductor devices; these defects are caused by the lattice mismatch between the interfaced materials of the heterostructure, with the blocking voltages and forward-voltage drops across the high-voltage junctions remaining unchanged.

2. SAMPLE FABRICATION AND EXPERIMENTAL RESULTS

Epitaxial layers of the $In_xGa_{1-x}As$ alloy with InAs content of up to 5% were grown on GaAs substrates by liquid-phase epitaxy. The layer thickness was varied from 10 to 85 μm. The *p*-GaAs ⟨100⟩, ⟨111⟩Ga, and ⟨111⟩As substrates doped with zinc to $(1–5) \times 10^{18}$ cm^{-3} were used. The epitaxial growth was performed from a confined In–Ga–As melt in the atmosphere of hydrogen in a quartz boat, with the crystallization occurring in cooling of the system from the crystallization onset temperatures (800–900°C) down to room temperature. The liquid-phase composition to be used to obtain solid-solution layers of the required composition was determined by calculation in terms of the quasi-regular approximation model (the parameters of the model necessary for the calculation were taken from [2]) with account of the elastic strains appearing because of the lattice mismatch between the layer and the substrate [12, 13]. The thickness of the epitaxial layer of a chosen composition was set by the height of the melt layer between GaAs substrates, i.e., by the thickness of the spacer between the substrates.

The content of electrically active defects in the epitaxial layers grown in this way depends on the content of residual (background) impurities in the melt and growth system, the temperature and duration of pregrowth annealing of the melt, the flow rate and moisture content of hydrogen, and the mode of crystallization of a film in the cooling of the system. When performing the growth process, the temperature as a function of time and the flow rate of hydrogen containing $\lesssim$3 ppm of water vapor and $\lesssim$1 ppm of oxygen were chosen in such a way that the epitaxial layer of the alloy was grown as a gradual p^0–π–n^0 junction with a free carrier concentration in the π layer equal to about 10^{13}–10^{14} cm^{-3} or lower. Figure 1 shows a typical distribution of free carriers across the p^0–π–n^0 structure as determined from the capacitance–voltage dependences of the Schottky barrier, measured in layer-by-layer etching-off.

The content of InAs in the epitaxial layers of the solid solution was determined from X-ray spectral microprobe analysis using a Camebax system. A continuous scanning (in three channels) and point (local along the coordinate) analysis of the chemical composition of the samples were performed. Figure 2 shows the distribution of InAs across a layer of the $In_xGa_{1-x}As$ alloy.

To obtain the fastest diodes, the thickness and composition of the heteroepitaxial layer were chosen so as to exceed the critical thickness that corresponded to the onset of relaxation defect formation in pseudomorphic films, i.e., to provide generation of a sufficient number of effective recombination centers in the base layers of the device. In doing so, it was important to preclude strong plastic strain of this layer. The critical layer thickness was calculated in terms of the energy-balance model [14].

The effective lifetime of nonequilibrium carriers (τ_{eff}) in the base regions was found by measuring the decay time of the charge accumulated on applying a pulse of reverse voltage to the diode (the Lax method). The values of τ_{eff} were found from the duration t_1 of the stage of high-reverse conductivity for the model of switching

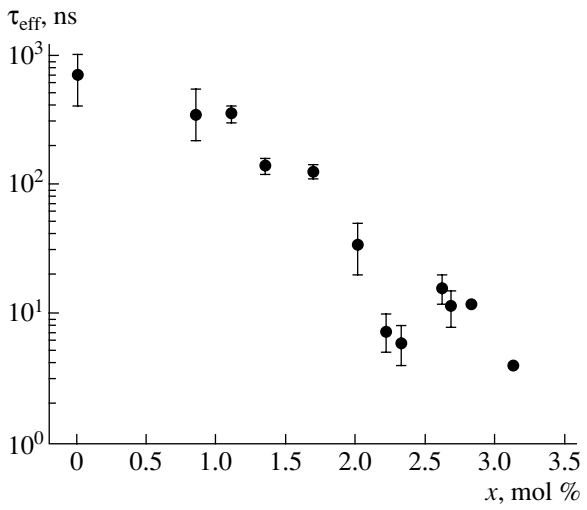

Fig. 3. Effective lifetimes τ_{eff} of nonequilibrium carriers in *p–i–n* $In_xGa_{1-x}As$ structures grown on GaAs substrates. The parameter x characterizes the film composition at the layer–substrate interface.

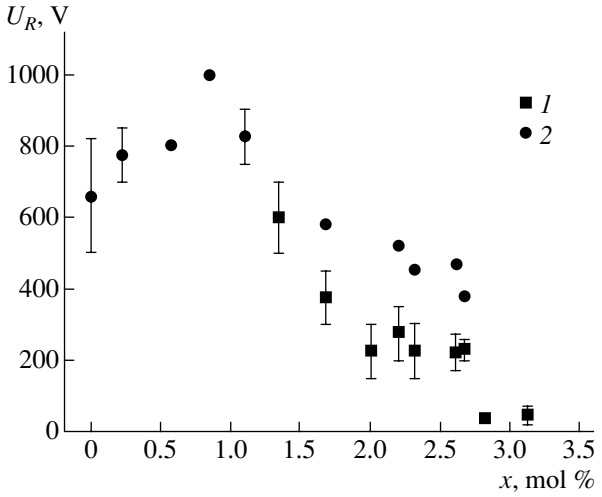

Fig. 4. Blocking voltage U_R vs. the composition of $In_xGa_{1-x}As$ at leakage currents $I_R \le 0.1$ mA. (*1*) Samples with an area of 0.01 to 0.1 cm^2, cleaved out from epitaxial wafers, and (*2*) samples with an etched-out mesa structure of area $S = 7 \times 10^{-3}$ cm^2.

of planar diodes in a circuit with a limiting resistance [15]. The conditions under which $t_1 \approx \tau_{eff}$ are as follows: the duration of forward-current pulses considerably exceeds τ_{eff}, the ratio between the amplitudes of the forward and reverse currents is chosen to be $I_f/I_r \le 5$–6, and diodes with a large base width W are studied ($W/L_d > 3$, where L_d is the carriers' diffusion length).

The values of τ_{eff} measured in this way for structures with varied In content in the base regions comparable in thickness are presented in Fig. 3. The effective lifetime sharply decreases after the calculated critical thickness h_c of the onset of plastic deformation is exceeded. Accordingly, the recovery times of the diodes also decrease, with the time in which the reverse current decays to a 0.1 level falling from several hundred nanoseconds to several nanoseconds.

It should be noted that nanosecond measurements necessarily involve circuit distortions of the switching oscilloscope patterns. In the case under consideration, the total duration of pulse edges was 3–4 ns, the maximum forward current was ~10 A, and the load resistance in the diode circuit was several ohms. This may account for the absence of a clearly pronounced plateau in the characteristics of the fastest of the diodes. It was found that, on raising the I_f/I_r ratio within the range of forward currents corresponding to a high injection level, the duration of the high-reverse-conductivity stage (t_1) becomes somewhat shorter, which may be due to a decrease in the injection efficiency of the emitters.

Figure 4 shows the results of measuring the blocking voltage U_R for the $In_xGa_{1-x}As$/GaAs samples under study. We attribute the steep fall of U_R for layers with high InAs content at $x \gtrsim 2.7$ mol %, i.e., at lattice mismatches $f \gtrsim 1.9 \times 10^{-3}$ at the layer–substrate interface, to the onset of the so-called strong plastic strain.

At a dc forward current of 0.5 A, the forward voltage drops across the diodes with a short time τ_{eff} did not exceed 2.5 V. The capacitance of the diodes was weakly voltage-dependent in the range 0–200 V: $C(U = 0) \approx 0.1$ pF/cm^2 and $C(U = 200\ V) \approx 0.04$ pF/cm^2.

3. CONCLUSIONS

(i) The possibility of reducing the effective lifetimes of nonequilibrium carriers by controlled variation in the lattice mismatch between the interfaced materials of device heterostructures was demonstrated.

(ii) Only the InGaAs/GaAs system was tested, but the approach suggested can be applied to devices based on other heterosystems, and not only on those with III–V compounds, and on systems produced by other epitaxial growth methods.

(iii) The optimal relationship between the thickness and composition of the base layers of the $In_xGa_{1-x}As$ alloy was found, which has potential to markedly improve the operation speed of high-voltage diodes.

(iv) High-voltage *p–i–n* diodes were fabricated, which surpass in operation speed (recovery time) the existing analogues, including GaAs and SiC Schottky diodes produced by the leading manufacturers [16].

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