

A High Voltage CMOS Voltage Level Converter for a Low Voltage Process

V. V. Shubin*

*Department of Semiconductor Devices and Microelectronics,
Novosibirsk State Technical University, Novosibirsk, 630073 Russia
e-mail: shubin@nzpp.ru

Received March 23, 2021; revised October 6, 2021; accepted October 6, 2021

Abstract—A new high-voltage CMOS voltage level converter designed for manufacturing in low-voltage technological processes is presented. The features of the construction, operation and application of a high-voltage CMOS converter using low-voltage transistors are described. The new high-voltage CMOS voltage level converter is compared with its analog in terms of dynamic characteristics. The described high-voltage voltage level converter, in comparison with the alternative circuit, has a higher response speed (~14% in the worst case), and also allows us to form a higher quality output waveform with the minimal distortion.

Keywords: converting equipment, CMOS voltage level converters, speed, quality, reliability, power consumption

DOI: 10.1134/S1063739722020081

INTRODUCTION

There are a number of reasons that determine the importance of the research topic for various voltage level converters:

- The need to couple the interfaces of electronic systems with different power sources.
- Coordination of circuits with different voltage levels of internal signals.
- Reducing the power consumption of electronic systems with several threshold voltages of MOS transistors [1].
 - Application in ESD upstream protection circuits [2].
 - Use in systems with the standby mode [3].
 - Application in the mode of erasing the information of the memory cell of the flash memory for the organization of F-N tunneling (Quantum-mechanical effect of tunneling according to Fowler–Nordheim), etc. [4, 5].

Modern Systems-on-Chip (SoC) for known reasons often require the use of several power supplies of different voltage levels. In this case, the laws of scaling linear dimensions require a decrease in the operating voltages of the power supplies, since a decrease in the channel length of MOS transistors leads to a decrease in their breakdown voltages. The use of MOS transistors with an increased breakdown voltage within one technological process requires the introduction of new materials and additional expensive technological operations.

This article presents a high-voltage CMOS voltage level converter in which, due to the circuitry solutions,

the use of standard low-voltage MOS transistors is allowed.

A description of several original circuits of a high-voltage CMOS voltage level converter, features of their operation and application, as well as the results of modeling and comparing these circuit options are proposed. Section 1 describes a traditional voltage level converter and its disadvantages, and Section 2 describes the basic circuit of a known high-voltage CMOS voltage level converter and its operation. Section 3 presents two circuits of the new high-voltage CMOS voltage level converter and their differences from the basic circuit, and Section 4 presents the results of modeling and comparing high-voltage CMOS voltage level converter circuits.

1. TRADITIONAL VOLTAGE LEVEL CONVERTER

The basic circuit of the traditional CMOS voltage level converter, presented in Fig. 1, is usually called a 10-transistor circuit [6–9].

A traditional CMOS voltage level converter can be broken down into three functionally independent blocks:

- A generator of direct and inverse input signals of low amplitude (GND/VddL), made on two series-connected inverters on transistors P1–P2 and N1–N2 (A).
- A converter of an input signal of low amplitude (GND/VddL) into a signal of high amplitude (GND/VddH), built on a flip-flop of two half-latches covered by feedback, on transistors P3–P4 and N3–

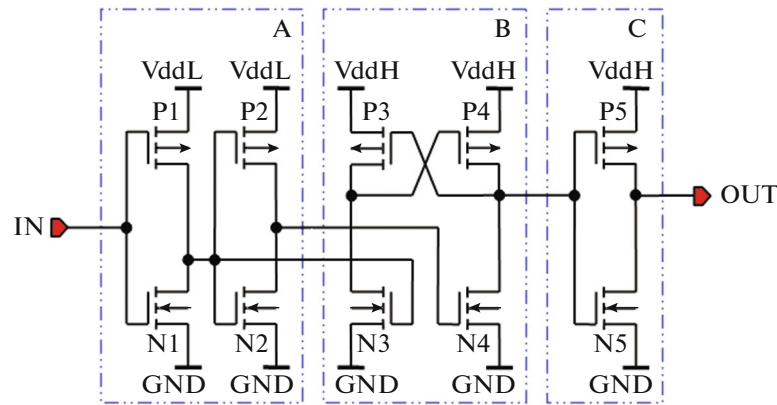


Fig. 1. 10-Transistor circuit of the traditional CMOS voltage level converter.

N4 and powered from a power supply with high amplitude (GND/VddH) (B).

- High-amplitude signal output buffer (GND/VddH) made on an inverter from CMOS transistors P5–N5 (C).

Sometimes a single inverter is used as a generator of direct and inverse input signals of low amplitude (GND/VddL). In this case, the input of this inverter is an input signal and at the same time a source of a direct signal, and the output is an inverse one [10].

Modeling and analyzing the circuitry of a traditional CMOS voltage level converter helps to reveal a number of disadvantages.

A conventional CMOS voltage level converter requires a downward bias of both half latches of the trigger of the low-amplitude input signal (GND/VddL) to high-amplitude signal (GND/VddH) to ensure the stable operation of a traditional CMOS voltage level converter. This condition is fulfilled by a significant decrease in the conductance of the pull-up network circuit on the P3–P4 transistors in comparison with the conductance of the pull-up network on the N3–N4 transistors. This circumstance, in turn, leads to an increase in the transient time when the signal at the input of the output buffer of the traditional CMOS voltage level converter is switched from a low voltage GND level to a high voltage VddH level. The described feature leads to an increase in the switching time of the formation of a high level VddH signal at the input of the output buffer and, therefore, to an increase in the propagation delay time of the low GND voltage level output signal at the output of a traditional CMOS voltage level converter OUT. In addition, due to the increased time of the transient process, the dynamic current consumption increases [11, 12].

Another significant disadvantage of using a traditional CMOS voltage level converter is the low value of its operating voltage caused by the limited capabilities of any technological process by the magnitude of the breakdown voltage of MOS transistors. To eliminate

this shortcoming, the scheme presented in the next section is used.

2. BASIC CIRCUIT OF A HIGH VOLTAGE CMOS VOLTAGE LEVEL CONVERTER

The patent for the invention [13] describes the basic circuit of a high-voltage voltage level converter (BCHVLC) and its operation. A diagram of this known device is shown in Fig. 2. As described in this description, the basic CMOS high voltage level converter contains two functional blocks, inverter (A) and latch circuitry (B). In turn, the latch circuit consists of the latch assembly (C) and the voltage distributor (D).

Inverter (A) is a MOS transistors P1 and N1 and is a generator of input direct and inverse signals for latch circuits (B). Inverter (A) is powered by a low voltage power supply VddL and therefore operates in the range of low amplitude signals GND–VddL.

The core of this circuit solution lies in the fact that in the latch assembly C a traditional voltage level converter between P-type transistors P2 and P3 (pull-up network) and N-type transistors N2 and N3 (pull-down network) introduced a voltage distributor on P-type transistors P4–P7 and N-type transistors N4–N7 forming a cascode connection of these transistors. As the simulation shows, such a change in the circuit allows redistributing the high level voltage VddH between all latch B transistors, so that between any two terminals of any MOS transistor, the potential difference does not exceed $\sim 1/3$ VddH in any static mode.

Thus, if the IC manufacturing process is limited to a voltage of $\sim 1/3$ VddH, and the voltage VddH is required at the output of the voltage level converter circuit, then this solution allows this condition to be fulfilled without the additional costs related to making the necessary changes to the technological process to increase its operating voltage.

In addition, we note another useful area of application described by the basic circuit of the high-voltage

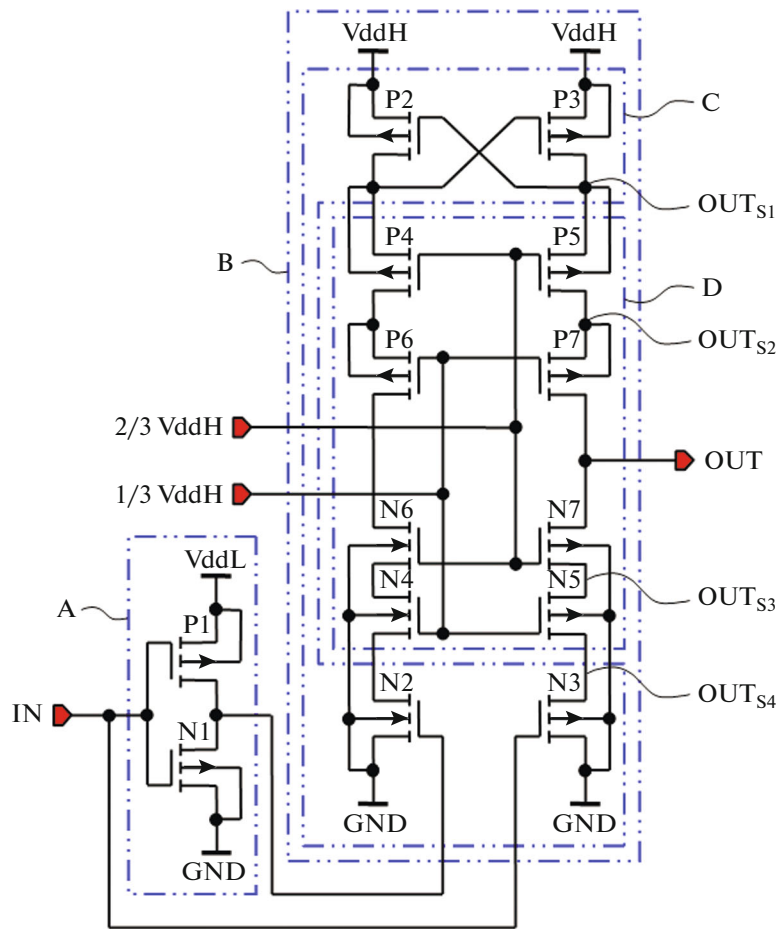


Fig. 2. Basic circuit of a high-voltage CMOS voltage level converter: A, inverter; B, latch circuit; C, latch assembly; D, voltage distributor.

voltage level converter. Depending on the connection of the OUT output terminal, the circuit allows the output voltage range to be shifted and used directly as an offset circuit or as an OUT_{S3} and OUT_{S4} intermediate voltage level converter. A graph of the changes in the switching voltages of BCHVLC when using the outputs OUT, OUT_{S1}, OUT_{S2}, OUT_{S3}, and OUT_{S4} without a load is shown in Fig. 3.

However, the described solution has several disadvantages:

- At the outputs OUT, OUT_{S1}, OUT_{S2}, OUT_{S3}, and OUT_{S4}, latch circuits B BCHVLC are formed by voltages with an amplitude of 0–VddH, OUT_{S1}–~2/3VddH–VddH, OUT_{S2}–~1/3VddH–VddH, OUT_{S3}–0–~2/3VddH, and OUT_{S4}–0–~1/3VddH. The indicated approximations of the values of the levels differ from the required total by 1–2 values of the threshold voltages of the MOS transistors. This difference, when used in CMOS applications, results in static current consumption.

- The waveforms of the output signals have significant distortion, in contrast to those generated by the standard CMOS logic gates.

- The use of a cascode circuit for switching on MOS transistors in the latch circuit B BCHVLC forms chains of series P-type transistors P2, P4, P6 and P3, P5, P7 and N-type transistors N2, N4, N6 and N3, N5, N7, which limits the output load capacity and thereby reduces the speed of the circuit.

One of the ways to increase the value of the output load capacity is to increase the slope of each individual MOS transistor by increasing their channel width W in the chain of all series-connected transistors. However, this method leads to an increase in the crystal area and increases the input capacity of the latch circuit (B), which again slightly reduces the overall performance.

The second way to increase the output load capacity is circuit buffering. The high-amplitude output buffers GND–VddH are designed to amplify the output signals when operating under a heavy load. However, this method requires additional constructive or technological efforts to protect them from excessively

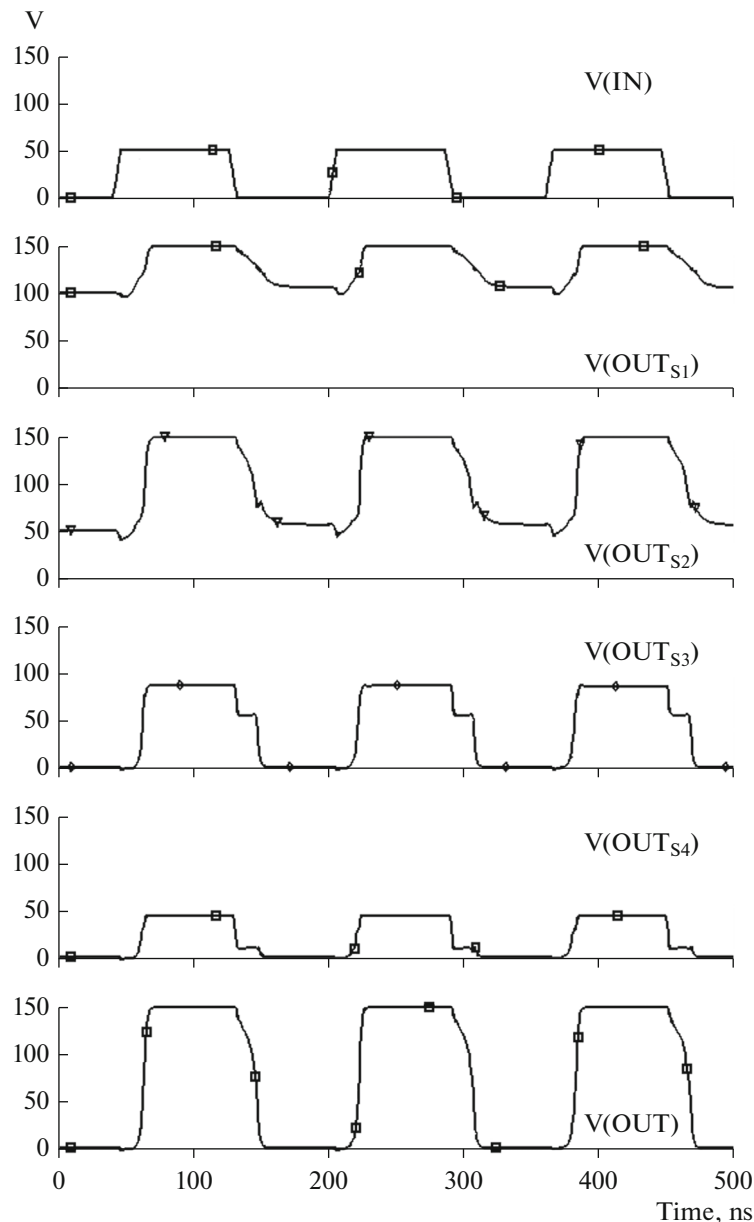


Fig. 3. Graph of changes in the switching voltage BCHVLC in time at the outputs OUT, OUT_{S1}, OUT_{S2}, OUT_{S3}, and OUT_{S4} without a load.

high voltages [14], and also increases the chip area and adds time for the signal to pass through the buffer.

3. NEW HIGH VOLTAGE CMOS VOLTAGE LEVEL CONVERTER

To increase the speed of operation of the basic high-voltage CMOS voltage level converter, two design solutions have been proposed, which can partially reduce these disadvantages.

Scheme 1 of a new high-voltage CMOS voltage level converter (NVPUN-1) [15] differs from the BCHVLC circuit by the connection of the gates of the

P-type transistors P2 and P3 of the latch node (C). In the proposed scheme, the gate of transistor P2 is connected to the drain of the transistor P5 and the substrate and source of the transistor P7, and the gate of transistor P3 is connected to the drain of transistor P4 and the substrate and source of transistor P6 of the voltage distributor (D) as shown in Fig. 4.

Another circuit 2 of the new high-voltage CMOS voltage level converter (NHVLC-2) [16] differs from the BCHVLC and NHVLC-1 circuits by the connection of the gates of the P-type transistors P2 and P3 of the latch node (C). In the NHVLC-2 circuit, the gate of the P2 transistor is connected to the drains of the P7

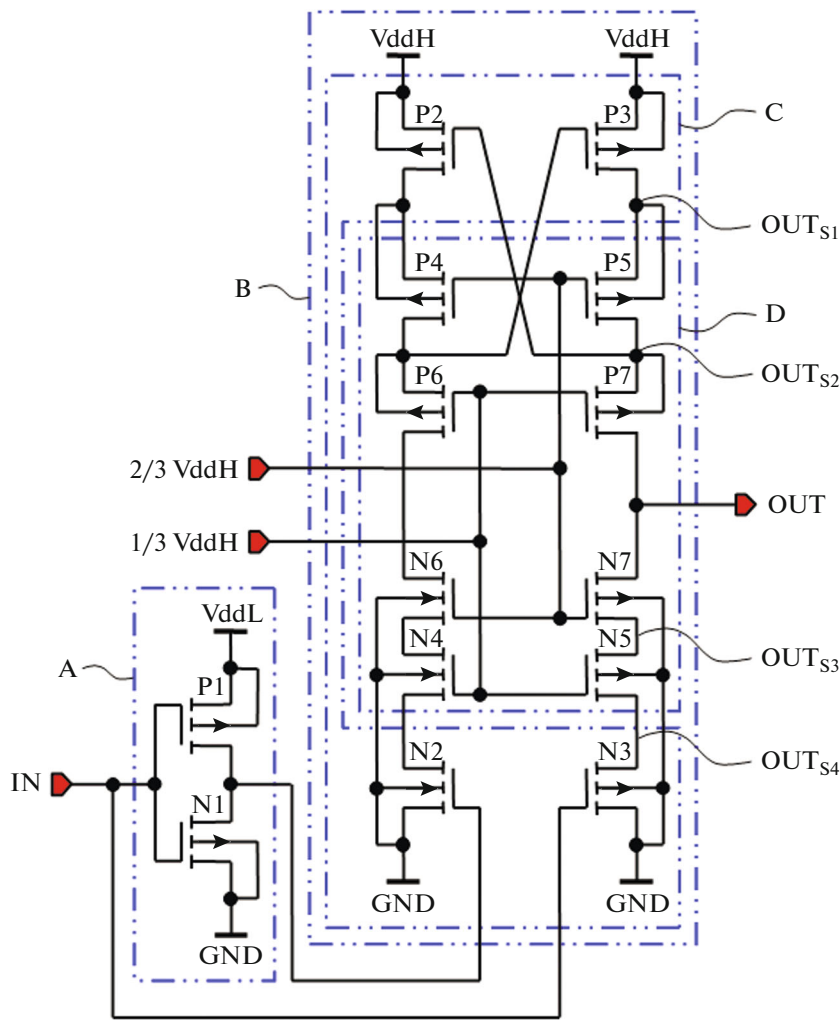


Fig. 4. Scheme 1 of the new high-voltage CMOS voltage level converter. (See Fig. 2 for designations.)

and N7 transistors; and the gate of the P3 transistor, with the drains of the P6 and N6 transistors of the voltage distributor (D) as shown in Fig. 5.

Among the limitations of the characteristics of the technological process, one of the main ones is the maximum (or breakdown) voltage of the source-drain of MOS transistors in the closed state, after which a breakdown occurs. As a rule, it is the source-drain breakdown voltage that determines the maximum permissible value of the operating voltage of the technological process.

The proposed connection, in addition to speeding up the process of converting the input signal, in contrast to the basic circuit, increases the applied gate-to-substrate voltage in the operating mode by 2–3 times up to VddH (in the NHVLC-2 circuit). However, given the fact that the breakdown voltage of the source-drain remains unchanged, and the gate-substrate voltage in any technological process, as a rule, is several times (5–10 times) higher than the source-

drain voltage, this formal change does not have a negative effect on the characteristics of the circuit.

4. RESULTS OF MODELING AND COMPARING HIGH-VOLTAGE CMOS VOLTAGE LEVEL CONVERTER CIRCUITS

Comparing different circuit diagrams of electronic devices that perform the same function is not an easy task, given the need to create the same conditions for each of them. Therefore, in order to achieve more reliable results, it is necessary to accept a number of agreements based on which optimization and comparison are carried out. In this study, the following agreements are accepted:

- The channel length (L) of all transistors is equal to the minimum value of the selected technological process.
- The ratio of the channel widths of all transistors W_P/W_N is determined by the matching of their resistances in the open state. This ratio in the CMOS valve

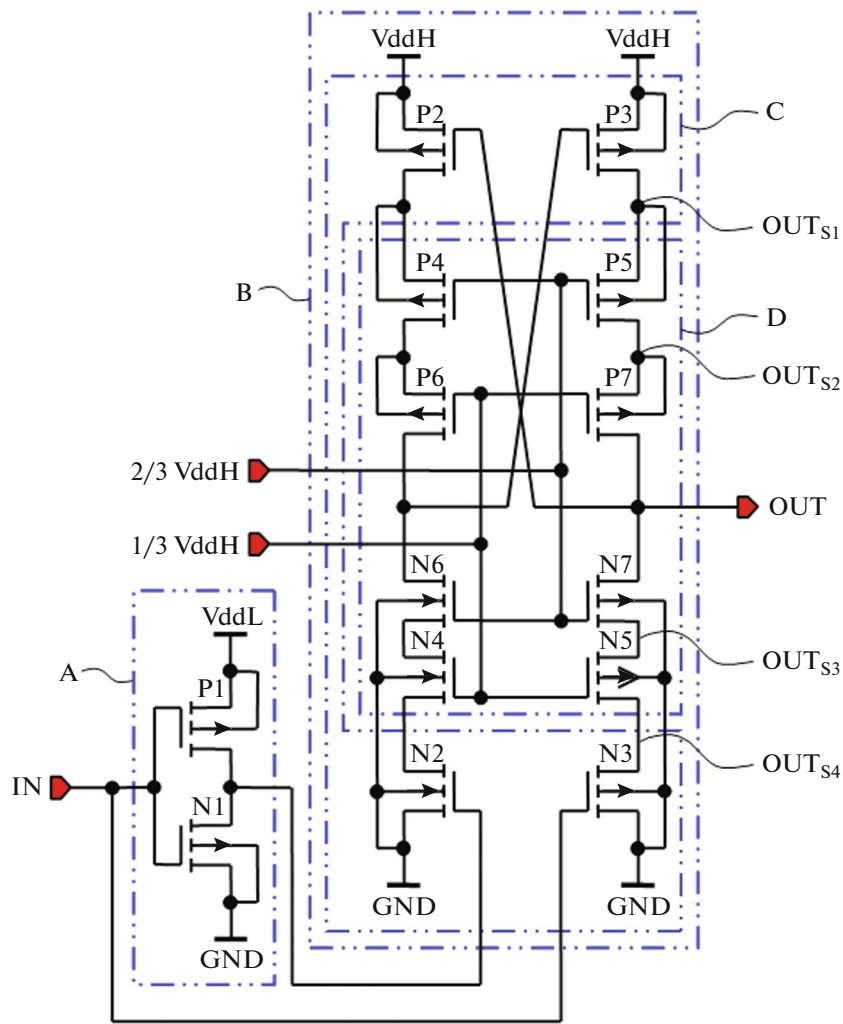


Fig. 5. Scheme 2 of the new high-voltage CMOS voltage level converter. (See Fig. 2 for designations.)

provides the same transfer characteristics when the input signal changes from low to high voltage and from high to low [12].

- $V_{ddL} = 5\text{ V}$, $V_{ddH} = 15\text{ V}$.
- High voltage CMOS voltage converter in the input signal range U_{IN} with amplitude from 0 to 5 V and output signal U_{OUT} with amplitude from 0 to 15 V.
- Duration of full edges of the input signal U_{IN} , positive t_R , and negative t_F : 6 nS.
- Output load capacity C_L is 3 pF.
- The schemes are compared according to the simulation results under the same conditions described above.

To assess the dynamic characteristics of the transformation, we use the generally accepted parameters:

- t_{PLH} and t_{PHL} are the time delays of the positive and negative edges from 0.5 value of the voltage amplitude of the input signal U_{IN} up to 0.5 value of the amplitude of the output signal voltage U_{OUT} ;

- t_R and t_F are the times of the duration of the positive and negative edges of the output signal measured from 0.1 to 0.9 values of the amplitude of the output signal.

- The numerical values are set by choosing the worst-case values within a single scheme.

The listed parameters are presented in Fig. 6.

The modeling results and graphs were obtained using the PSpice and Probe modules of OrCAD 9.2 f. Cadence, using a 3rd level mathematical model and 3 μm CMOS process data. The calculations were carried out in the transient DC time analysis mode for direct current. Graphs of the results of modeling the operation of the basic (BCHVLC) and new high-voltage CMOS voltage level converter (NHVLC-1, NHVLC-2) are presented.

The graphs of the simulation results clearly demonstrate the superiority in speed of the new high-voltage CMOS voltage level converter (NHVLC-1 and NHVLC-2) over the basic circuit (BCHVLC), and the

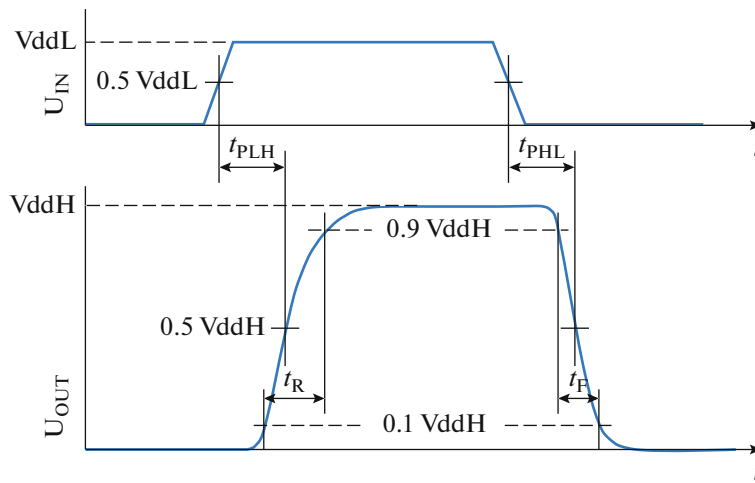


Fig. 6. Graphical presentation of monitored parameters.

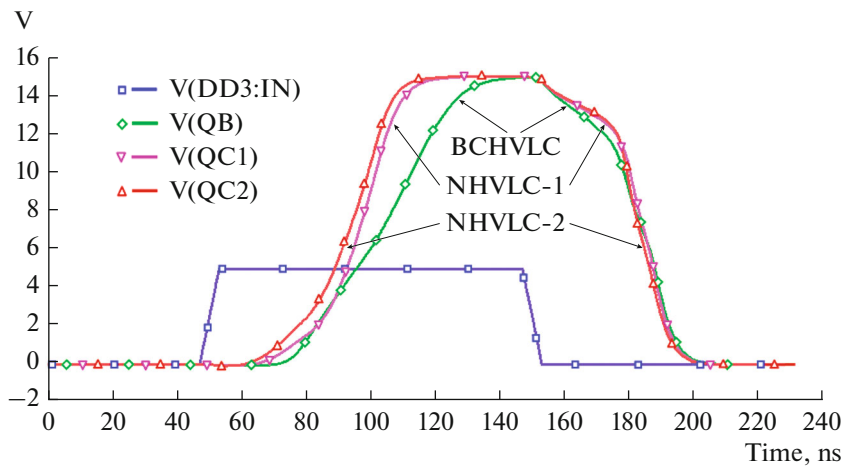


Fig. 7. Graphs of the results of modeling the operation of the basic (BCHVLC) and new high-voltage CMOS voltage level converter (NHVLC-1, NHVLC-2), obtained using the probe module of the OrCAD 9.2 program.

numerical values of the time parameters and the results of their comparison are presented in Table 1. It can be seen that when comparing the values for the

worst case, which are taken as the base values when drawing up the specification data of the technical specifications, any of the proposed circuit options for

Table 1. Numerical representation of the simulation results of the compared high-voltage CMOS voltage level converters: BCHVLC with NHVLC-1 and NHVLC-2

Parameter	BCHVLC, ns	NHVLC-1, ns	NHVLC-2, ns	Outperformance NHVLC-1/NHVLC-2 compared to BCHVLC in terms of speed, %
t_{PLH}	55.041	47.305	44.413	14.055/19.309
t_{PHL}	32.997	33.823	32.505	-2.503/1.491
t_R	43.644	28.761	31.374	34.101/ 28.114
t_F	32.55	29.187	26.984	10.332/17.100

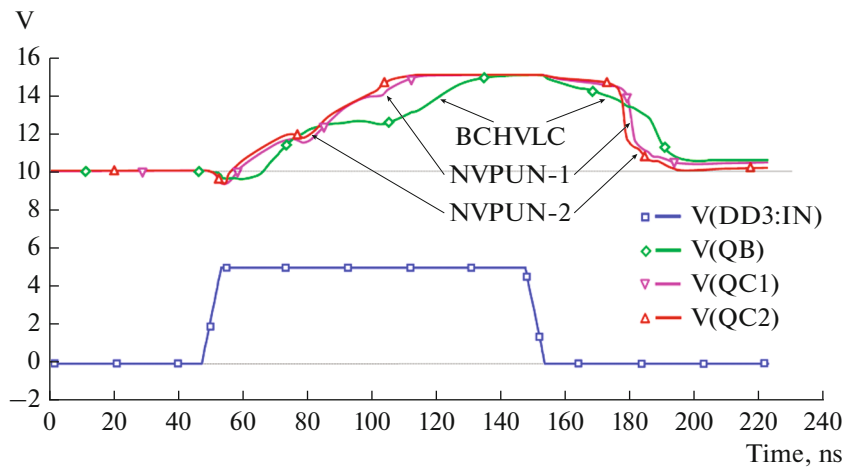


Fig. 8. Graphs of the results of modeling the operation of the basic (BCHVLC) and new high-voltage CMOS voltage level converter (NVPUN-1, NVPUN-2) as a shift circuit, obtained using the probe module of the OrCAD 9.2 program.

the new high-voltage CMOS voltage level converters, NHVLC-1 and NHVLC-2, surpasses the basic circuit (BCHVLC) in speed.

In addition, the proposed circuits of the new high-voltage CMOS voltage level converter (NHVLC-1 and NHVLC-2) have additional possibilities of being used as a voltage level shift circuit and (or) as a converter of the input signal up to the level $2/3 V_{ddH}$, as shown by the plots of the voltage graphs in Fig. 3.

However, when using the new high-voltage CMOS voltage level converter (NHVLC-1 and NHVLC-2) as a shift circuit, two disadvantages should be noted:

- The signal level differs from the desired value by approximately the value of the threshold voltage.
- The low quality of the shape of the fronts, both in duration and in the presence of a distortion of the waveform.

As the graphs of the simulation results show, the use of the proposed circuits of the new high-voltage CMOS voltage level converter (NHVLC-1 and NHVLC-2) as a shift circuit helps to significantly reduce the amount of distortion of the shape of the edges and their duration (see Fig. 8).

The increased duration of the voltage level fronts leads to a longer state time in which the circuits between the power supply of a high voltage level V_{ddH} and a low voltage level GND are simultaneously open conducting circuits of the P-channel PUN (Pull-Up Network) transistors and N-channel PDN (Pull-Down Network) transistors. This condition leads to an increase in the dynamic current consumption and to a decrease in the operating frequency of the basic circuit of a high-voltage CMOS voltage level converter (BCHVLC), in comparison with the proposed new circuits (NHVLC-1 and NHVLC-2).

CONCLUSIONS

This article describes two circuits of a new high-voltage CMOS voltage level converter, NHVLC-1 and NHVLC-2, for a low-voltage technological process. Their electrical schematic diagrams are presented, and a description of the functional device and their operation, based on the original method of the cascode switching of CMOS transistors, is given.

In the new high-voltage CMOS voltage level converter, NHVLC-1 and NHVLC-2, a connection is used, in which the applied gate-substrate voltage rises up to V_{ddH} (in the NHVLC-2 scheme). However, due to the fact that the breakdown voltage of the source-drain remains unchanged, and the voltage of the gate-substrate in any technological process, as a rule, is several times (5–10 times) higher than the voltage of the source-drain, this feature allows the proposed circuit to be used in a low-voltage process.

The simulation results demonstrate that the dynamic performance of the new high voltage CMOS converter of the voltage level for the low voltage technological process are superior to the analogous characteristics of the basic high voltage level CMOS voltage level converter. The switching delay time of the new CMOS high voltage voltage level converter (NHVLC-1 and NHVLC-2) is reduced by at least ~14%; and the duration of the fronts, by at least ~28%. In addition, the use of the new high-voltage CMOS voltage level converter NHVLC-1 and NHVLC-2 as a shift circuit improves the quality of the output signal shape, leads to a decrease in the dynamic current consumption, and an increase in the operating frequency compared to the basic circuit of a high-voltage CMOS voltage level converter.

REFERENCES

1. Kursun, V. and Friedman, E.G., *Multi-Voltage CMOS Circuit Design*, Chichester, West Sussex: Wiley, 2006.
2. Ker, M.-D. and Hsu, K.-C., Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS intergrated circuit, *IEEE Trans. Dev. Mater. Reliab.*, 2005, vol. 5, no. 2, pp. 235–249.
3. Shibata, N., Kiya, H., Kurita, S., Okamoto, H., Tan'no, M., and Douseki, T., A 0.5-V 25-MHz 1-mW 256-Kb MTCMOS/SOI SRAM for solar-power-operated portable personal digital equipment - sure write operation by using step-down negatively overdriven bitline scheme, *IEEE J. Solid-State Circuits*, 2006, vol. 41, no. 3, pp. 728–742.
4. Tilke, A., Pescini, L., Stiffler, M., Kakoschke, R., Shum, D., Chan, N., Kim, S., Hecht, V., and Han, K.J., Highly scalable embedded flash memory with deep trench isolation and novel buried bitline integration for the 90-nm node and beyond, *IEEE Trans. Electron Dev.*, 2007, vol. 54, no. 7, pp. 1681–1688.
5. Otsuka, N. and Horowitz, M., Circuit techniques for 1.5 V power supply flash memory, *IEEE J. Solid-State Circuits*, 1997, vol. 32, no. 8, pp. 1217–1230.
6. Koo, K.-H., Seo, J.-H., Ko, M.-L., et al., A new level-up shifter for high speed and wide range interface in ultra deep sub-micron, in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2005, vol. 2, pp. 1063–1065.
7. Kumar, M., Arya, S.K., and Pandey, S., Level shifter design for low power applications, *Int. J. Comput. Sci. Inform. Technol.*, 2010, vol. 2, no. 5, pp. 124–132.
8. Tan, S.C. and Sun, X.W., Low power CMOS level shifters by bootstrapping technique, *Electron. Lett.*, 2002, vol. 38, no. 16, pp. 876–878.
9. Zhang, B., Liang, L., and Wang, X., A new level shifter with low power in multi-voltage system, in *Proceedings of the IEEE International Conference on Solid-State and Integrated Circuit Technology, Shanghai, 2006*, pp. 1857–1859.
10. Gupta, Sh. and Kumar, M., CMOS voltage level-up shifter—a review, *Int. J. Adv. Eng. Sci.*, 2013, vol. 3, no. 3.
11. Baker, J.R., *CMOS. Circuit Design, Layout, and Simulation*, New York: Wiley-IEEE, 2005, 2nd ed.
12. Rabaey, J.M., Chandrakasan, A., and Nikolic, B., *Digital Integrated Circuits: A Design Perspective*, Englewood Cliffs, NJ: Prentice Hall, 2002, 2nd ed.
13. Lee, W.K., CMOS digital level shift circuit, US Patent no. US6099100A, 2008.
14. Pan, D., Li, H.W., and Wilamowski, B.M., A low voltage to high voltage level shifter circuit for MEMS application, in *Engineering Proceedings of the IEEE 15th Biennial University/Government/Industry Microelectronics Symposium, Boise, ID, USA, June 30–July 2, 2003*, 2003, cat. no. 03CH37488.
15. Shubin, V.V., Glukhov, A.V., Bykov, V.M., and Egorkin, A.V., High voltage level converter, RF Patent no. 2712422, 2020.
16. Shubin, V.V., High voltage level converter, RF Patent no. 2702979, 2019.