ISSN 1063-7397, Russian Microelectronics, 2019, Vol. 48, No. 5, pp. 335–339. © Pleiades Publishing, Ltd., 2019.
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A New Voltage Level Shifter For Low-Power Applications

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Received January 15, 2019; revised January 22, 2019; accepted January 22, 2019

Abstract—A new voltage level shifter (NVLS) for low-power applications is presented. Moreover, the original method of forming a circuit with low conductivity used in the NVLS to increase speed and reduce dynamic current consumption is described. The simulation results demonstrate that the switching time delay of the NVLS is reduced by at least 30%. Compared to traditional circuits, the proposed voltage level shifter operates steadily over a wider range of working voltages.

Keywords: converter technology, logical voltage level shifters, operation speed, high speed, quality, reliability

DOI: 10.1134/S1063739719040085

INTRODUCTION

Every year researchers are paying increased attention to voltage level shifters due to the growing number of functional requirements for modern electronic systems (given below):

—interfacing of elements of electronic systems with several power sources;

—matching circuits with different voltage levels of internal signals;

—using in schemes of electrostatic discharge protection (ESD) [1];

—reducing power consumption in systems with multiple threshold voltages of MOS transistors [2];

—using in systems in the standby mode [3];

—using the flash-memory cell information for the organization of F-N tunneling in the erasing mode (quantum-mechanical Fauler-Nordheim effect), etc. [4, 5].

The classification of voltage level shifters according to functional and design-technological features is very complex and requires special description. In this article, we study classical bottom-top level shifters manufactured by CMOS technology [2].

We present the description of a new low-voltage to high-voltage shifter (bottom-up) with two power sources and equivalent direct and inverse output buffers. In addition, the application of the original method of low-conductive circuits that is used to improve the operation rate and reduce the dynamic current consumption, is described.

1. TYPICAL CMOS VOLTAGE LEVEL SHIFTER

Figure 1 shows the scheme of a typical CMOS voltage level shifter (TVLS) [6–10].

A TVLS can be divided into three functionally independent units:

(1) Generator of the input direct and inverse low-amplitude *GND–VDDL* signals on *VT1–VT4* transistors.

(2) Converter of low-amplitude *GND–VDDL* signal to high-amplitude *GND–VDDH* signal on *VT5–VT8* transistors.

(3) Buffer of the output direct high-amplitude *GND–VDDH* signal on *VT9–VT10* transistors. The generator of the input direct and inverse low-amplitude *GND–VDDL* signals creates direct and inverse signals and consists of two inverters connected in series. Both inverters are fed from the low level *VDDL* voltage source. The output of the first inverter on *VT1* and *VT2* transistors forms an inverted signal for the inverse input of the voltage level shifter and serves as the input signal for the second inverter. At the same time, the output of the second inverter on *VT3* and *VT4* transistors forms the direct signal for the direct input of the voltage level shifter. Generator of the input direct and inverse low-amplitude signals *GND–VDDL* can be assembled on one inverter, in which the source of the direct signal is the input of the inverter, while the source of inverse signal is its output.

The converter of the *GND–VDDL* signal from low to high amplitude is made in the form of a trigger latch. Both the converter and buffer of the direct high-amplitude *GND–VDDH* signal are powered from a high-amplitude *VDDH* power source.

For reliable operation of a TVLS, the displacement of transfer characteristics downward is required in

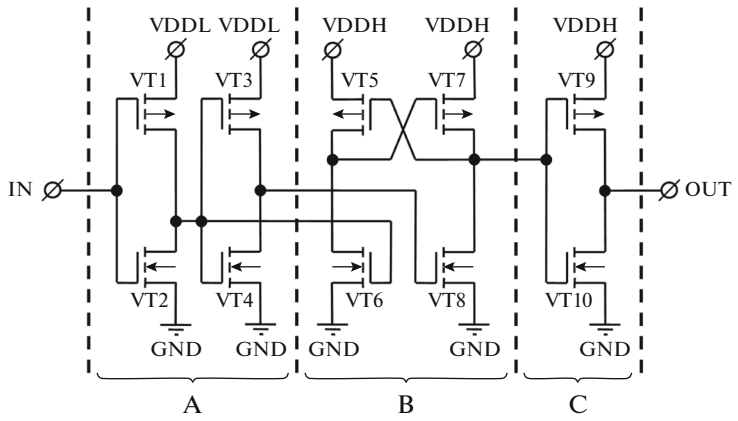

Fig. 1. TVLS: (a) generator of input direct and inverse low-amplitude signals (*GND–VDDL*); (b) low-amplitude signal (*GND–VDDL*) converter into high-amplitude signal (*GND–VDDH*); (c) buffer of output direct high-amplitude signal (*GND–VDDH*).

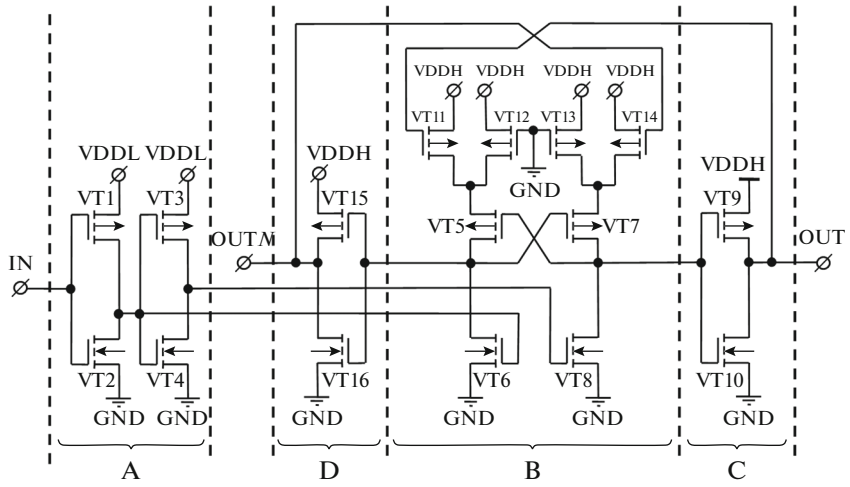

Fig. 2. NVLS for low-power applications. (a) Generator of input low-amplitude direct and inverse signals (*GND–VDDL*); (b) low-amplitude signal (*GND–VDDL*) converter to signal of high amplitude (*GND–VDDH*); (c) buffer of output direct high-amplitude signal (*GND–VDDH*); (d) buffer of output inverse high-amplitude signal (*GND–VDDH*).

each half of the latch trigger of the low-amplitude signal (*GND-VDDL)* converter when the signal is transformed into a high-amplitude signal (*GND-VDDH*). This condition is ensured by reducing the W_P/W_N ratio of the channel widths of the *VT5–VT8* latch transistors. In turn, this leads to an increase in the latch switching time and, consequently, to a loss of speed of a TVLS. In addition, due to the increase in the transient time, the dynamic current consumption increases [9, 11].

Therefore, currently, increased attention is being paid to improving voltage level shifters. Below we present a solution aimed at eliminating these disadvantages.

2. DIAGRAM OF A NEW VOLTAGE LEVEL SHIFTER FOR LOW-POWER APPLICATIONS

A diagram of a new voltage level shifter (NVLS) for low power applications [12] is shown in Fig. 2. This voltage level converter differs from an ordinary one by the presence of a Pull-Up Network of the trigger of the converter of the low-amplitude *GND–VDDL* signal into a high-amplitude *GND–VDDH* signal. The inverter on *VT15* and *VT16* transistors forms the buffer of the output inverse high-amplitude *GND–VDDH* signal.

Buffers of the output direct and inverse high-amplitude *GND–VDDH* signals are designed to amplify the output signals when operating on high loads and they are used to generate the feedback signals when controlling highly conductive circuits in the Pull-Up Network.

The P-channel *VT5*, *VT7*, *VT11* and *VT14* transistors form two highly conductive circuits, namely, *VT11/VT5* and *VT14/VT7*. Due to this they are fabricated with a large channel width (*W*) and minimum length (*L*). The P-channel *VT12* and *VT13* transistors, in contrast to *VT5*, *VT7*, *VT11* and *VT14*, are fabricated with the minimal channel width *W* and large channel length *L*. Due to this, along with transistors *VT5* and *VT7*, they form circuits with low conductivity.

The conductivity of MOS transistors is inversely proportional to the length L of the channel, and therefore, the higher the channel length L of transistors *VT12* and *VT13* the lower their conductivity. The lower the conductivity of *VT12* and *VT13* transistors the lower the total conductivity of the *VT12*/*VT5* and *VT13*/*VT7* circuits. In the process of switching the circuit of N-channel *VT6* and *VT8* transistors, it is necessary to overcome the opposition of the chains of the Pull-Up Networks of the latch on the *VT12*/*VT5* and *VT13*/*VT7* transistors. Due to this, the lower their conductivity the faster the circuit switching.

Since the gates of *VT12* and *VT13* transistors are connected to a low-voltage *GND* power source, their gate/substrate capacitance does not affect the speed of the circuit. However, the longer the channel length L of *VT12* and *VT13* transistors the lower their conductivity and the shorter the transient switching process when the trigger latch of the signal converter switches from low-amplitude to high-amplitude. Due to this, since in the proposed scheme the low conductivity circuit is not used to generate a high-level signal, its speed is higher than that of the usual scheme. At the same time, in the proposed scheme the dynamic current consumption is less, since the magnitude of the dynamic current consumption in CMOS circuits is proportional to the duration of the transient switching process. The channel length of *VT12* and *VT13* transistors can be arbitrarily large and is chosen solely for reasons of topological expediency.

3. SIMULATION RESULTS AND COMPARISON OF A NEW VOLTAGE LEVEL SHIFTER FOR LOW-POWER APPLICATIONS WITH A TYPICAL ONE

Comparison of two different schemes that perform one function is always a difficult problem. The most common method of comparing digital circuits is to compare the results of simulating schemes with the minimum allowable element size within a single technological process. Such a method is ill-suited for comparing voltage level converters, since reliable operation of a TVLS requires oblique transfer performances of the latch trigger.

Therefore, to compare voltage level converters, it is necessary to use another method—comparing the results of simulating schemes being previously optimized for operation under equal conditions: with the same output load and the same input action. The disadvantage of this method is the difficulty of achieving the necessary but equal level of optimization. This can lead to a comparison of schemes with different levels of optimization, i.e., a comparison of schemes that are in unequal conditions.

In addition, the procedure for such an optimization takes a large amount of time.

Therefore, in order to achieve more reliable results, it is necessary to formulate the conditions based on which optimization and comparison are carried out. In this work, the following agreements are adopted.

—The channel lengths (L) of all transistors are equal to the minimum allowable value of the channel length of the selected technological process except when required by the features of the circuit.

—The channel width ratio W_P/W_N of inverters for a generator of the input direct and inverse low-amplitude *GND–VDDL* signals and a buffer of the direct high-amplitude *GND–VDDH* signal are chosen so that their resistances in an open state are matched. The purpose of such a choice of transistor size is to obtain inverters with the transfer performance that ensures the equal switching times of the inverters when the input voltage signal changes from low to high and from high to low [13].

—The schematic diagrams of transistors of the generator of the input direct and inverse low-amplitude *GND–VDDL* signals, buffer of the output direct high-amplitude *GND–VDDH* signal, and N-channel converter of the low-amplitude *GND–VDDL* signal to a high-amplitude *GND–VDDH* signal coincide (for the schemes to be compared), while the size of the transistors is the same.

—The circuit is optimized by selecting the dimensions—length (L) and width (W)—of P-channel transistors of low-amplitude signal (*GND–VDDL*) converter and high-amplitude signal (*GND–VDDH*) converter, ensuring the maximum speed [13].

—The schemes are compared according to the simulation results under the identical conditions described above.

In addition, we choose the following conditions for calculating transient processes when comparing the dynamic parameters of an NVLS for low-power applications and the TVLS.

(1) Input signal U_{INPUT} with a voltage amplitude of 0 to 3 V is converted into output signal U_{OUTPUT} with an amplitude of 0 to 10 V.

(2) $VDDL = 3$ V, $VDDH = 10$ V.

(3) The duration of the full edges of the input signal U_{INPUT} (positive t_R and negative t_F) is 6 ns.

(4) The output load capacitance is $C_L = 20$ pF.

To evaluate the conversion characteristics, we use the generally accepted parameters:

—t_{PLH} and t_{PHL} are the delay times of the positive and negative edges from a 0.5 voltage amplitude of the input signal U_{INPUT} to a 0.5 voltage amplitude of the output signal;

—t_R and t_F are the duration times of the positive and negative edges of the output signal, measured from the 0.1 to 0.9 amplitude level of the output signal.

The aforementioned parameters are listed in Fig. 3.

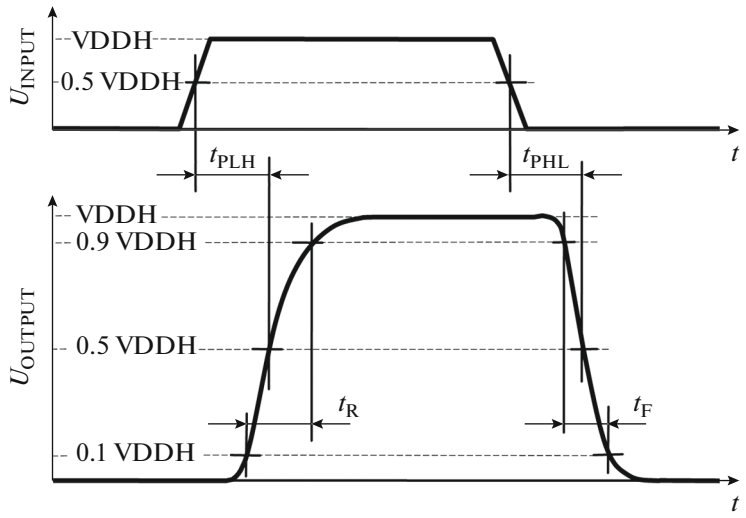

Fig. 3. Representation of monitored parameters.

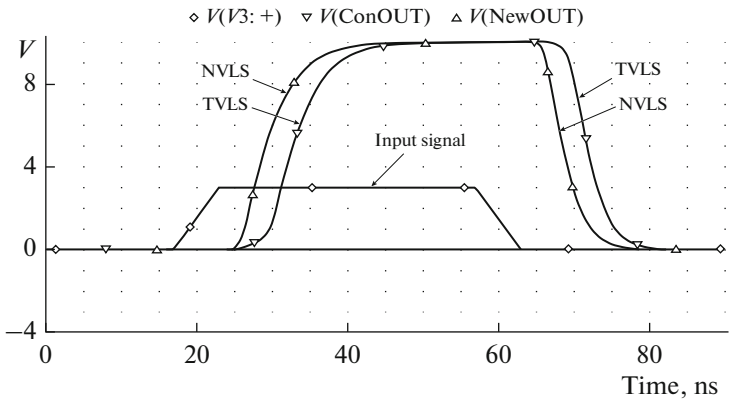

Fig. 4. Simulation results (in graphic form) of operation of NVLS for low-power applications, and TVLS obtained using Probe module from OrCad 9.2 program.

The simulation results were obtained using the PSpice module of the OrCAD 9.2 f. Cadence program. In this case, a mathematical model of the 3rd level and the data of the 3 μm CMOS technological process were used. The graphs in Fig. 4 were plotted using the Probe module. The calculations were carried out in the Transient mode of temporary analysis by dc (DC-analysis). The simulation results demonstrate superiority in the speed of an new voltage level converter for low-power applications over a conventional one.

The numerical values of the time parameters obtained in the simulation of the two compared voltage level shifters and the results of their comparison are shown in Table 1.

CONCLUSIONS

In this article we describe an NVLS for low-power applications and present its electrical circuit diagram. Its operation is described. It is based on the original

Table 1. Parameters of NVLS and TVLS, and results of their comparison in terms of speed

Parameter	TVLS	NVLS	Superiority of NVLS over TVLS by speed, %
t_{PLH}, ns	14.280	9.754	31.695
t_{PHL}, ns	13.003	8.957	31.116
t_R, ns	9.160	9.046	1.245
t_F, ns	6.072	6.033	0.642

method of forming a low conductivity circuit, which is used to reduce the delay time of switching and the dynamic current consumption by minimizing the effect of the counter-effects of the transient process when overcharging the output trigger's capacitance.

In the proposed NVLS, the output inverter of an inverted signal is additionally introduced. The output inverters for direct and inverse signals are needed to preset the highly conductive Pull-up-Network. They can simultaneously perform the amplifying function of the buffers of the output direct and inverse signals.

The simulation results demonstrate that the dynamic performances of the NVLS for low-power applications are superior to those of a TVLS. The time delay of switching is reduced by more than 30%. Compared to traditional schemes, the scheme of a proposed new voltage level converter can operate over a wider range of operating voltages. In addition, in the new converter, dynamic current consumption is reduced by reducing the switching delay time.

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Translated by G. Dedkov