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Specifics of Electromagnetic Radiation Effects on Integrated Circuits

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Abstract—Modern regulations [1] stress the necessity of testing integrated circuits (ICs) in order to determine the real level of their resistance to single voltage pulses induced by electromagnetic radiation (EMR). With expansion of the EMR spectral composition, however, direct energy release can occur due to the absorption of the EMR field energy by the IC chip itself. To assess this possibility, the relationship is found between different mechanisms of the EMR-induced energy release for the typical irradiation geometry.

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1. EVALUATING ENERGY RELEASE IN AN IC CHIP EXPOSED TO THE EMR FIELD

The first experimental investigations and tests of electronic equipment by using microwave generators showed that, as the duration of the acting field's edge gets shorter, protection devices lose their effectiveness; thus, it becomes easier for electromagnetic fields to penetrate through inhomogeneities in frameworks and easier for the induced currents and voltages across integrated circuit (IC) outputs to grow in amplitude.

The typical irradiation geometry for the IC exposed to the electromagnetic radiation (EMR) field is shown in Fig. 1.

A semiconductor chip 250 to 700 μm thick is placed on a metal base. The EMR energy causes the energy release in the semiconductor with the following two basic mechanisms:

—induction of pickups on the IC power-supply pins with the subsequent energy transfer to the chip;

—direct absorption of some of the EMR field energy by the IC chip.

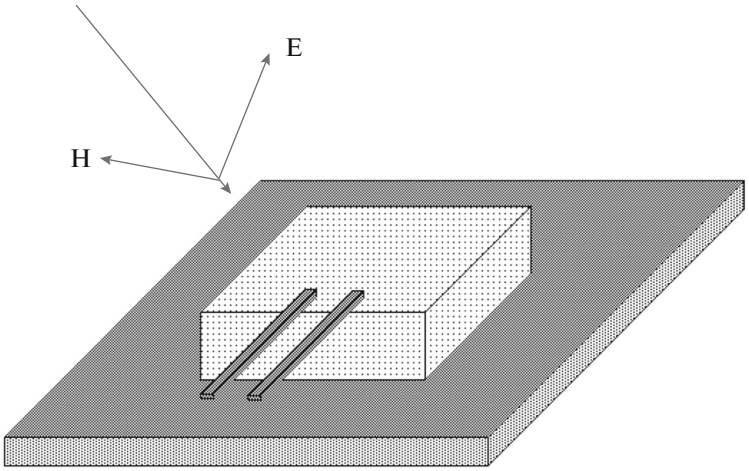

Fig. 1. IC chip in field of plane electromagnetic wave.

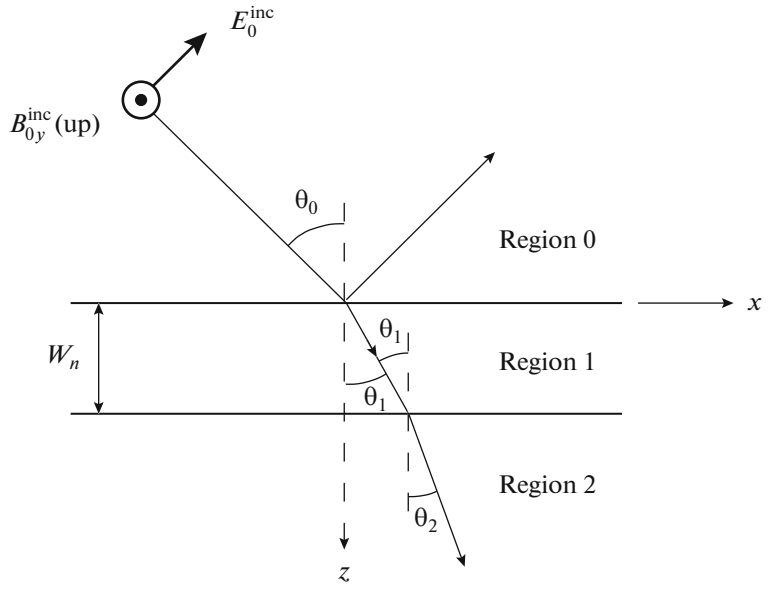

Fig. 2. Incidence of plane electromagnetic wave on interface.

The real irradiation geometry for the IC exposed to the EMR field is complex and has three dimensions. To simplify the problem, we can use the results of the investigation [2] concerning the possibility of modeling the exposure in the semi-infinite geometry, which is shown in Fig. 2.

Region 0 represents air, region 1 is a semiconductor or dielectric substrate, and region 2 represents an aluminum conductor.

Here, W_n is the thickness of the substrate (chip). Figure 2 shows a plane electromagnetic wave moving down from the air to the interface between region 0 and region 1.

In [2], it was shown that, under the effect of an E-type wave (the electric field vector is in the incidence plane), the tangential component of the electromagnetic field in the air at the dielectric surface can be written as

$$B_{0y}(x,0) = B_{0y}(0,0)e^{ikx\sin\theta}[1 + f_{er}]; \quad (1)$$

$$E_{0x}(x,0) = \frac{\omega}{k_0} B_{0y}(0,0)e^{ikx\sin\theta}[1 - f_{er}]\cos\theta_0, \quad (2)$$

while under the effect of an M-type wave (the magnetic field vector is in the incidence plane), it can be written as

$$E_{0y}(x,0) = E_{0y}(0,0)e^{ikx\sin\theta}[1 + f_{mr}]; \quad (3)$$

$$B_{0x}(x,0) = \frac{-k_0}{\omega} E_{0y}(0,0)e^{ikx\sin\theta}[1 - f_{mr}]\cos\theta_0, \quad (4)$$

where f_{er} and f_{mr} are the complex reflection coefficients for E-type and M-type waves, respectively; k_0 is the wavenumber for air (region 0); θ_0 is the wave incidence angle; and ω is the angular frequency.

The squared absolute value $0 \le |f_r|^2 \le 1$ represents the energy of the incident wave reflected from the structure, while the value $1 - |f_r|^2$ represents the energy absorbed by the chip.

Figure 3 shows the behavior of the reflection coefficient f_{er} and the absorbed power P_{abs} for the normal incidence of the E-type wave on the substrate $W_n =$ 250 μm thick, which is made of doped silicon with specific resistance of 100 Ohm cm. It can be seen that, up to the frequencies of about 4×10^{10} Hz, the silicon substrate is electrically thin, and almost all the energy of the wave is reflected. The first absorption peak occurs when the electrical thickness of the substrate becomes one-fourth of the EMR wavelength for silicon.

The analysis shows that, in the frequency range up to 2×10^{10} Hz, the total absorption losses in the silicon substrate do not exceed 0.5 dB. In the case of exposure to the two-exponential EMR pulse with the maximum

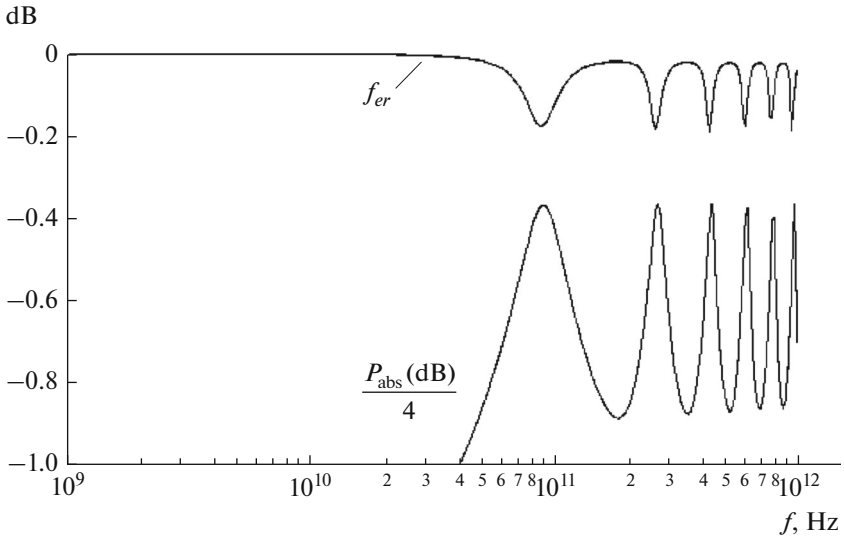

Fig. 3. Behavior of reflection coefficient f_{er} and absorbed power P_{abs} for normal incidence of E-type wave.

electric field intensity of 300 kV/m, maximum magnetic field intensity of 790 A/m, half-height duration of 3×10^{-9} s, and edge of 5×10^{-10} s, the major portion of the pulse energy is within the frequency spectrum bounded by 2×10^{10} Hz. The energy flow carried by this pulse (the Umov–Poynting vector) is $\Pi = E_{max} \times H_{max} \times t_i \cong 0.7$ J/m^2, or about 7×10^{-5} J/cm^2.

For 10% energy losses (which a priori exceed the potential losses throughout the frequency range of the EMR pulse), the maximum energy absorbed per pulse does not exceed $E^s_{abs} \cong 7 \times 10^{-6}$ J/cm^2 (per unit area).

According to [3–5], this energy may be enough to damage the IC. This, however, depends significantly on the distribution of the absorbed energy over the chip. With the thickness of the skin layer in silicon exceeding that of the substrate throughout the frequency range under consideration, the energy release from the EMR field can be very tentatively regarded as uniform. Then, the maximum density of the energy absorbed per pulse will not exceed $E^v_{abs} \cong 28 \times 10^{-4}$ J/cm^3 (per unit volume), and the energy release intensity will not exceed 10^5 W/cm^3. With the specific heat capacity of silicon being 1.6 J/(K cm^3), the overheating caused by the EMR energy absorbed can be neglected. However, before making a final conclusion, the energy release due to the pickups induced on the IC power-supply pins should be evaluated.

2. EVALUATING ENERGY RELEASE IN AN IC CHIP UNDER THE EFFECT OF AN EMR-INDUCED PICKUP

The irradiation geometry shown in Fig. 1 is analyzed assuming that the EMR-induced pickup is due to the short length (2 cm) of the IC pins.

As an input circuit, we selected a CMOS IC with a protection circuit at the input, which is shown in Fig. 4. The protection circuit consists of two diodes (one to the substrate and the other to the power source via the well) and defends the IC against input pulses of any polarity.

Here, $E(t)$ is the electric field intensity, l is the electrical length of the dipole (IC pin), and C_A is the pin capacitance. For a cylindrical pin, we have

$$C_A = \frac{2\pi\varepsilon_0 l}{\ln(2l/a) - 1},$$

where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m and a is the diameter of the pin. For $a = 0.5$ mm, we have $C_A \cong 3.25 \times 10^{-13}$ F.

The energy release was analyzed using the DIODE-2D physical and topological modeling software [6], which allows us to investigate two-dimensional nonstationary processes of carrier transport in semiconductor structures, including those exposed to external single voltage pulses. As an EMR pulse, we use the two-exponential signal (see above) with the edge $t_e = 5 \times 10^{-10}$ s, maximum electric field intensity $E_{max} = 300$ kV/m, and duration $t_p = 3 \times 10^{-9}$ s.

The results of the analysis are shown in Fig. 5. We can clearly see two peaks associated with the leading and trailing edges of the EMR pulse. The first maximum occurs at about 0.2 ns; and the second maximum, at about 2 ns. During exposure to the pickup pulse, the total energy absorbed by the IC input circuits was about 2.3×10^{-4} J with the major portion (2.1×10^{-4} J) being released during exposure to the EMR pulse edge.

Note that the energy flow carried by the given EMR pulse through the IC 1 cm^2 in the area is about 7×10^{-5} J. Therefore, in the given geometry, the

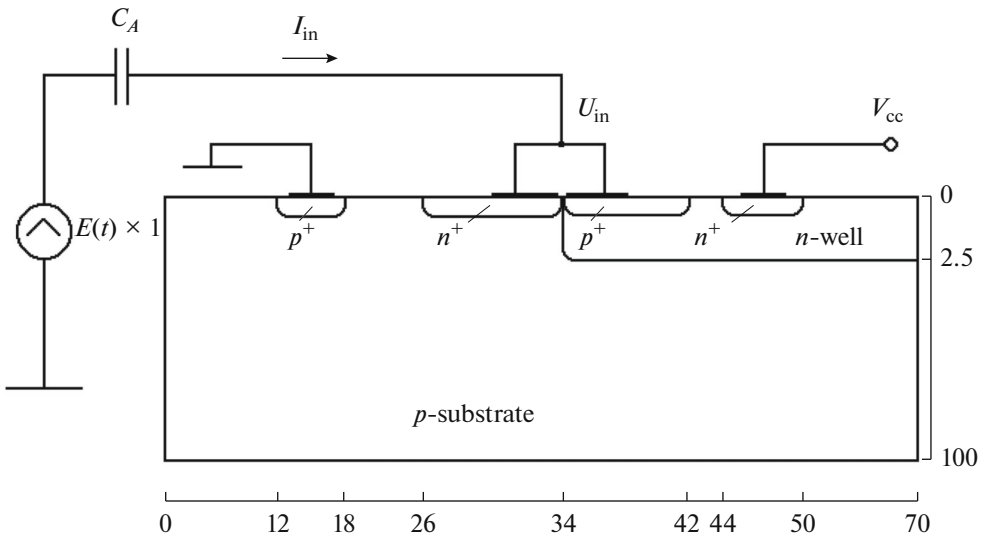

Fig. 4. Physical and topological model of CMOS IC input circuit with protection: $E(t)$ is electric field intensity, l is electrical length of dipole (IC pin), and C_A is pin capacitance.

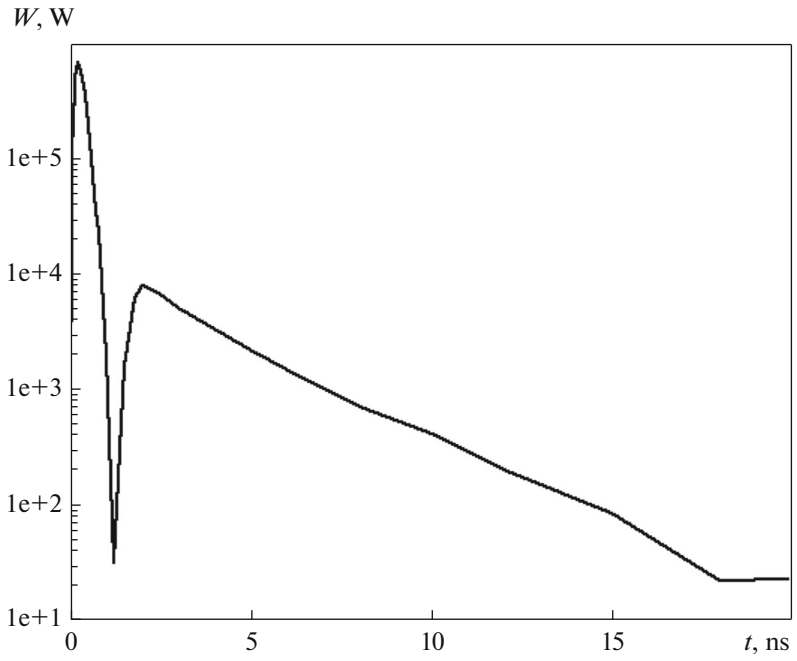

Fig. 5. Time dependence of power consumed by CMOS IC input under effect of EMR-induced pickup.

pickup induced on the 2-cm pin transfers the energy (to the IC chip) that is about thrice as high as that passing through the cross section of the IC 1 cm^2 in area. Thus, the total amount of the energy absorbed by the IC is not increased markedly, which was to be expected because the volume of the object interacting with the EMR (IC plus its pins) nearly triples.

However, the distribution of the absorbed energy (transferred in the form of a pickup through the IC pins) differs considerably from the uniform distribution, which can result in high local densities of energy release. Figure 6 shows the calculated spatial distribution of the energy release over the cross section of the CMOS IC input circuit at the instant 0.2 ns (maximum energy release). It can be seen that the energy release is localized in a narrow near-surface region under the p^+ region in the n-well. The energy release intensity reaches 4×10^{12} W/cm^3, which exceeds that caused by the direct absorption of the EMR energy by more than seven orders. Such a high value is due to the

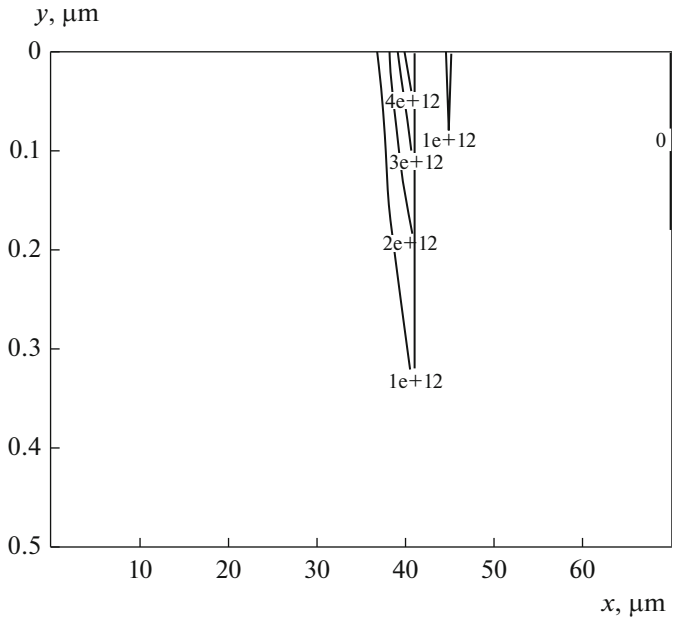

Fig. 6. Spatial energy release distribution (in W/cm^3) over cross section of CMOS IC input circuit at instant 0.2 ns.

fact that almost all the energy is released in a very small volume at the chip surface [7].

Thus, in the case of the pickup induced by EMR on circuit pins, the absorbed energy is localized in relatively small (in terms of volume) regions, which gives rise to local overheated areas that can damage the device. The external pins capture the EMR energy, while the internal metallization and heterogeneous structure of the IC localize the energy in small critical volumes. It is this mechanism that is responsible for the primary and secondary effects that can irreparably damage the IC when exposed to EMR.

In conclusion, this investigation demonstrates that, throughout the time, frequency, and intensity ranges that are characteristic of modern and promising EMR sources, the EMR effects on IC pins can be modeled by electric signals generated using special-purpose single voltage pulses generators.

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