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A Generator of High-Voltage Nanosecond Pulses with a Subnanosecond Rise Time

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Abstract—A generator of high-voltage pulses of nanosecond duration with a subnanosecond rise time is described. The generator contains a nanosecond-pulse shaper based on an assembly of drift step-recovery diodes (DSRDs) connected in series and a sharpening switch based on an assembly of deep-level dynistors (DLDs) connected in series. The results of tests of this generator at a pulse repetition rate of 100 Hz are presented. Voltage pulses with an amplitude of 20 kV, a rise time of 0.3 ns, and a duration of 10 ns are formed across a load with a resistance of 50 Ω.

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In high-power semiconductor generators, the rise time of high-voltage pulses is usually reduced by applying diode sharpeners [1, 2] connected in series to a load. When a sharpened voltage pulse is blocked, a region with a strong electric field initiating an intense impact-ionization wave is created in the diode structures. The produced electron-hole plasma (EHP) ensures fast (fractions of a nanosecond) switching of diodes into a high-conductivity state. In this case, a current pulse with a submicrosecond rise time is applied to the load.

The main disadvantage of diode sharpeners is the short duration of the high-conductivity phase after switching, which is determined by the total amount and density of the EHP generated during travel of an ionization wave. As a result, the amount of switched energy deposited in the load is limited.

This drawback is eliminated in new four-layer semiconductor devices with the impact-ionization switching mechanism—deep-level dynistors (DLDs) [3, 4], in which a high conductivity after switching can be maintained for an arbitrarily long time owing to electrons and holes injected from the emitter layers during flow of the switched current.

Up to now, DLDs have been used in circuits with capacitive energy storages [5–7]. In this case, the switched-current rise rate was determined mainly not by the switching time but the total inductance of the elements of the switching circuit having rather large overall dimensions, which are necessary for ensuring the sufficient electric strength under long-term action of the charging voltage of the storage.

In the mode of sharpening of nanosecond pulses, the high-voltage action time is very short and the switching circuit contains only the sharpener and a load. In this case, the dimensions and inductance of the switching circuit can be significantly reduced, thus allowing the rise rate of switched current pulses to be increased.

Figure 1 shows a circuit diagram of the developed generator of high-voltage nanosecond pulses with a DLD sharpener.

The sharpened nanosecond pulses are generated by a current opening switch in the form of an assembly of drift step-recovery diodes (DSRDs) connected in series [8, 9]. The operating mode of the DSRD assembly is ensured with the use of a magnetic-compression chain including high-voltage C_1 and saturable-core chokes with ferrite cores L_1 and L_2. Fast charging of C_1 is performed with a circuit of pulsed voltage multiplication containing high-voltage capacitors C_0 and C and thyristors T.

In the initial state, a source of a dc voltage of +1.2 kV and ensures charging of capacitors C_0 and C in the polarities shown in Fig. 1 and the application to the DLDs of a small forward voltage, which reduces the value of their self-capacitance. Circuit D–R_2 excludes the charging of C_1 from the source.

When thyristors are turned on under on forced conditions (the amplitude of control-current pulses is ~20 A and the rise time is ~200 ns), capacitors C exchange their charge to a voltage close to the initial one. During its charge exchange (~600 ns), choke L_1 has a high inductance and blocks the high voltage arising across the assembly of capacitors C_0 and C connected in series.

At the moment the charge-exchange process terminates, the core of choke L_1 saturates. The inductance of the choke becomes low and, as a result of switching, it injects a short (~200 ns) forward-current pulse, which is the discharge current of capacitors C_0 and C, into the DSRD circuit. During switching,

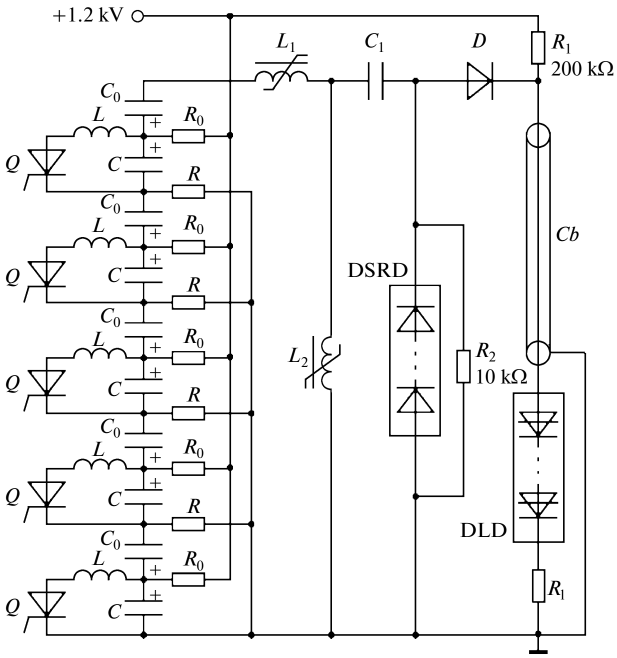

Fig. 1. Circuit diagram of the generator of high-voltage nanosecond pulses with a subnanosecond rise time: (Q) 40TPS12; (DSRDs) the diameter of structures is 20 mm, 20 diodes are connected in series; (DLDs) the diameter of structures is 8 mm, 5 dynistors are connected in series; (L_1, L_2) cores of ferrite no. 97 (Epcos), K41.8 × 26.5 × 12.5 (L_1, three rings, $w = 20$; L_2, two rings, $w = 9$), $L = 1.5$ μH; $C_0 = C = 23$ nF, $C_1 = 2.2$ nF; $R_0 = 50$ kΩ, $R = 1$ kΩ.

capacitor C_1 is charged to a voltage close to the summary charging voltage of C_0 and C.

At the moment the charging current stops, the core of choke L_2 saturates, its inductance abruptly drops, and C_1 rapidly discharges through the L_2–DSRD circuit. As a result, a reverse current rising at a rate of ~8 A/ns flows through the diodes. The reverse current removes the EDP created during the forward-current flow from the DSRD structures and ensures their rapid (several nanoseconds) turning-off at the moment the base regions are cleared of the accumulated current carriers.

During the DSRD turning-off, the current (~550 A) flowing through L_2 is switched to coaxial cable Cb with a characteristic impedance 50 Ω and then to the output circuit consisting of the DLD assembly and a resistive load $R_l = 50$ Ω. As a result, the self-capacitances of the dynistors are rapidly (~2 ns) charged and the voltage across them abruptly increases. When the threshold voltage level (~4 kV) is reached, the DLDs are switched and feed a current pulse to the load. This current rises at a rate determined by the switching capabilities of the DLDs and the inductance of the output circuit.

Figure 2 shows an oscillogram of a voltage pulse across the load obtained at an operating frequency of the generator of 100 Hz. At a pulse amplitude of ~20 kV, the rise time is no longer than 0.3 ns.

In the generator considered, the circuit elements forming the sharpened pulse were placed in a metal case with dimensions of 20 × 10 × 10 cm, and the assembly of DLDs connected in series was placed inside a coaxial connector.

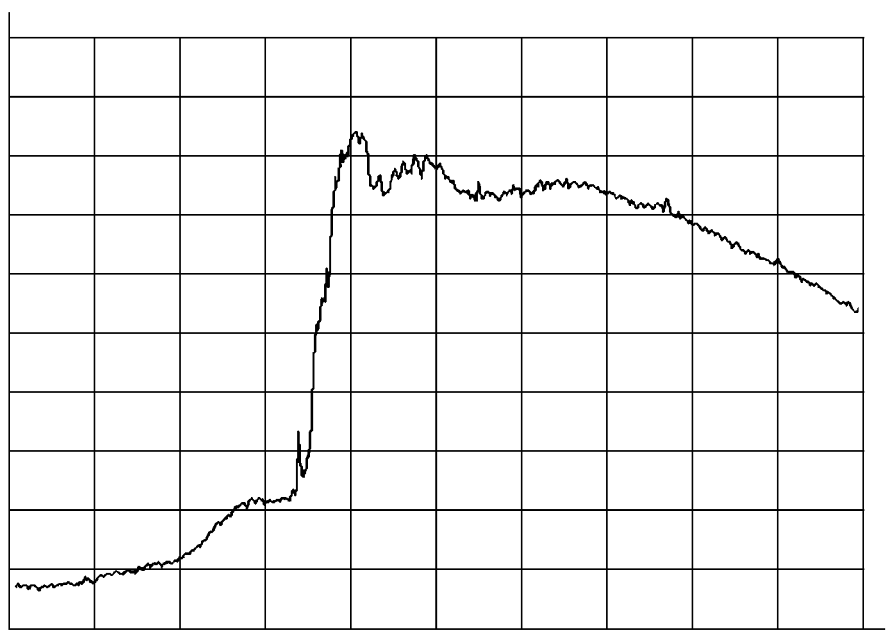

Fig. 2. Oscillogram of a voltage across the load. The vertical and horizontal scales are 3 kV/division and 1 ns/division, respectively.

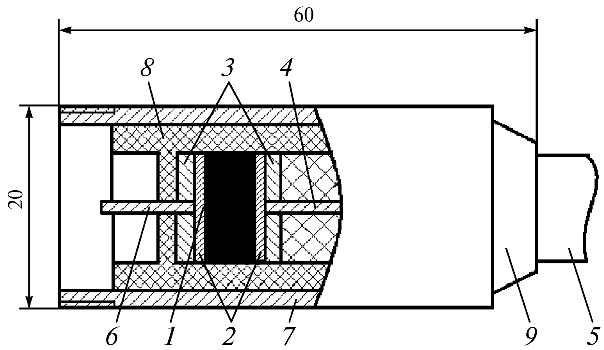

Fig. 3. Coaxial connector with the DLD sharpener.

A drawing of the connector is shown in Fig. 3. Current collectors *2* in the form of thin molybdenum disks are soldered to the end surfaces of assembly *1* consisting of five 8-mm-diameter dynistor structures soldered together. The lateral surface of the assembly is insulated with an organosilicon compound. The assembly is clamped between copper disks *3*. Central conductor *4* of coaxial cable *5* is soldered to one disk, and output contact pin *6* is soldered to the second. The metal case of connector *7* is insulated from the DLDs with Teflon sleeve *8*. Contact unit *9*, standard for high-frequency CP connectors, is screwed into the case of *7* and ensures connection to the cable braid.

Load R_l manufactured in the form of 1-W TBO resistors connected in parallel is the internal current conductor of another coaxial connector opposite with respect to the connector in Fig. 3.

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