ISSN 0020-4412, Instruments and Experimental Techniques, 2010, Vol. 53, No. 2, pp. 213–223. © Pleiades Publishing, Ltd., 2010.
Original Russian Text © E.V. Atkin, A.G. Voronin, Yu.A. Volkov, A.D. Klyuev, A.Yu. Pakhomov, A.S. Silaev, 2010, published in Pribory i Tekhnika Eksperimenta, 2010, No. 2, pp. 62–73.

APPLICATION OF COMPUTERS IN EXPERIMENTS

An Integrated Circuit for Reading out Signals of Silicon Detectors

E. V. Atkin[a], A. G. Voronin[b], Yu. A. Volkov[a], A. D. Klyuev[a], A. Yu. Pakhomov[b], and A. S. Silaev[a]

[a] *National Research Nuclear University (Moscow Engineering Physical Institute), Kashirskoe sh. 31, Moscow, 115409 Russia*
[b] *Skobel'tsin Research Institute of Nuclear Physics, Moscow State University, Moscow, 119992 Russia*

Received February 10, 2009; in final form, June 18, 2009

Abstract—An integrated circuit (IC) for recording signals and studying characteristics of silicon detectors is designed and experimentally checked. The basic purpose of the IC is to use it in test setups with sources of ionizing radiation and on accelerators for studying silicon detectors of a new geometry (layout). The IC allows evaluation of the operation of the "silicon detector–readout electronics" system for relativistic particles and nuclei with a charge from $Z = 1$ to $Z > 50$. The results of designing the IC and its experimental characteristics are given.

DOI: 10.1134/S0020441210020119

INTRODUCTION

At present, an important scope of silicon detectors is basically track systems, systems for measuring charges of particles transmitted through the detector, and calorimetric systems [1–3]. The basic parameters determining the quality of each system is the signal-to-noise ratio and dynamic range of input signals measured by the number of minimally ionized particles (MIPs), which can be recorded by the system. On the one hand, track systems do not require a large dynamic signal range (as a rule, several MIPs will suffice for recording), but, on the other hand, it is necessary to have a high signal-to-noise ratio (>10). For charge measuring systems, the dynamic range increases up to ≥2000 MIPs, and the noise requirements can be reduced to a signal-to-noise ratio of 7 : 10. In calorimetry, the requirements for the dynamic range can come to recording tens of thousands of MIPs, and the signal-to-noise ratio can be >5.

The designed integrated circuit (IC), which reads signals of semiconductor detectors, is intended for converting the charge generated in a silicon detector, while a charged particle flies through it, into the voltage proportional to the charge and for the further analog signal processing, i.e., for converting the shape, amplitude, and duration of these signals into signals suitable for digitization.

Because the IC is intended for studying characteristics of silicon detectors of various types, the technical requirements for it result from analyzing the characteristics of the most typical detectors mainly used in the particle charge measuring systems and calorimetry.

The basic technical requirements are as follows. The dynamic range of the MIP input signals is ≥30000 for detectors with a 300-μm thickness; the maximal capacitance value of the connected detector is ≥100 pF; the power consumption is ≤3.5 mW/channel; the time of reaching the signal peak at the *RC*–*CR*-filter output is ≤3 μs; the clock frequency of the digital control circuits is ≥10 MHz; the signal-to-noise ratio at a 100-pF capacitance value and 500-μm thickness of the detector is no worse than 2.5; the minimal signal is 1 MIP; the slope of the noise characteristic is 8.1 electron/pF; and the maximal output voltage is 2.6 V.

To measure characteristics of track silicon detectors, it is possible to use ICs from the IDEAS Co., e.g., VA1 [4] or a 16-channel IC of the charge-sensitive amplifier (CSA) [5], designed for reading out signals of silicon detectors and having an RMS (root mean square) noise not exceeding 2000 electrons. For this purpose, as the first stage of the readout system, a CSA of the 16-channel IC is used, and, then, its outputs are connected to the inputs of the integrated IC of the silicon detectors (ИМСКД), thus ensuring a signal-to-noise ratio >10.

The closest analog of the designed IC is the VA32HDR14 IC [6] (IDEAS). Two modifications of the IC, namely, ИМСКД1 and ИМСКД2, were designed. Each has its own special features for ensuring qualitative measurements of characteristics of the "silicon detector–readout electronics" system.

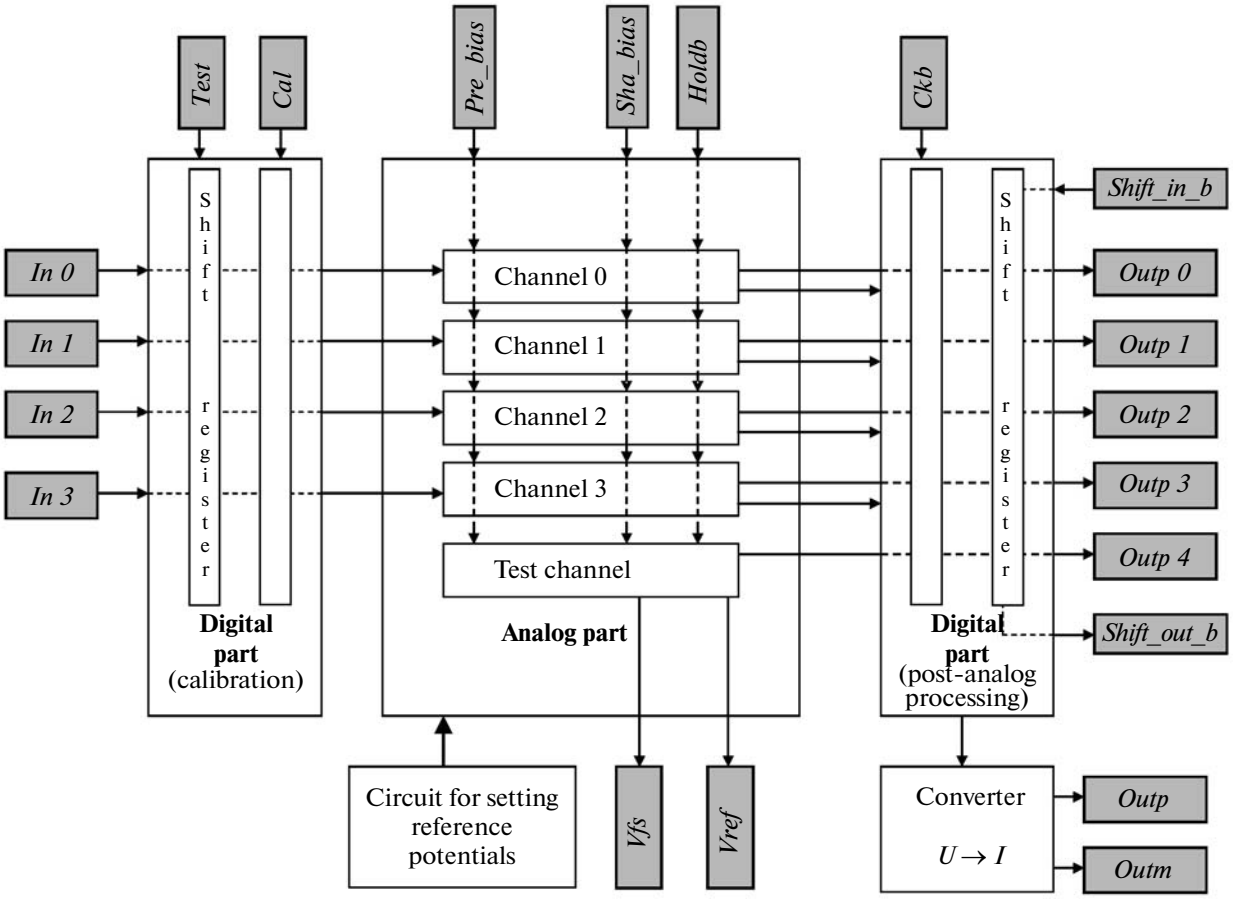

Fig. 1. Block diagram of the four-channel IC.

BLOCK DIAGRAM

The block diagram of the IC is shown in Fig. 1. It consists of the analog and digital parts.

The basic part of the IC contains four identical analog channels intended for reading out and preprocessing signals picked off the silicon detectors. Each analog channel contains a CSA with an automatically changeable gain (Fig. 2), shaper amplifier (active *CR–RC* filter), and track-and-hold unit (THU). The gain variation allows one to expand the dynamic range of the input signals.

The digital part of the IC services two basic functions: (i) control of switching signals of the THU outputs of the channels, which is fulfilled by the interchannel multiplexer and shift register, and (ii) control of the channel calibration.

The analog multiplexer controlled by the shift register is used at the CSA input of the basic channels for performing calibrations. The test signal is applied through the analog multiplexer, which arrives through the *Cal* (calibration) output at one of the selected basic channels.

The IC consecutively reads out analog information, and, for this purpose, the THU outputs are connected to the inputs of the output analog multiplexer, controlled, as in the case of the calibration system, by the shift register. The output stage is designed as a voltage-to-current converter (Fig. 3).

The IC also uses additional analog circuits. They include the reference potential setting circuit and additional channels having structures similar to those of the basic channels, to the outer contact pads of which all intermediate, most typical points, are connected, thus allowing one to study in more detail the behavior of the "silicon detector–readout electronics" system. The ИМСКД1 IC has a circuit for measuring leakage currents of the silicon detectors. An additional output (buffer) amplifier–voltage-to-current converter is brought into the ИМСКД2 IC.

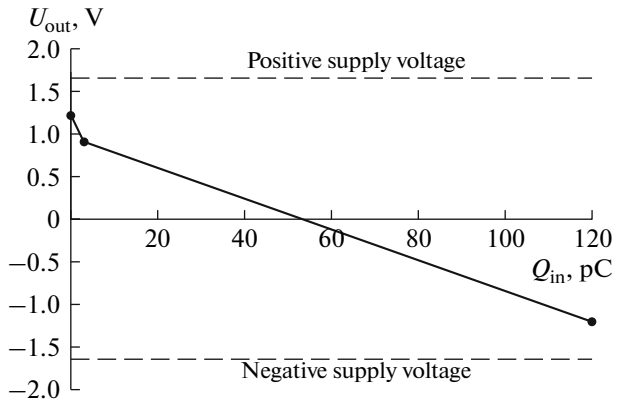

Fig. 2. Planned transfer characteristic of the CSA.

DESIGN TOOLS AND BASIC SIMULATION RESULTS

When designing the integrated IC, the Cadence computer-aided design facilities (IC5.1.41, Neocell 3.4, IUS5.7, and SOC 4.2 software products) were used. Verification tools (Calibre) of the Mentor Graphics company and technological libraries (Design Kits) of the Belgian AMIS company accessible via the European Europractice organization (www.europractice.com) were used.

Figure 4 shows some simulation results, namely, the typical waveform of signals at the output of the shaper amplifier and the corresponding transfer characteristic in an input signal range up to 120 pC. The simulation has shown that, when the gain automatically changes, the break (inflection) of the transfer characteristic occurs at a 3-pC level, corresponding to the selected value. In this case (from the simulation results), the peak value of the amplitude of the signal, corresponding to 1 MIP, is~500 μV at the shaper amplifier output for the detector with a 300-μm thickness, and the RMS noise voltage is ~220 μV at a 100-pF capacitance value of the detector. Thus, in accordance with the simulation results for the minimal signal, the signal-to-noise ratio for the detector with a 300-μm thickness should be ~2.5. In accordance with the technical requirements, this ratio should be true for detectors with a 500-μm thickness, for which 1 MIP is ~1 mV. The measurements results of the IC, in particular, to compliance with the simulation are given below.

SCHEMATICS IC

The CSA inputs are connected to the silicon detector to draw the alternating current (through a blocking capacitor). The first stage of the CSA is constructed in a cascode circuit with a parallel power supply (so-called parallel cascode). In this case, as an input transistor, a MOS transistor (the enhancement mode *p*-channel transistor) is selected. The selection of this type of conductivity for the input transistor is caused by two factors: (i) need for minimizing the $1/f$ noise and (ii) positive polarity of the input signals. To increase steepness and minimize noise, the input transistor has a large equivalent channel width W (8000 μm) and small channel length L (0.5 μm). To discharge the feedback capacitor in the CSA and to set the input transistor mode, the IC uses a high-ohmic (2 MΩ) resistor, which determines the fall time of the output pulse of the IC. The transconductance of the input transistor is 1.6 mA/V (1.6 mS) in nominal conditions, and C_{in} (gate–source capacitance) is 10 pF.

To ensure the complete dynamic range for the input charge, it was divided (from noises to saturation) into two subranges. Figure 2 shows the planned CSA transfer characteristic (dependence of its output voltage on the input charge of the detector). The gain varies, when the input charge is ~3 pC. On the one hand, this allows one to ensure a higher slope of the transfer characteristic in the small-amplitude region and, thus,

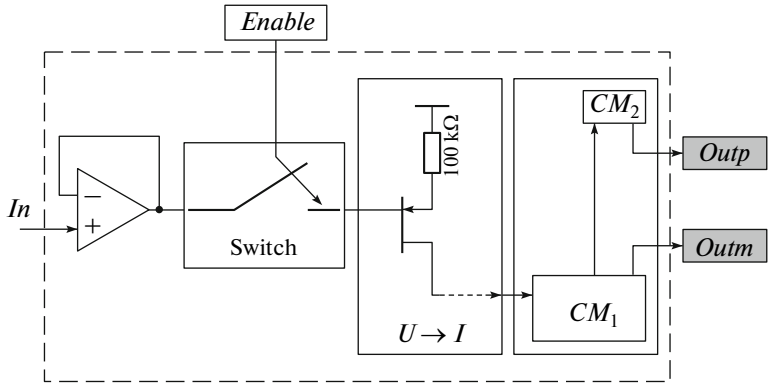

Fig. 3. Block diagram of the output stage: (CM_1, CM_2) current mirrors.

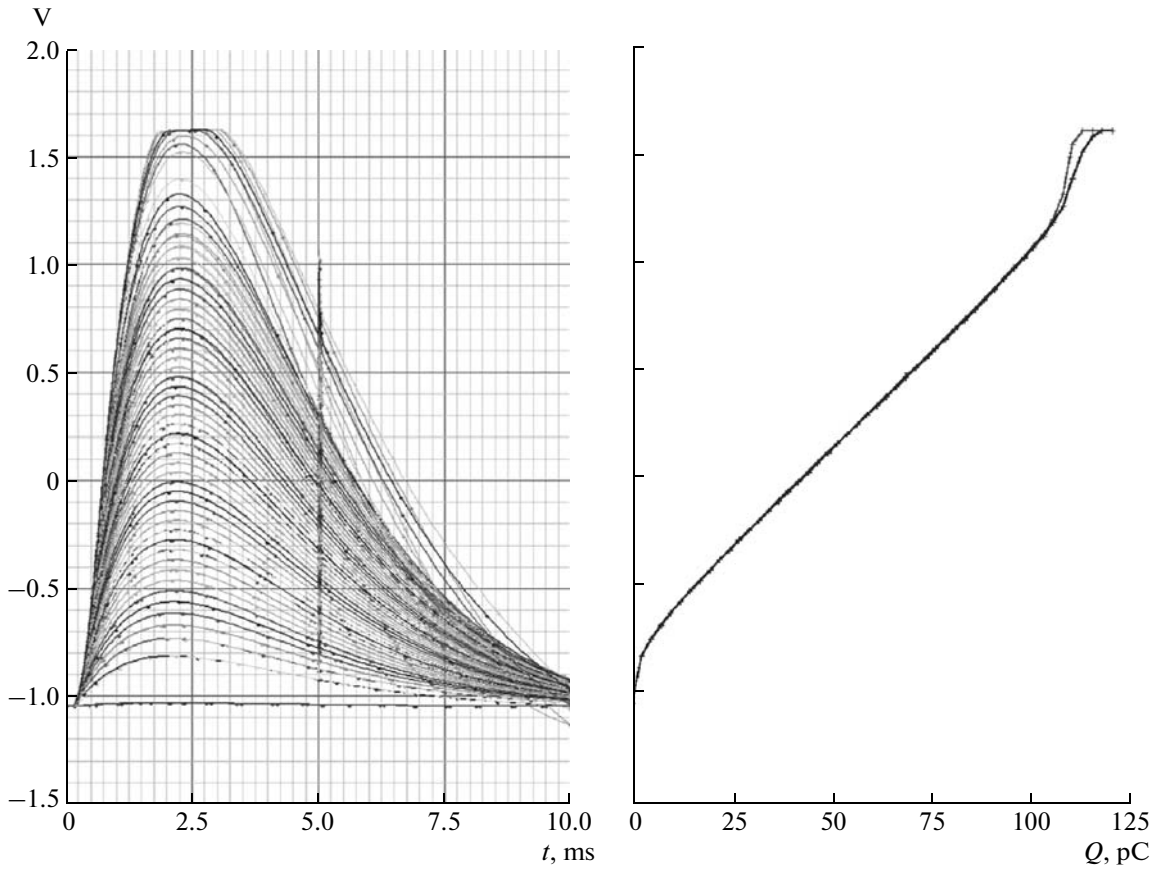

Fig. 4. Response of the shaper amplifier and its transfer characteristic (simulation).

achieve a better signal-to-noise ratio, and, on the other hand, to ensure a smaller slope in the large-signal region and, thus, achieve a dynamic range of >100 pC.

The subranges are automatically changed in the designed circuit. For this purpose, an additional switch circuit is brought at the CSA output. In the initial state (without a signal and in the small-amplitude region), the switch circuit is in the off state and does not influence the CSA feedback. The gain is determined by a relatively small capacitance value (~6.6 pF) of the feedback. This capacitance determines the CSA transmission gain by the formula

$$K_Q = U_{\text{out}}/Q_{\text{in}} = 1/C_{\text{fb}} = 0.15 \text{ V/pC}.$$

For higher amplitudes (starting from ~3 pC), the switch circuit dynamically opens. In this case, an additional capacitor is added into the signal reverse transmission channel through an auxiliary amplifier (virtually operating in the *B* class mode). The gain of the amplifier and capacitance value of the additional capacitor determines the CSA feedback circuit in the large-amplitude region. Thus, the CSA transmission gain decreases as compared to the gain in the small-amplitude region. In this case, the equivalent capacitance value of the CSA feedback is ~67 pF.

The CSA output (see Fig. 2) is connected to the input of the shaper amplifier, which is the active *CR*–*RC* filter circuit. The shaping time is selected ~2.2 μs. The basic purpose of the filter is to shorten the signal duration to unities of microseconds and, thus, increase the channel loading capability up to 100 kHz. The second function of the shaper amplifier is to improve the signal-to-noise ratio in the channel.

The schematic diagram of the shaper amplifier is based on a parallel cascode circuit similar to the CSA circuit but with an input *n*-MOS transistor. In this case, the circuit mode is optimized for operation with negative-polarity signals at the input and positive-polarity signals at the output of the shaper amplifier (with amplitudes of up to 2 V).

The next stage in the IC channel is the THU intended for fixing the amplitude value at the output of the shaper amplifier in response to the *Holdb* external control logic signal (holding). Its circuit is based on a switch on complementary transistors, a 1-pF capacitor, and a buffer single-stage operational amplifier with 100% feedback. The amplitude of the signal at the

CSA and shaper amplifier output is proportional to energy losses of recorded particles. Therefore, the *Holdb* external control signal should be applied at the moment, when the signal at the output of the shaper amplifier reached its maximum. This occurs ~2.2 μs after the event recording. In this case, the THU changes to the holding mode of a fixed amplitude, and the amplitude itself can be read through the switch and voltage-to-current converter.

The circuit of the digital part of the IC is synthesized as a functional analog of a Va32HDR14.2 IC from IDEAS [4]. The corresponding time diagram of the readout cycle is shown in Fig. 5. This diagram reflects the main readout mode. The test (calibration) operation mode of the IC exists. In this case, the test pulse arrives at the CSA inputs through the contact *Cal* and calibration system switch, simulating the signal of the detector. The state of the calibration switch is controlled by the same signals as of the state of the output switch and by a *Test_on* signal (test is on), which must have a high level.

The output stage of the IC is the voltage-to-current converter module, which does not require input reference potential V_{ref}, as it is realized in the Va32HDR14.2 IC. A single-phase signal from the multiplexer output arrives at the input of the converter.

The first clock pulse arriving at the output shift register simultaneously activates the trigger producing the *Enable* signal (read enabling). The *Enable* signal is reset by the pulse of the trigger, which generates a *Shift_out* signal intended for the consecutive reading of several ICs.

Upon application of the enabling *Enable* signal, the voltage from the multiplexer output through the operational amplifier operating as a follower and the switch arrives at the *Mux_out* output of the IC (output of the multiplexer, only for the ИМСКД2) and, in parallel, through the voltage-to-differential-current converter at the current outputs of the IC *Outm* (negative-polarity output) and *Outp* (positive-polarity output). The load resistor can be connected to the *Outm* and *Outp* outputs with respect to both the ground and the power supply buses (±1.65 V), respectively.

RESULTS OF THE LAYOUT DESIGN

The IC layout area is 4 × 2 mm^2. The topology is designed taking into account the AMIS Co. design rules for the CMOS process with a 0.35-μm geometry. This process is used for interconnections and creating resistors and capacitors (five metal layers and two polysilicon layers).

Each analog channel of the ИМСКД IC consisting of three basic modules (CSA, shaper amplifier, and THU) is designed as an elongated rectangle (strip) with an 80-μm height, including power supply buses

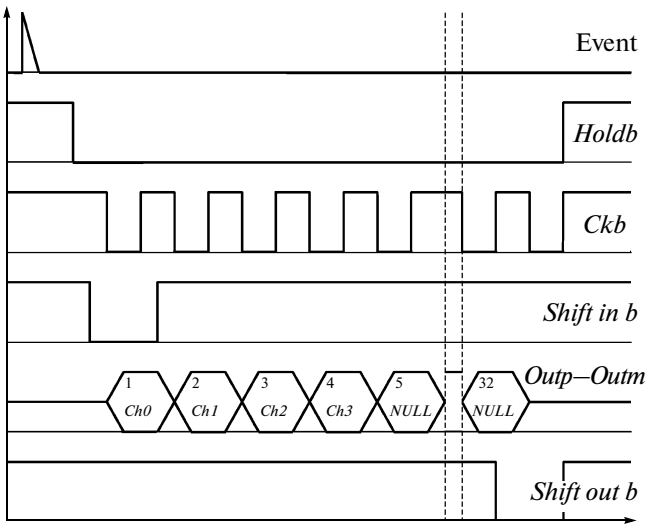

Fig. 5. Diagrams of the reading cycle of the digital part.

(up to 10 μm each). The channel area is 80 × 3000 μm^2. The larger part of the channel is occupied by the CSA (80 × 2000 μm^2). The *p*-MOS transistor, feedback resistor, capacitor occupying the basic CSA area (60 × 1000 μm^2), and remaining components of the CSA circuit are placed at the CSA input. The shaper amplifier with a total 80 × 414.5-μm^2 area and THU with an 80 × 474.5 μm^2 size are placed further.

LABORATORY TESTS

For performing laboratory tests, the integrated ICs were placed in CLCC84 ceramic cases. Voltage diagrams of the analog stages in the small-signal mode at the IC pads are shown in Figs. 6 and 7.

The measured amplitude (transfer) characteristics of the IC are shown in Fig. 8 in different scales. The spread of the amplitude characteristics does not exceed 10% for ten measured samples.

The break (inflection) point of the amplitude characteristic is located in the vicinity of a ~600-MIP (3 pC) input signal. The amplitude characteristic of the break zone is shown in Fig. 9. The MIP value is calculated for the detector with a 300-μm thickness, and it is 500 μV at the output, corresponding to the simulation data.

The transfer characteristic of the IC as a function of the supply voltage value was studied. The standard supply voltage value of the IC (of both the analog and digital parts) is ±1.65 V (power supply is bipolar). The measurements were performed at an increased and decreased (by ±10%) supply voltage (see Fig. 10). The investigation has shown a high sensitivity of the IC to the supply voltage value. The absolute spread of the output voltage reaches 0.5 V, which is 20% at a 2.5-V maximal output signal amplitude and correspondingly

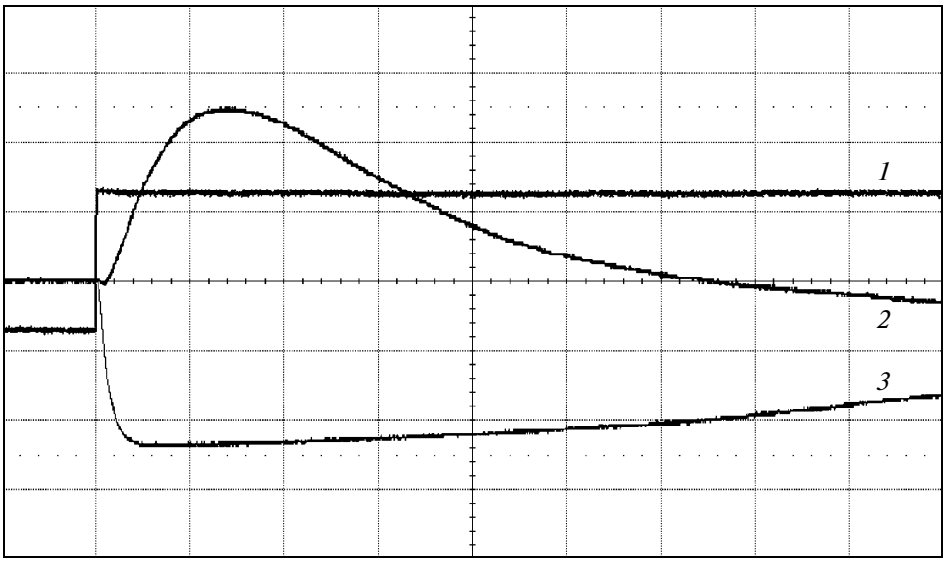

Fig. 6. Typical diagrams of the analog stages: (*1*) test input signal, (*2*) output of the shaper amplifier (test channel), and (*3*) CSA output. The scale in the vertical direction is (*1*) 500 and (*2*, *3*) 200 mV/division, and in the horizontal direction is 2 μs/division.

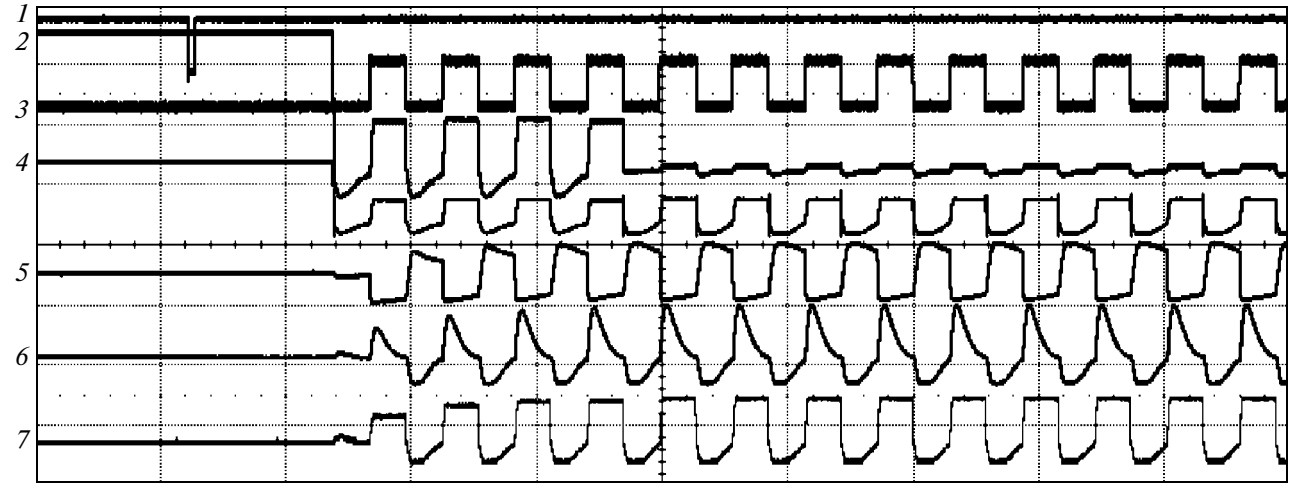

Fig. 7. Typical diagrams of the analog stages: (*1*) *RESET* signal, (*2*) output of the IC with the de-energized test channel, (*3*) test pulses, (*4*) THU output of the test channel, (*5*) CSA output of the test channel, (*6*) output of the shaper amplifier of the test channel, and (*7*) output of the IC with the energized test channel.

increases to 200%, when the output signal decreases to 0.25 V. It follows from Fig. 10 that the position of the break point changes, but the slope of the characteristic does not change, i.e., the constant level shift takes place in the region with a decreased gain (second subrange). It is required to have voltage stabilization no worse than 1% to eliminate the dependence of the transfer characteristic of the IC on the supply voltage.

The dependence of the signal value at the IC output on the equivalent detector capacitance was measured in the range from 0 to 130 pF. When the detector capacitance value is <68 pF, no substantial influence on the output signal amplitude is observed. A further increase in the detector capacitance value leads to reducing the gain of the IC. For a 130-pF capacitance of the detector, the gain value decreases by 5% as compared to the gain of a 68-pF capacitance.

The amplitude of the maximal output voltage of the IC at the working portion of the characteristic varies from 2.5 to 2.6 V, corresponding to ~38000 MIPs for a 300-μm thick detector. For signals exceeding 28000 MIPs, one can note an increase in the nonlinearity of the gain of the IC (Fig. 11) that agrees with the simulation.

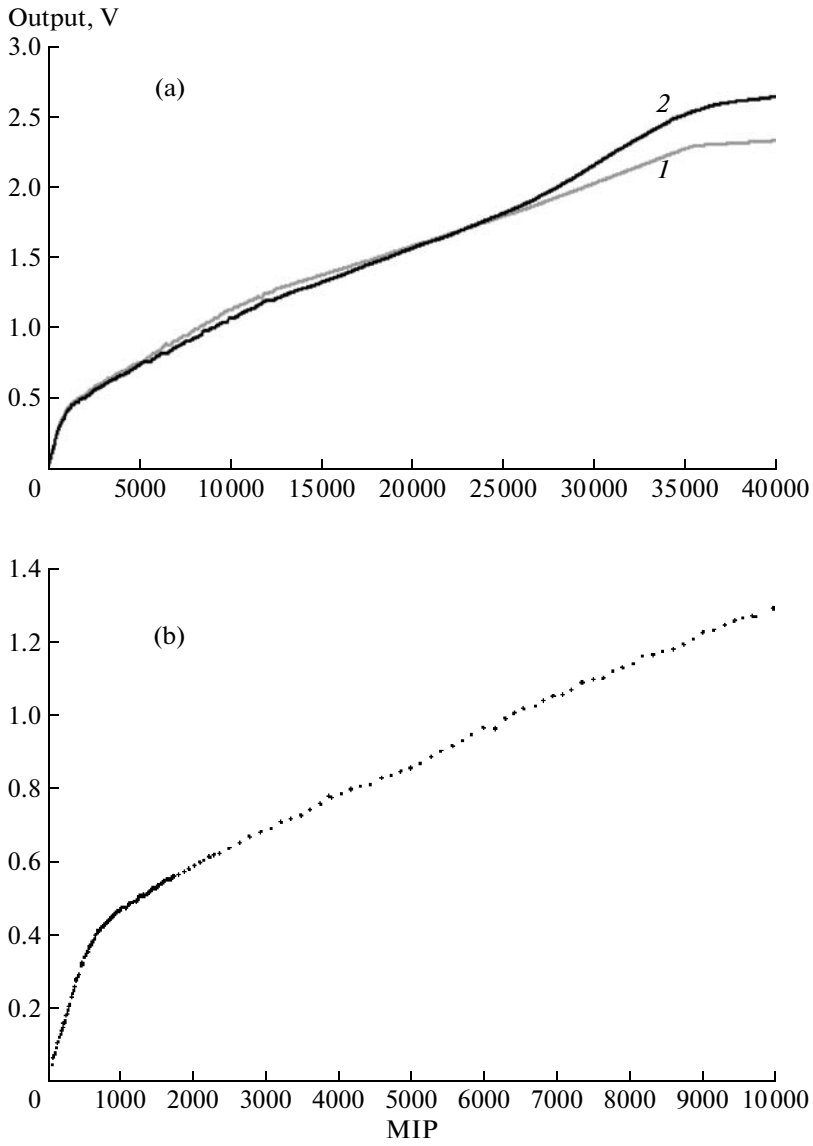

Fig. 8. (a) Complete amplitude characteristic of the IC: (*1*) channel of the shaper amplifier, and (*2*) CSA channel, (b) portion of the amplitude characteristic of the IC up to 10000 MIPs (CSA channel). The calibration capacitance value is 6.8 pF, and the equivalent capacitance value of the detector is equal to zero.

In measuring noise characteristics of the ICs, a "1-MIP signal-to-noise" ratio close to 2.5 is obtained for detectors with a 500-μm thickness that satisfies the technical specification of the IC. However, the value of 2.5 obtained by simulation was not reached for the detector with a 300-μm thickness, indicating either incorrect noise component models or effects in the IC substrate. The measurements were performed by several methods. The obtained noise values measured by different methods differed by ≤10%. The measurements were performed at the output of each stage to determine noisy stages. The peripherals, in particular, the fourth-order shaper amplifier, were used for studying noise characteristics of the input stage (CSA). The analysis of results has shown that the input stage basically contributes to noise, and the filtering properties of the shaper amplifier are not sufficient for reaching a 220-μV calculated (simulated) noise (RMS deviation).

The tests have shown that in designing units based on the developed IC, it is required to thoroughly study the layout of conductors connected to the IC. Otherwise, it is possible to observe a weak excitation of separate stages at a 0.5- to 5.0-mV level. Figure 12 shows one of the typical versions, when there is pick-up at the IC input, the source of which is the THU operation at a certain bias current and 10-pF stray capacitances of the printed circuit board (THU oscillation is not shown in the oscillogram, it is actually 5 mV).

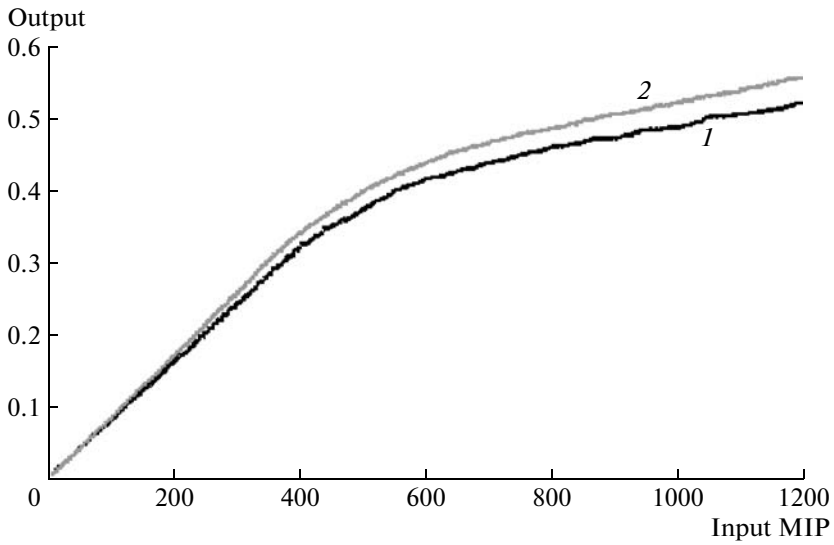

Fig. 9. Amplitude characteristic of the IC in the break point zone. The calibration capacitance value is 1 pF, and the equivalent detector capacitance value is zero: (*1*) shaper-amplifier channel and (*2*) CSA channel.

SPECIAL FEATURES OF THE ИМСКД1 AND ИМСКД2 MODIFICATIONS

The ИМСКД1 has no external controls of its characteristics and contains two additional circuits (a circuit for measuring the leak current of the detector and an analog channel circuit, whose structure is similar to that of the basic channel).

The ИМСКД2 is intended for the detailed study of characteristics of a separate multichannel detector. Circuits of controls of individual stages and intermedi-

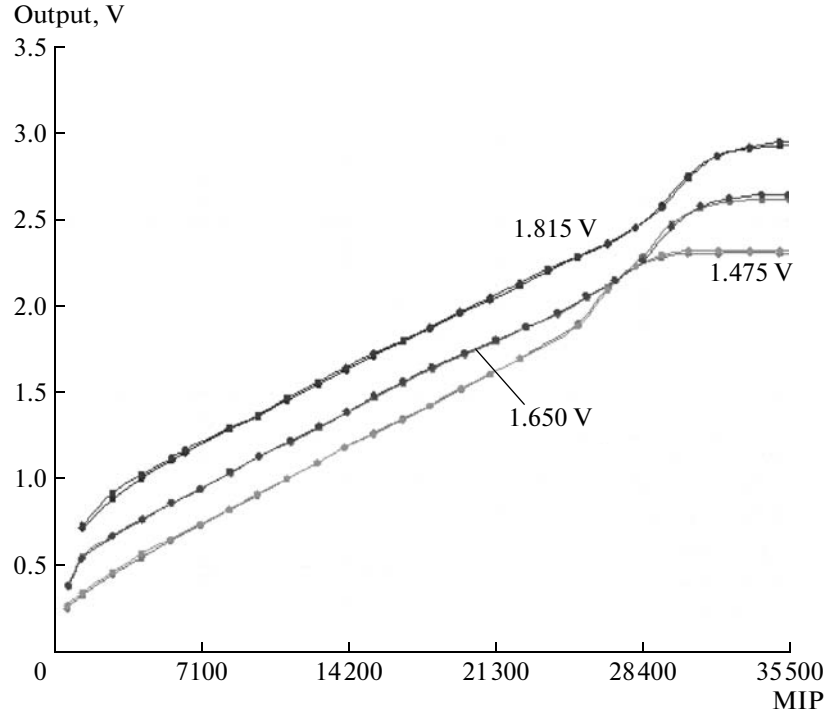

Fig. 10. Amplitude characteristics of the IC (as a function of the amplitude of the test pulse) for different supply voltages (1st and 2nd channels are shown).

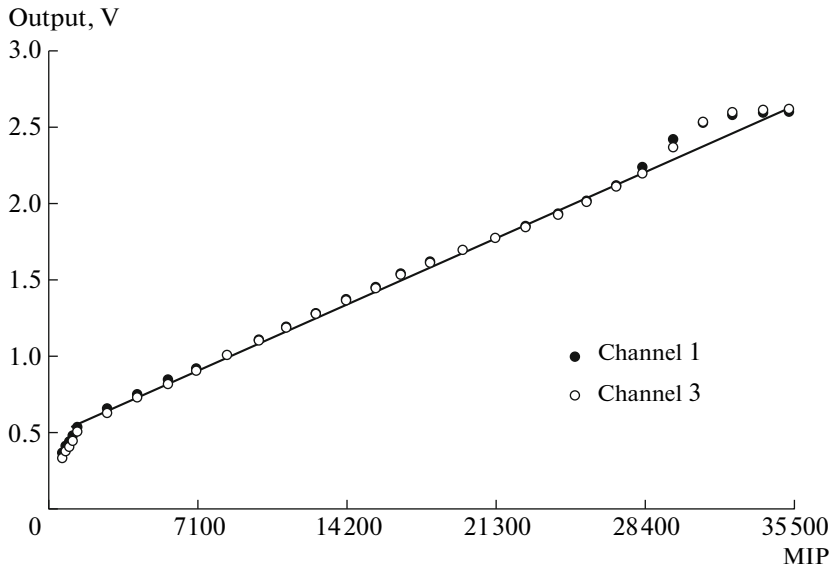

Fig. 11. Amplitude characteristics of the IC. The calibration capacitance value is 51 pF.

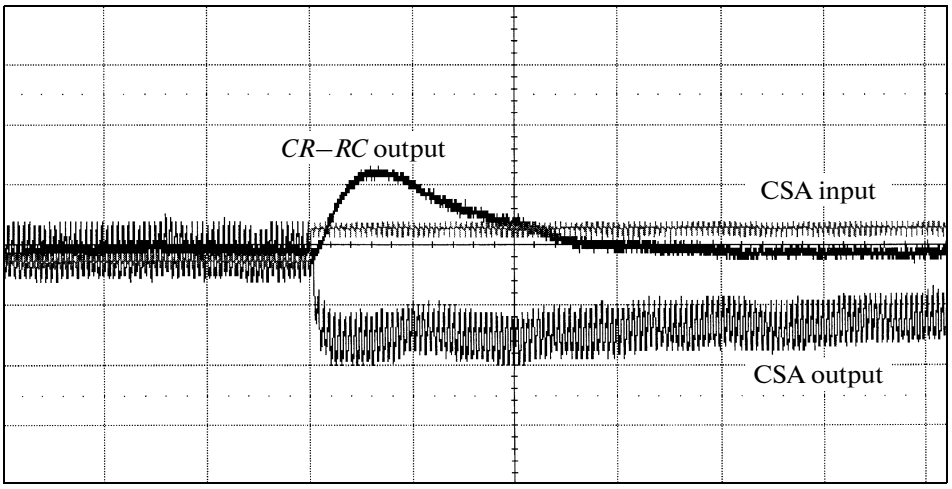

Fig. 12. Noise oscillograms in the analog stages of the ICs. The scale in the vertical direction is (*CR–RC*) 5 and (CSA) 10 mV/division, and in the horizontal direction is 5 μs/division.

ate outputs of the stages are connected to contacts of the ICs in the ИМСКД2. There are three additional circuits (two analog-channel circuits and a separate output stage similar to the basic one).

CSA (input stage). The ИМСКД1 contains a 2-MΩ high-ohmic resistor, which determines the time constant of the output signal fall, for discharging the feedback capacitor in the CSA and setting the operation mode of the input transistor the IC.

The ИМСКД2 uses a long-channel *n*-MOS transistor with dimensions of 100 × 1 μm and external gate–source control to decrease parallel noise of the feedback circuit by 30% and to optimize the discharge time. The maximal output signal substantially changes its own shape due to the nonlinearity of the transistor characteristics, and, in this case, the signal amplitude remains unchanged. Examples of oscillograms with an *n*-channel MOS transistor are given in Figs. 6, 13a, and 13b, where diagrams of the voltage simulating the input action, response of the CSA and shaper amplifier in the small- (up to 3 pC) and large-signal modes, respectively, are shown.

Two external bias voltages (*pre_bias* and *pre_bias2*) are applied to the ИМСКД2 IC for changing the position of the inflection (break) point of the transfer characteristic and for optimizing the CSA circuit for the

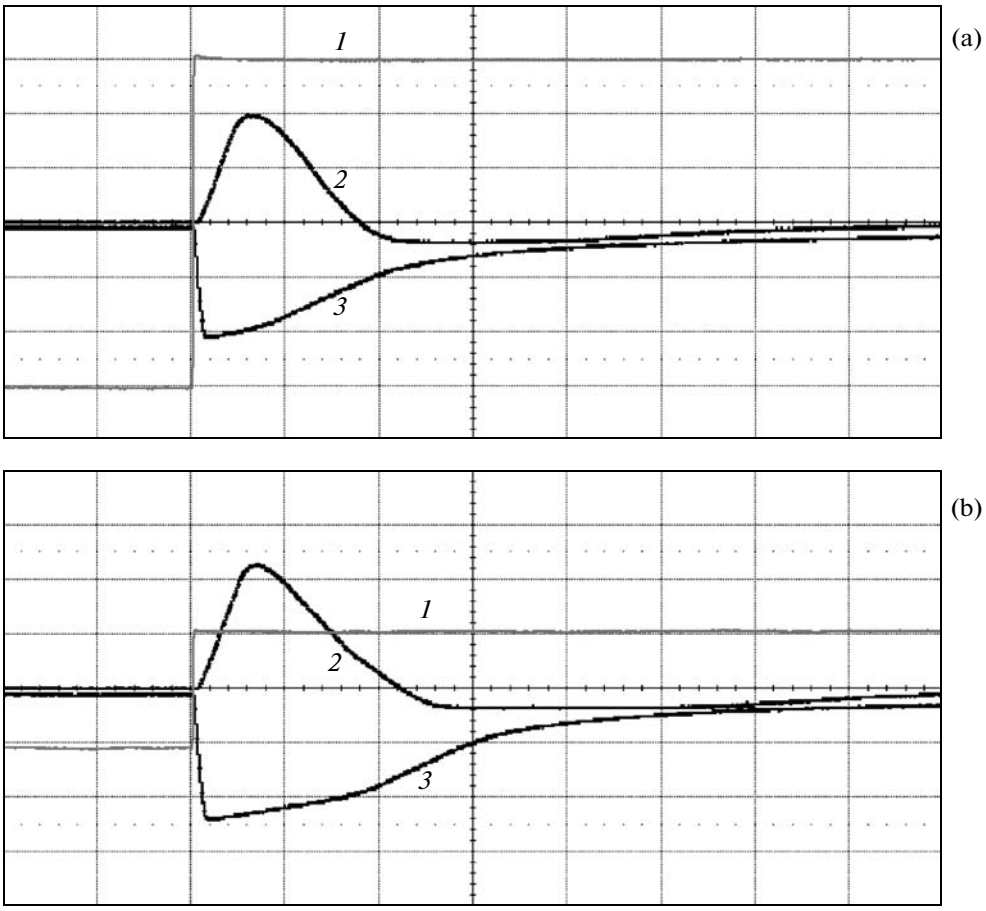

Fig. 13. Input pulse (*1*) and typical response of the (*3*) CSA and (*2*) shaper amplifier in the large-signal mode. The scale (a) in the vertical direction is (*1*) 100 mV/division and (*2*, *3*) 1 V/division, and in the horizontal direction is 5 μs/division; (b) in the vertical direction is (*1*) 500 mV/division and (*2*, *3*) 1 V/division, and in the horizontal direction is 5 μs/division.

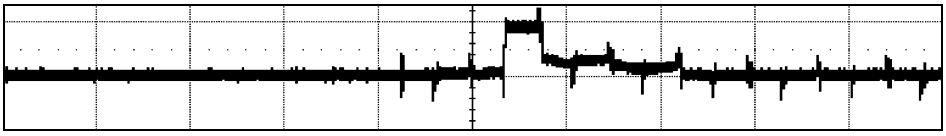

Fig. 14. Typical response of the ИМСКД2. The scale in the vertical direction is 100 mV/division and in the horizontal direction is 100 μs/division.

minimum power consumption. The CSA modification for the ИМСКД2 in accordance with simulation data allowed us to decrease the CSA power consumption to 1 mW/channel.

Output stage. In the ИМСКД1, the conversion unit (Fig. 3) consists of series basic modules, namely, a single-stage cascode operational amplifier with 100% feedback, an enabling/disabling switch controlled by the *Enable* logic signal produced in the digital part of the IC, a simplest voltage-to-current converter on a high-resistance (100 kΩ) resistor, and an additional circuit on current mirrors CM_1 and CM_2 providing the differential current output.

In the ИМСКД2, when the *Enable* signal is absent, the output stage is de-energized, and, in this case, the consumption of the IC decreases. The *N*-channel transistor, converting the voltage of the output multiplexer into a current, simultaneously produces an *MUX_OUT* voltage monitor signal.

Two current mirrors based on complementary transistors convert this current into a differential one. The

Fig. 15. Typical response of the THU in the (a) small- and (b) large-signal modes. The scale (a) in the vertical direction is (*1*, *2*) 500 mV/division, and in the horizontal direction is 20 μs/division; (b) (*1*) 1 V/division, and (*2*) 500 mV/division, and in the horizontal direction is 20 μs/division.

circuit design of the current mirrors in the ИМСКД2 is modified to exclude a current jump, when the stage bias is turned on in response to the *Enable* signal. The outputs of the current mirrors in paraphase generate a current into the load with a 50-μA/V conversion factor and are intended for operation with a load capacitance value of up to 10 pF. There is the external output stage biasing pad for optimizing the working point. A typical oscillogram of the current-mirror response for an *Outp* positive signal is shown in Fig. 14.

THU. In the ИМСКД2 version, the THU was modified mainly to reduce the power consumption. The operation of the THU circuit in the small-signal mode is shown in Fig. 15. A decrease in the current consumption negatively influenced the THU operation in the large-signal mode. As follows from Fig. 15b, the signal rise and fall rate in the large-signal mode has increased as compared to the ИМСКД1, leading to a decrease in the ИМСКД2 speed.

REFERENCES

1. Basiladze, S.G., Bogdanova, G.A., Volkov, V.Yu., et al., *Prib. Tekh. Eksp.*, 2006, no. 3, p. 52 [*Instrum. Exp. Tekh.* (Engl. Transl.), 2006, no. 3, p. 350].
2. Ganel, J., Adams, J.H., Ahn, H.S., et al., *Nucl. Instrum. Methods Phys. Res., Section A*, 2005, vol. 552, no. 3, p. 409.
3. O'Brien, E., Karmanov, D., Merkin, M., et al., *XII Intern. Conf. "Calorimetry in High Energy Physics (CALOR 06)," Chicago, Illinois, 2006*, AIP Conf. Proc. 867, 2006, pp. 132–138.
4. IDEAS. Specifications. Model VA1.
5. Atkin, E.V., Voronin, A.G., Korolev, M.G., et al., *Prib. Tekh. Eksp.*, 2010, no. 2, p. 74.
6. IDEAS. Specifications. Model VA32HDR14.2.