ISSN 0018-151X, High Temperature, 2019, Vol. 57, No. 6, pp. 870–877. © Pleiades Publishing, Ltd., 2019.

THERMOPHYSICAL PROPERTIES OF MATERIALS

Synthesis and Investigation of Al/Sn/La_2O_3 Nanocomposite for Gate Dielectric Applications

M. Nakhaei[a], *, M. Ebrahimzadeh[a], M. Padam[a], and A. Bahari[a]

[a] *Department of Solid State Physics, University of Mazandaran, Babolsar, Iran*

**e-mail: mnakhaei137@gmail.com*

Received July 8, 2016; revised October 29, 2016; accepted December 27, 2016

Abstract—In this research, TGA technique was used for determining thermal and gravimetrical stability of Al/Sn/La_2O_3 nanostructures prepared by sol-gel and spin-coating methods. Structural properties and surface morphology of the films were investigated by different analysis methods. Energy dispersive X-ray spectroscopy and a map were used to make a quantitative chemical analysis of unknown materials. Electrical properties of the samples were measured by metal-dielectric-semiconductor through capacitance—voltage and current rate—voltage. The conduction mechanism in the electrical field below 0.12 MV/cm and in the temperature range of 335 K < T < 420 K was found to be ohmic emission. A model of thermal excitation is proposed to explain the mechanism of ohmic conduction current. The highest value of dielectric constant (k) was ~32 at T_1 = 200°C with almost amorphous structure. The results showed that at T_1 = 200°C the Al/Sn/La_2O_3 nanostructure has lower leakage current rate and higher capacitance than those for other samples because of almost amorphous structure.

DOI: 10.1134/S0018151X19060191

INTRODUCTION

The metal-oxide-semiconductor field effect transistors (MOSFETs) play an important role in ultra-large-scale integration (ULSI) that is used in electric products, for example: personal computers, digital cameras and mobile phones [1]. Geometrical size of MOSFETs with high dielectric constant k is important for processing speed and electrical power dissipation [2]. Gate dielectric plays a major role in the MOSFETs performance [3]. Silicon dioxide (SiO_2) with atomic layer was used as gate dielectric material in the current MOSFETs [4]. Facing some problems, such as high leakage currents, tunneling currents, high power dissipation, and boron diffusion becomes a critical issue for SiO_2 gate dielectric [4]. Some researchers suggest materials with high k demonstrate lower leakage and tunneling currents as well as lower boron diffusion [5]. The results of researches show that uncommon earth oxides like lanthanum oxide (La_2O_3) can be suitable for MOSFETs because of high dielectric constant [6–8]. Nanomaterials with amorphous structure and flat surface can make tunneling and leakage currents and boron diffusion less in MOSFETs gates [9, 10]. La_2O_3 has high k (around 27) [11], but its crystallinity temperature is above 400°C [12]. It has the properties of p-type semi-conducting because its resistivity decreases with increasing temperature [13]. Aluminum can make composites more amorphous [14, 15]. In this research, we also used SnO because of its good effects such as thermal stability [16–18].

In this paper, we tried to synthesize and investigate the material and dielectric properties of La_2O_3 doped with Al and Sn expecting that nanocrystallites can be used as a good gate dielectric for the future MOSFET generations.

EXPERIMENTAL PROCEDURES

In this work, lanthanum chloride ($LaCl_3 \cdot 7H_2O$), cetyl trimethyl ammonium bromide (CTAB), ammonia (25%), aluminum tri-sec-butylate ($C_{12}H_{27}AlO_3$), acetyl acetone ($C_2H_5O_8$), isopropyl alcohol (C_3H_8O), tin (II) chloride ($SnCl_2$), and H_2O were used to synthesize Al/Sn/La_2O_3 nanostructure. All materials in this research were of analytical reagent grade purchased from Merck (Darmstadt, Germany) unless otherwise stated. The synthesis of La_2O_3 nanostructure was carried out as follows. Firstly, 0.91 g of CTAB were put into 102 mL of distilled water under magnetic stirring at room temperature. Then 2.0 g of $LaCl_3 \cdot 7H_2O$ were added with stirring to form a homogeneous transparent solution, and 3.0 mL of ammonia (25%) was added dropwise to adjust the pH value of the solution to 10.0. Along with the addition of ammonia, the solution was turned translucent colloidal.

Then 0.3 mL of $C_{12}H_{27}AlO_3$ were dissolved in 0.5 mL of C_3H_8O and 0.5 mL of $C_2H_5O_8$ under magnetic stirring at room temperature. Simultaneously 0.54 g of $SnCl_2$ with 0.1 g CTAB were dissolved in 10.0 mL of distilled water under magnetic stirring at room temperature. After that both solutions were

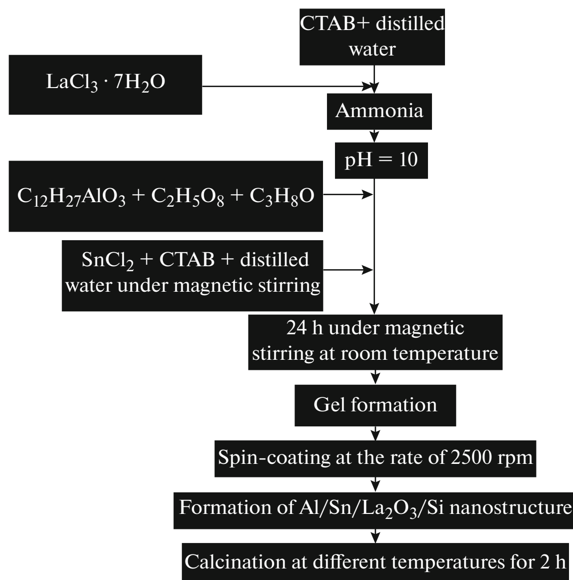


Fig. 1. The schematic flow chart of the $Al/Sn/La_2O_3$ nanostructure synthesis process.

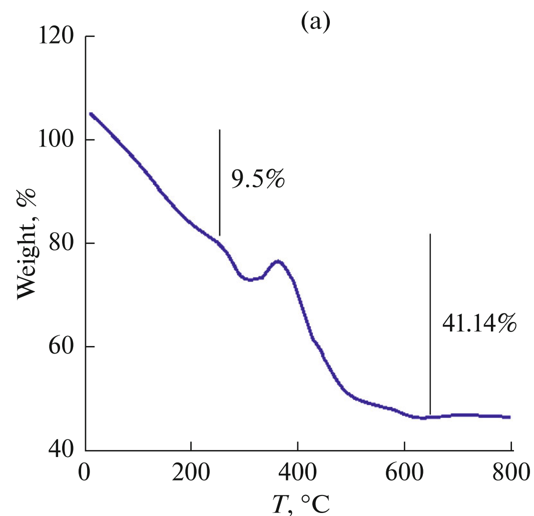
added to La_2O_3. After magnetic stirring for 24 h, the gel was coated on Si substrate at 2500 rpm to form $Al/Sn/La_2O_3$ nanostructure. The surfaces of these nanostructures were uniform enough. After that $Al/Sn/La_2O_3$ nanostructures were calcined at $T_1 = 200°C$, $T_2 = 300°C$, $T_3 = 400°C$, and $T_4 = 600°C$. The molar ratios for all four samples were $[C_{12}H_{27}AlO_3]/[LaCl_3 \cdot 7H_2O] = 1/5$ and $[SnCl_2]/[LaCl_3 \cdot 7H_2O] = 4/5$. The samples were investigated with several techniques such as thermogravimetric analysis (TGA), X-ray diffraction (XRD), Fourier transfer infrared radiation (FTIR), scanning electron microscopy (SEM), atomic force microscopy (AFM), energy dispersive X-ray (EDX), X-map, capacitance–voltage curve (C–V), and current rate–voltage curve (J–V). Figure 1 shows the schematic flow chart of the $Al/Sn/La_2O_3$ nanostructure synthesis process. The sample's characteristics are shown in Table 1.

RESULTS AND DISCUSSION

TGA curve for $Al/Sn/La_2O_3$ nanostructure is shown in Fig. 2a. The TGA showed 9.5% loss at around 20–200°C because of impurities, such as H_2O

Table 1. Experimental temperatures

Sample no.	T, °C
1	200
2	300
3	400
4	600



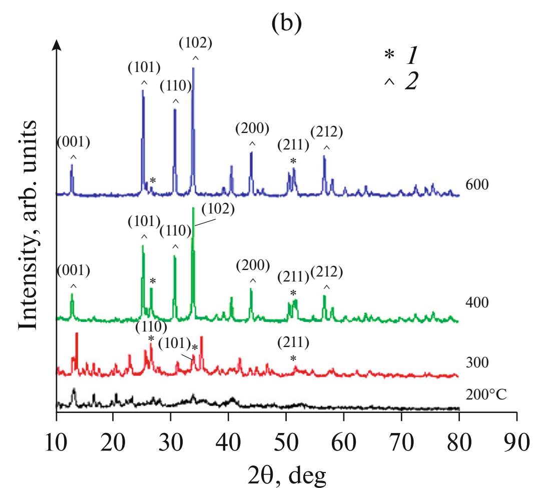


Fig. 2. (a) TGA measurement and (b) XRD patterns of $Al/Sn/La_2O_3$ nanostructures at different calcination temperatures: (*1*) SnO_2 and (*2*) LaOCl.

and Cl_2 [19]. At temperatures from 250 to 600°C, $Al/Sn/La_2O_3$ nanostructure weight was is 41.14%. According to TGA curve this nanostructure became stable after $T = 600°C$.

The XRD patterns of the samples are shown in Fig. 2b. At $T_1 = 200°C$, $Al/Sn/La_2O_3$ nanostructure has almost amorphous structure. Amorphous structures have lower tunneling and leakage currents and boron diffusion than crystalline ones in MOSFETs gates [20]. Some dominant peaks also appeared at T_2, T_3, and T_4. The Joint Committee on Powder Diffraction Standards (JCPDS) numbers of XRD peaks of SnO_2 (tetragonal) and LaOCl (tetragonal) are 21-1250 and 08-0477, respectively.

XRD patterns of the $Al/Sn/La_2O_3$ nanostructure showed diffraction peaks absorbed at 2θ values in Fig. 2b. The prominent peaks were used to calculate the nanocrystalline size through the Scherrer equation. Since the Scherrer equation is used for spherical crystallites,

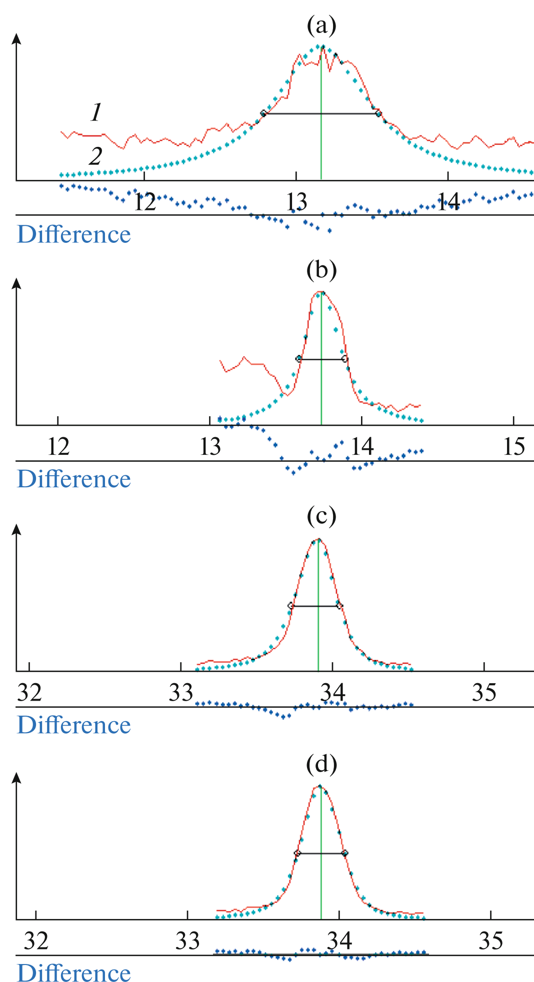


Fig. 3. The grain sizes of Al/Sn/La_2O_3 nanostructures calculated with X-powder software: (a) $T_1 = 200°C$, (b) $T_2 = 300°C$, (c) $T_3 = 400°C$, and (d) $T_4 = 600°C$.

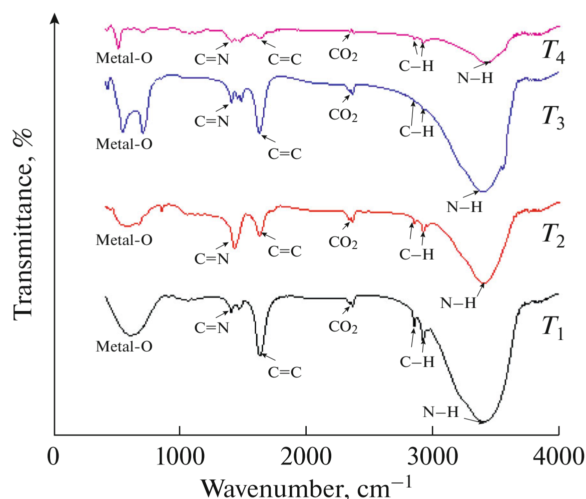


Fig. 4. Comparison of FTIR spectra of Al/Sn/La_2O_3 nanostructure at different calcination temperatures.

we used the X-powder software. The crystalline phase (tetragonal) of the highest peak (102) in XRD patterns was used for measuring the crystalline sizes of the samples. The crystalline sizes of Al/Sn/La_2O_3 nanostructures were shown in Fig. 3. These sizes were about 13 to 35 nm.

The grains sizes changed with the temperature changing. Mechanical strength was increased by reducing the grain size of Al/Sn/La_2O_3 nanostructures [21]. The relation between yield and grains size is described mathematically by the Hall–Petch equation [21]

$$\sigma_y = \sigma_0 + \frac{k_y}{\sqrt{D}}.$$

Here, σ_y is the yield stress, σ_0 is a material's constant for the starting stress for dislocation movement (or the resistance of the lattice to dislocation motion), k_y is the strengthening coefficient (unique to each material), and D is the average grains' diameter. Reduction of the grain sizes, the yield strength, and yield stress of the Al/Sn/La_2O_3/Si nanostructure decrease and so more mechanical stable structure of samples can be produced, which can prevent light atom penetration and leakage current. Al/Sn/La_2O_3 nanostructure at $T_1 = 200°C$ had almost amorphous structure with grain size of ~13 nm that it was calculated by X-powder software or Scherrer correction (see Fig. 3).

The FTIR technique was used for characterizing the purity and quality of conjunctions. The FTIR spectra is shown in Fig. 4. Absorption characteristic bands of Al/Sn/La_2O_3 nanostructures are given in Table 2. The NH_2 and CO_2 absorption peaks reduce with increasing temperature in the sample. The junctions of dipoles, such as C=C and C=N at 1440 and 1600 cm^{-1} wave numbers decreased with increasing temperature (Fig. 4). Absorption of the samples at $\lambda = 600$ cm^{-1} decreased with increasing temperature, so Al/Sn/La_2O_3 nanostructure at $T_1 = 200°C$ had stronger metal-O junctions [22].

The surface morphology of the dielectric layer was studied by the SEM technique. SEM images of Al/Sn/La_2O_3 nanostructures are shown in Fig. 5. These SEM images support the XRD analysis. The

Table 2. FTIR absorption characteristic bands of Al/Sn/La_2O_3 nanostructure [22]

Band assignation	Wavenumber, cm^{-1}
N–H in NH_2 group	3400
CO_2	2400
C=C	1600
Stretching conjunction of C=N	1440
La-O	600

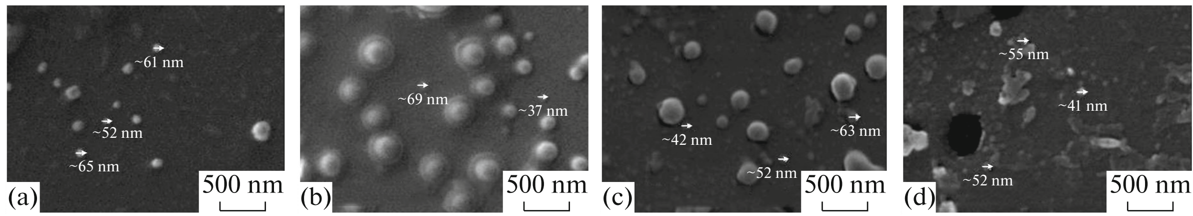


Fig. 5. SEM images of $Al/Sn/La_2O_3$ nanostructures at different calcination temperatures: (a) T_1, (b) T_2, (c) T_3, and (d) T_4.

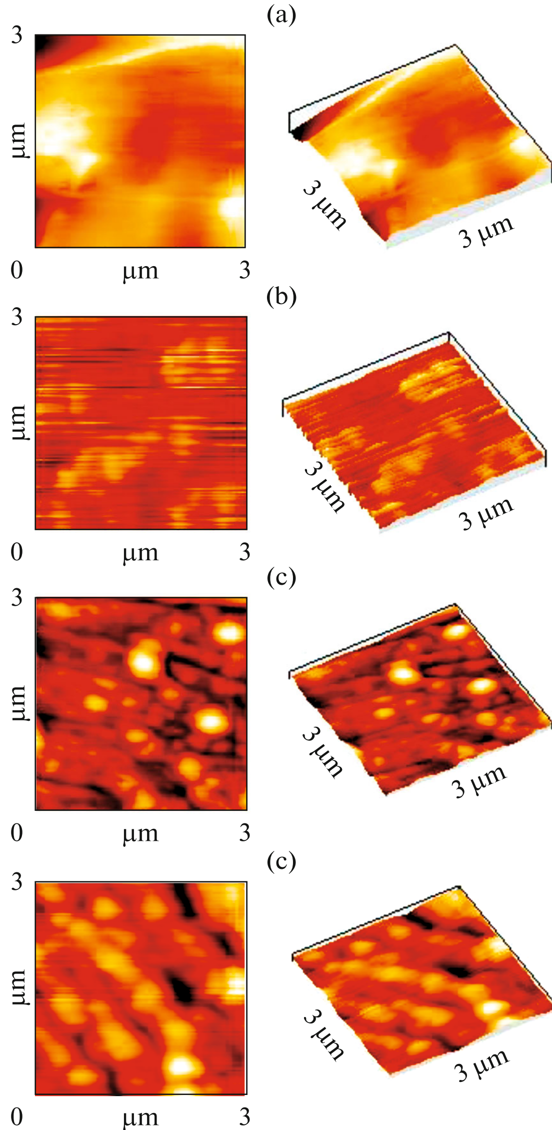


Fig. 6. AFM images of $Al/Sn/La_2O_3$ nanostructure at different calcination temperatures: (a)–(d) see Fig. 5.

structure phases changes at higher temperatures. These images show that almost uniform structure was formed at T_1 = 200°C because of its almost amorphous structure. In SEM images the average grains size of these nanostructures were ~ 40 to 60 nm. According to the SEM image of $Al/Sn/La_2O_3$ nanostructure, the surface of $Al/Sn/La_2O_3$ nanostructure at T_2 = 200°C was formed more smooth than other samples. It was clear that the number of trapping of charge carrier decreased in this sample, and we could result that mobility μ of carriers increased at T_2 = 200°C. In agree with equation [23]

$$\sigma = q\left(n\mu_e + p\mu_p\right),$$

where σ is the conductivity ($\sigma = \frac{j}{E}$), q is the electric charge, μ_p and μ_e are electric mobility of positive and negative electric charges. Conductivity increased with increasing mobility of $Al/Sn/La_2O_3$ nanostructure at T_2 = 200°C. In addition, according to the relation between dielectric constant ε and σ [24]:

$$\varepsilon(w) = 1 + \frac{4\pi i\sigma}{w}, \tag{1}$$

dielectric constant will increase with increasing conductivity. Here, $w = 2\pi\upsilon$ and υ is frequency.

Moreover, statistical properties of a surface-like surface roughness were described with AFM technique. The surface roughness was described with topography spectra (Fig. 6) and DME software images. The roughness causes light dispersion and absorption. The surface roughness (Table 3) such as the roughness average S_a, the mean value S_m, the peak-valley height S_y and the root mean square S_q of the $Al/Sn/La_2O_3$ nanostructure were determined using DME software.

DME software reaches different roughness parameter (Table 3) at different temperatures. In this paper, the $Al/Sn/La_2O_3$ nanostructure at T_1 = 200°C showed much decrease in S_m than others. According to average roughness S_a, uniform surface was observed for $Al/Sn/La_2O_3$ nanostructure at T_1 = 200°C (S_a = 19.2 nm). These measurements showed that this sample had a flat and smooth surface morphology. It made $Al/Sn/La_2O_3$ nanostructure at T_1 more stable to local shear than other samples. Lower roughness and crack free of the $Al/Sn/La_2O_3$ nanostructure at T_1 with almost amorphous structure made it possible to have more mechanical stability. The reason was that lower cracks could reduce the leakage current and light atom penetration through the gate materials in MOSFETs [25].

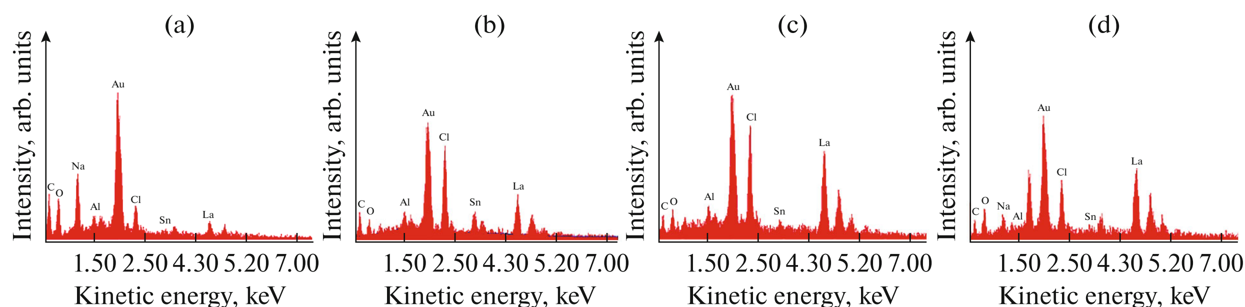


Fig. 7. EDX of $Al/Sn/La_2O_3$ nanostructures at different temperatures: (a)–(d) see Fig. 5.

EDX technique was used to make a quantitative chemical analysis of the prepared composite. Figure 7 shows the EDX spectra of $Al/Sn/La_2O_3$ nanostructure at different temperatures. EDX spectra indicated that all four samples were composited of La, Al, and Sn. EDX spectra was taken from a point but not from an area, so Si from the substrate isn't in the spectrum. The values of peaks in EDX spectra and chemical composition of $Al/Sn/La_2O_3$ are shown in Table 4.

Table 3. Roughness parameters of $Al/Sn/La_2O_3$ nanostructure at different calcination temperatures (image fraction is 100%)

Sample no.	T, °C	S_a, nm	S_q, nm	S_m, fm	S_y, nm
1	200	19.2	23.5	−0.90	38.9
2	300	155	196	−12.0	380
3	400	20.5	25.9	−1.68	41.8
4	600	23.1	31.0	−4.38	91.5

X-map images of $Al/Sn/La_2O_3$ nanostructure at T_1 are shown in Fig. 8. These images were used to show distribution of elements, then confirmed by EDX technique.

Capacitance–voltage curve (C–V) is affected with capacitive response of interface traps and oxide charges. Figure 9a shows C–V characteristics of $Al/Sn/La_2O_3$ nanostructures at different temperatures. The C–V curves were taken at 1 MHz for $Al/Sn/La_2O_3/Si$ MOS structures with 15.6-nm thick $Al/Sn/La_2O_3$ films (before calcination). The variation of the capacitance C with gate voltage V_G ranging from −3.0 to 3.0 V. The maximum accumulation capacitance of the $Al/Sn/La_2O_3$ was ~2027 nF. The accumulation capacitance C_{acc} of the as-deposited amorphous $Al/Sn/La_2O_3$ film was higher than that for other $Al/Sn/La_2O_3$ films and the dielectric constant was ~32 for sample with almost amorphous structure (the sample at T_1). The capacitance of $Al/Sn/La_2O_3$ nanostruc-

Table 4. Elements composition obtained from EDX analysis

Elements	Weight, %	Atomic, %	Z	Absorption	Fluoroscence
T_1 = 200°C					
Al K	16.28	49.35	1.2457	0.4024	1.0010
Sn L	13.29	9.16	0.9673	0.9464	1.0262
La L	70.43	41.48	0.9307	0.9796	1.0000
T_2 = 300°C					
Al K	6.07	24.23	1.2912	0.3812	1.0012
Sn L	21.97	19.94	1.0022	0.9487	1.0249
La L	71.97	55.83	0.9662	0.9618	1.0000
T_3 = 400°C					
Al K	4.31	18.70	1.3080	0.3554	1.0009
Sn L	4.80	4.73	1.0151	0.9361	1.0358
La L	90.89	76.57	0.9796	0.9923	1.0000
T_4 = 600°C					
Al K	1.80	8.55	1.3221	0.3470	1.0009
Sn L	3.84	4.16	0.0259	0.9343	1.0374
La L	94.36	87.29	0.9906	0.9933	1.0000

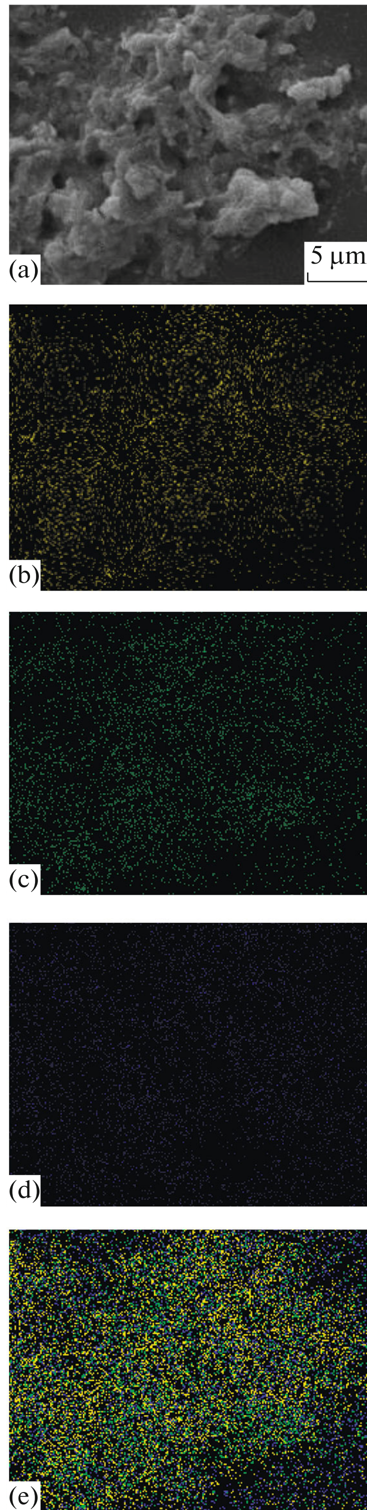


Fig. 8. Microstructure of $Al/Sn/La_2O_3$ calcined at T_1: (a) BSE image; map images elements: (b) La, (c) Sn, (d) Al, and (e) Al/Sn/La.

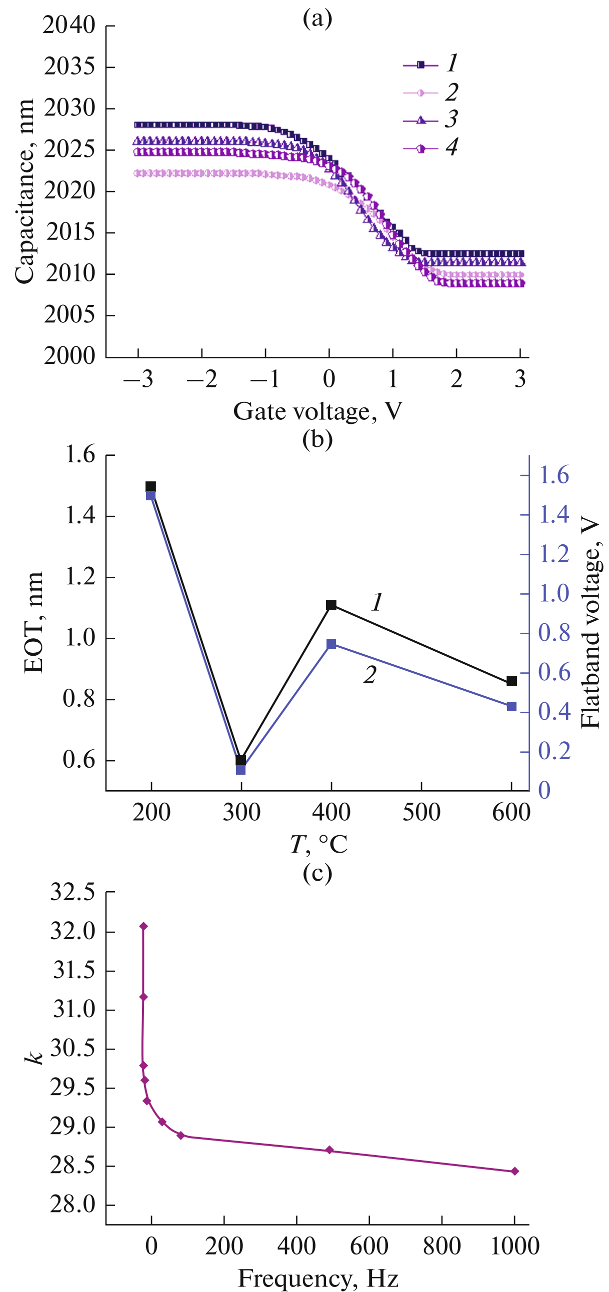


Fig. 9. (a) C–V curve of $Al/Sn/La_2O_3$ nanostructures: (*1*)–(*4*) T_1–T_4, (b) EOT (*5*) and Flatband voltage (*6*) results at different calcination temperatures, and (c) variations of k at different frequencies for $Al/Sn/La_2O_3$ nanostructure at T_1.

tures decreased with increasing gate voltage (Fig. 9a). The capacitance decreases to the superimposed voltage with increasing calcination temperatures, because of high leakage current rate.

The equivalent oxide thickness (EOT) is an important parameter in MOSFETs. The EOT D_{eq} of the samples was calculated according to equation from [25]:

$$\frac{D_{eq}}{\varepsilon_{r,SiO_2}} = \frac{D_{high-k}}{\varepsilon_{r,high-k}},$$

where ε_r is dielectric constant. Figure 9b shows the EOT and flatband voltage of $Al/Sn/La_2O_3$ nanostructures calcined at different temperatures. The maxi-

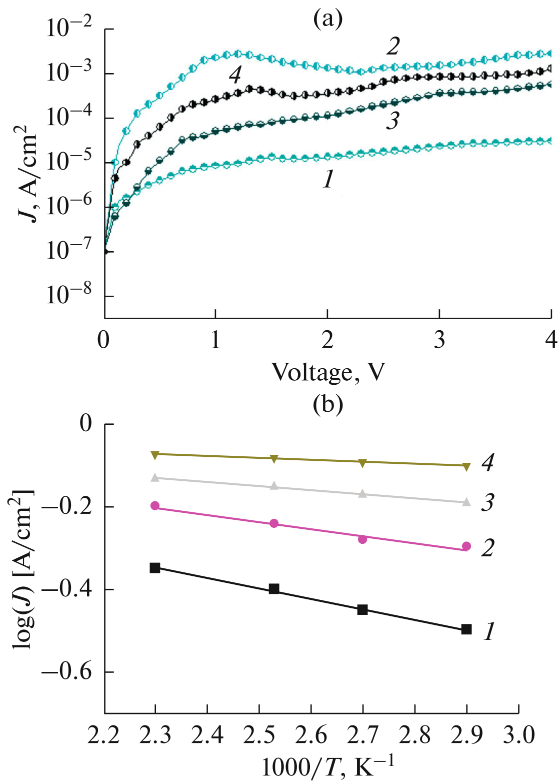


Fig. 10. (a) J–V characteristics of $Al/Sn/La_2O_3$ nanostructures at different calcination temperatures: (*1*)–(*4*) T_1–T_4 and (b) logarithmic current rate vs. $1000/T$ under negative bias: (*1*) 0.05 V, (*2*) 0.1, (*3*) 0.15, and (*4*) 0.2.

mum values of EOT and k were ~1.5 nm and ~32 for the sample at T_1.

The dielectric constant of $Al/Sn/La_2O_3$ nanostructure was investigated to see its response to an applied low a.c. voltage in the frequency range from 100 to 1.0 MHz. In Fig. 9c variations of k on frequency are shown. It can be observed that dielectric constant decreases with increasing frequency that could be confirmed with Eq. (1). The highest value of k is ~32 at 100 Hz and T_1 with relatively amorphous structure.

Figure 10a shows the current rate–voltage (J–V) curves for $Al/Sn/La_2O_3$ nanostructure at different calcination temperatures for positive bias voltage from 0 to 4.0 V. The curves were obtained in the temperature range from 335 to 420 K. Leakage current rates were below 10^{-2} A/cm^2 for all samples. The leakage current increased with increasing calcination temperatures because of more crystalline structure. From Fig. 10a it is evident that $Al/Sn/La_2O_3$ nanostructure at T_1 has lower leakage current rates (~8×10^{-6} A/cm^2) than other samples because of almost amorphous structure. Mathematically, the expression for current rate according to Poole–Frenkel model [22] can be written as

$$J = AT^2 \exp \frac{1}{k_B T}\left[\left(\frac{57.7\,\text{eV}}{Kd}\right)^{1/2} - \varphi_t\right],$$

where d is electrode spacing in Å, φ_t is the depth of the trap potential well and A is the Richardson constant having a value of 120 A/cm^{2}K^2, k_B is the Boltzmann constant.

The plot of log(J) versus $1000/T$ at applied voltage $V < 0.2$ V and in the temperature range of 335 K $< T <$ 420 K for sample 1 was shown in Fig. 10b. To study the conduction mechanism at lower electric field and higher temperature, ohmic emission was considered because of a strong dependence on applied temperature and electric field. Current rate equation for ohmic conduction could be written as follows [26]:

$$J = qN_c\mu E \exp\left(\frac{-\Delta E_{ac}}{k_B T}\right).$$

Here, q is the electron charge and μ is the electron mobility in insulator, ΔE_{ac} is the electron activation energy that can be obtained from the curve fitting value of log(J) versus $1000/T$ plot in Fig. 10b, and

$$N_c = 2\left(\frac{2\pi m^* k_B T}{h^2}\right)^{\frac{3}{2}}$$

is the effective density of states in the conduction band [27], m^* is electron effective mass, which can be assumed as $m^* = 0.3m_0$, m_0 is free electron mass. Following equation presents the hopping electron concentration [28]

$$n = N_c \exp\left(\frac{-\Delta E_{ac}}{k_B T}\right).$$

According to Table 5, with increasing electric field, the activation energy decreases and the hopping electron concentration increases.

As was clear, the electron mobility with increasing electric field decreases that could be due to an increase in density of electron cloud overlap. Whatever the

Table 5. Parameters of the ohmic conduction were calculated with varied voltages for the sample no. 1 (T_1 = 200°C) at 335 K

Applied voltage, V	E, MV/cm	Slope, (A – K)/cm^2	ΔE_{ac}, eV	Hopping electron concentration, 10^{20} cm^{-3}	Intercept, A/cm^2	μ, 10^{-12} cm^2/V s
0.05	0.03	–0.25	0.23	1.08	0.234	4.52
0.1	0.06	–0.17	0.19	1.82	0.194	2.34
0.15	0.09	–0.10	0.10	2.24	0.103	1.03
0.2	0.12	–0.05	0.04	3.00	0.046	0.226

overlapping of adjacent atoms is more, electrons can easily move along the electric field.

Thus, the hopping electron concentration was 3.00×10^{20} cm^{-3} at the electric field of 0.12 MV/cm and temperature of 335 K. The very low carrier mobility and concentration resulted in the low conduction current in $Al/Sn/La_2O_3$ (as-prepared) thin film. All the parameters at 335 K were calculated (Table 5).

CONCLUSIONS

In this research, the TGA analysis of $Al/Sn/La_2O_3$ nanostructure showed that loss of weight till 600°C reaches 50.64% and the impurities became less with increasing the temperature. In addition, TGA analysis showed good thermal stability after 600°C. The XRD analysis showed almost amorphous structure of $Al/Sn/La_2O_3$ that was calcined at $T_1 = 200$°C with 13 nm grain size. The effects of calcination on the surface topography were investigated by AFM technique, and it was found that the roughness values for the gate dielectric materials were increased increasing temperature. One reason for this is that calcination can increase the density of $Al/Sn/La_2O_3$ nanostructure.

It was found that with the calcination temperature increasing the roughness of the gate dielectric decreases. This reduces the grain boundaries in the conduction channel for higher mobility of MOSFET devices. C–V measurements taken at 1 MHz, showed that the maximum capacitance of $Al/Sn/La_2O_3$ nanostructure was at T_1. The results of experiments (such as J–V dependences) showed that the $Al/Sn/La_2O_3$ nanostructure at $T_1 = 200$°C has lower leakage current rate and higher capacitance than that of other samples because of almost amorphous structure. The leakage current rate was about 8×10^{-6} A/cm^2. The conduction mechanism in the electrical field below 0.12 MV/cm and in the temperature range of 335 K $< T <$ 420 K was found to be ohmic emission. Very low carrier mobility and concentration result in the low conduction current in $Al/Sn/La_2O_3$ (as-prepared) thin film. A model of the thermally excited electron was proposed to explain the mechanism of the ohmic conduction in $Al/Sn/La_2O_3$ (as-prepared) thin film. These properties can also prevent leakage current, tunneling current and boron diffusion through the thin $Al/Sn/La_2O_3$ nanostructure. At last we can introduce $Al/Sn/La_2O_3$ nanostructure at $T_1 = 200$°C as a good candidate for gate dielectric for MOSFETs devices.

REFERENCES

1. Morgan, P., Bahari, A., and Robenhagen, U., *J. Vac. Sci. Technol., A*, 2005, no. 23, p. 201.
2. Bahari, A., Ebrahimzadeh, M., and Gholipur, R., *Int. J. Mod. Phys. B*, 2014, vol. 28, 1450102.
3. Khorshidi, Z., Bahari, A., and Gholipur, R., *J. Electron. Mater.*, 2014, vol. 48, no. 11, p. 4349.
4. Kuei, P.Y., Chou, J.D., Huang, C.T., Ko, H.H., and Su, S.C., *J. Cryst. Growth*, 2011, vol. 314, no. 1, p. 81.
5. Bahari, A. and Ramzannejad, A., *Int. J. Mod. Phys. B*, 2012, vol. 26, 1250080.
6. Bahari, A., Morgan, P., and Li, Z., *Surf. Sci.*, 2008, vol. 602, p. 2315.
7. Promsuy, S., Tangtrakarn, A., Mongkolkachit, C., Wanakitti, S., and Amornkitbamrung, V., *J. Sol-Gel Sci. Technol.*, 2015, vol. 74, p. 187.
8. Bahari, A. and Gholipur, R., *Int. J. Mod. Phys. B*, 2012, vol. 26, 1250191.
9. Chowdhury, H.M., Mannan, A.M., and Mahmood, A.S., *Emerging Tech. Sci. Eng.*, 2010, vol. 2, p. 1.
10. Bahari, A. and Roodbari, M., *J. Mod. Phys.*, 2013, vol. 4, p. 1.
11. Kale, S., Jadhav, K., Patil, P., Gujar, T., and Lokhande, C., *Mater. Lett.*, 2005, vol. 59, p. 3007.
12. Houssa, M., Tuominen, M., Naili, M., Afanas'ev, V., Stesmans, A., Haukka, S., and Heyns, M., *J. Appl. Phys.*, 2000, vol. 87, p. 8615.
13. Ng, J.A., Kuroki, Y., and Sugi, N., *Microelectron. Eng.*, 2005, vol. 80, p. 206.
14. Eslami, A., Haghighi, M., Rahemi, N., and Nasiri Laheghi, S., *Int. Conf. Adv. Mater. Proc. Technol.*, 2010, p. 1297.
15. Bahari, A. and Gholipur, R., *J. Electron. Mater.*, 2013, vol. 12, p. 3539.
16. Xu, W., Xia, L., Ju, J., Xi, P., Cheng, B., and Liang, Y., *J. Sol-Gel Sci. Technol.*, 2016, vol. 78, p. 353.
17. Okamura, K., Nasr, B., Brand, R.A., and Hahn, H., *J. Mater. Chem.*, 2012, vol. 22, no. 11, p. 4607.
18. Thanachayanont, C., Yordsri, V., and Boothroyd, C., *Mater. Lett.*, 2011, vol. 65, p. 2610.
19. Refa, M. and Melsabawy, K., *Bull. Mater. Sci.*, 2011, vol. 4, p. 873.
20. Roodbari, M., Rezaee, M., and Shahtahmasbi, N., *Int. J. ChemTech. Res.*, 2011, vol. 3, p. 1681.
21. Hansen, N., *Scr. Mater.*, 2004, vol. 51, p. 801.
22. Bahari, A. and Gholipur, R., *J. Mater. Sci.: Mater. Electron.*, 2012, vol. 24, p. 674.
23. Hayati, A., Bahari, A., Ramzannejad, A., and Jafari, R., *Res. J. Recent Sci.*, 2015, vol. 4, p. 23.
24. Ashcroft, N.W. and Mermin, N.D., *Solid State Physics*, New York: Holt, Rinehart and Winston, 1976, p. 16.
25. Yamaguchi, T., Satake, H., Fukushima, N., and Toriumi, A., *Int. Electron Devices Meet.*, 2000, vol. 63, p. 19.
26. Sze, S.M., *Physics of Semiconductor Devices*, New York: Wiley, 1981, 2nd ed.
27. Houssa, M., Tuominen, M., Naili, M., Afanas, V., Stesmans, A., Haukka, S., and Heyns, M., *J. Appl. Phys.*, 2000, vol. 87, p. 8615.
28. Mahapatra, R., Lee, J.H., Maikap, S., Kar, G.S., Dhar, A., Hwang, N.M., Kim, D.Y., Mathur, B.K., and Ray, S.K., *Appl. Phys. Lett.*, 2003, vol. 82, p. 2320.