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Fabrication of high performance thin-film transistors via pressure-induced nucleation

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We report a method to improve the performance of polycrystalline Si (poly-Si) thin-film transistors (TFTs) via pressure-induced nucleation (PIN). During the PIN process, spatial variation in the local solidification temperature occurs because of a non-uniform pressure distribution during laser irradiation of the amorphous Si layer, which is capped with an SiO_2 layer. This leads to a four-fold increase in the grain size of the poly-Si thin-films formed using the PIN process, compared with those formed using conventional excimer laser annealing. We find that thin films with optimal electrical properties can be achieved with a reduction in the number of laser irradiations from 20 to 6, as well as the preservation of the interface between the poly-Si and the SiO_2 gate insulator. This interface preservation becomes possible to remove the cleaning process prior to gate insulator deposition, and we report devices with a field-effect mobility greater than 160 cm^2/Vs.

Since the introduction of thin-film transistors (TFTs) to large-area electronics, developments in the manufacturing technology for TFTs have focused on improving the electrical properties of the films and in reducing the cost to achieve commercialization. TFTs have applications in a number of fields, including displays, biosensors, phototransistors, and memory[1–5].

Amorphous Si (a-Si) has been the dominant technology as the active layer of TFTs over the past few decades; however, the technological limits in performance such as low mobility and poor stability are being reached. To overcome these limitations, devices based on polycrystalline Si (poly-Si) and amorphous oxide semiconductors (AOSs) have been investigated[6–10]. After that, several methods for improving these TFT performances have been extensively reported over the past few years. For example, the optimization of the laser irradiation condition, various TFT structures (perpendicular, parallel, and tilted channel structures), and various Si recrystallization technologies for high performance of poly-Si TFTs were studied[1,7,11–13]. Moreover, the optimization of composition ratio, channel engineering, and various post treatments for high performance of AOS TFTs were also studied[9,10,14]. Although AOSs are attractive materials for the fabrication of transparent and flexible TFTs because of the optical transparency and low-temperature process capability, there remain a number of unsolved problems, including a relatively low mobility (~10 cm^2/Vs) and poor stability. On the other hand, low-temperature poly-Si (LTPS) based on Si recrystallization using lasers has a number of advantages, including a relatively high mobility (~100 cm^2/Vs) and excellent stability; the principal drawback of this technology is the fabrication cost.

Among the various Si recrystallization technologies, excimer laser annealing (ELA) is the most commonly used[6,11]. With this technology, an a-Si thin film is irradiated 10–50 times using an XeCl excimer pulsed laser. This large number of pulses leads to relatively large manufacturing costs, and reducing the number of laser exposures is important in order to reduce the costs of this technology.

We have previously reported a pressure-induced nucleation (PIN) technique to obtain both size- and density-controlled Si nanoparticles (SiNPs), together with an increase in the grain size of poly-Si, by using laser crystallization of an a-Si thin film with a SiO_2 capping layer (C/L)[11]. In PIN mechanism, a non-uniform pressure distribution was proposed to explain the initiation of nucleation and lateral growth which can produce a relatively larger poly-Si grain compared with that produced by conventional ELA. Moreover, the formation of these SiNPs is also attributed to pressure on the liquid Si, which resulted in the growth of SiNPs through the SiO_2 C/L as Si grains grew laterally from the low-pressure region to the high-pressure region (i.e., lower solidification temperature).

Here, we report on the fabrication of high performance of LTPS TFTs using PIN technology. The performance of TFTs is strongly related to the fabrication conditions, which include the number of laser exposures, the SiNP etching time, and the cleaning processes used. Using an SiO_2 C/L, an increased grain size can be obtained with less laser energy density and a reduced number of laser exposures. Moreover, we investigated not only the optimized SiNP etching time under specific laser irradiation conditions, but also performed removal of two conventional essential cleaning processes in poly-Si TFT fabrication: one prior to laser irradiation and one prior to gate insulator deposition, paying special attention to the effects on the performance of the TFTs. Combining all these conditions, we could demonstrate the feasibility of high-performance LTPS TFTs using a cost-effective fabrication method. A top-gate structure was used, and TFTs were fabricated using the process shown in Fig. 1. The experimental process described in more detail below.

Results and discussion

Figures 2a–d show scanning electron microscopy (SEM) images of the Secco-etched poly-Si thin films with 15-nm-thick SiO_2 C/Ls fabricated using the PIN process, and Fig. 2e shows an SEM image of the thin films fabricated with no SiO_2 C/L, i.e., conventional ELA. All the poly-Si thin films were crystallized using a laser intensity of 340 mJ/cm^2, which is larger than the critical laser energy density (i.e., the triggering energy density of lateral grain growth in PIN mechanism[11]).

For the PIN films, as the number of laser exposures decreased, the grain size of poly-Si thin films also decreased. Moreover, SiNPs that were a few tens of nanometers in size were formed on the poly-Si surface as is marked by arrows in Fig. 2. Inset of Fig. 1(a) is a high-resolution transmission electron microscopy (HR-TEM) image showing the SiNP, SiO_2 C/L, and poly-Si thin film. Statistical analysis of the average grain size (see Fig. 2f) is as follows: the grain size was 399.9 ± 60.9 nm for 20 exposures, 383.2 ± 52.8 nm for 10 exposures, 209.6 ± 72.1 nm for 6 exposures, and 69.4 ± 10.7 nm for 5

exposures. The conventional ELA process (with 20 exposures) exhibited an average grain size of 103.1 ± 24.2 nm. The grain size of the poly-Si thin-film formed using the PIN process was approximately four times larger than that formed by ELA under the same laser irradiation conditions (compare Fig. 2a with Fig. 2e). Compared to conventional laser crystallization, with a C/L being present the vapor pressure of the liquid Si builds up pressure between the liquid Si and C/L due to the blocking effect of the SiO_2 C/L. Following the PIN process, a non-uniform pressure distribution underneath the SiO_2 C/L leads to a non-uniform solidification temperature for laser-irradiated a-Si (liquid Si). Nucleation was then readily initiated in the low-pressure points, and lateral growth occurred toward the high-pressure points. Thus, an enlarged grain size of the poly-Si thin film may be obtained through the use of the C/L (i.e., the PIN process) compared with that without the C/L (i.e., conventional ELA).

The transfer characteristics of the poly-Si TFTs fabricated using the PIN process are shown in Fig. 3a. The field-effect mobility (μ_{FET}) can be found using

$$\mu_{FET} = \left(\frac{2}{C_i}\right)\left(\frac{L}{W}\right)(G_{max})^2,$$

and the threshold voltage (V_{th}) was estimated by linear extrapolation of the square root of the transfer characteristics at the maximum gradient (G) according to the following equation:[15,16]

$$V_{th} = V_G - \frac{\sqrt{I_D}}{G_{max}},$$

where

$$G = \frac{\partial \sqrt{I_D}}{\partial V_G},$$

and where we are in the saturation regime, i.e., $V_D > V_G - V_{th}$. In the above expressions, C_i is the gate capacitance per unit area, G_{max} is the maximum gradient of G, and L and W are the channel length and
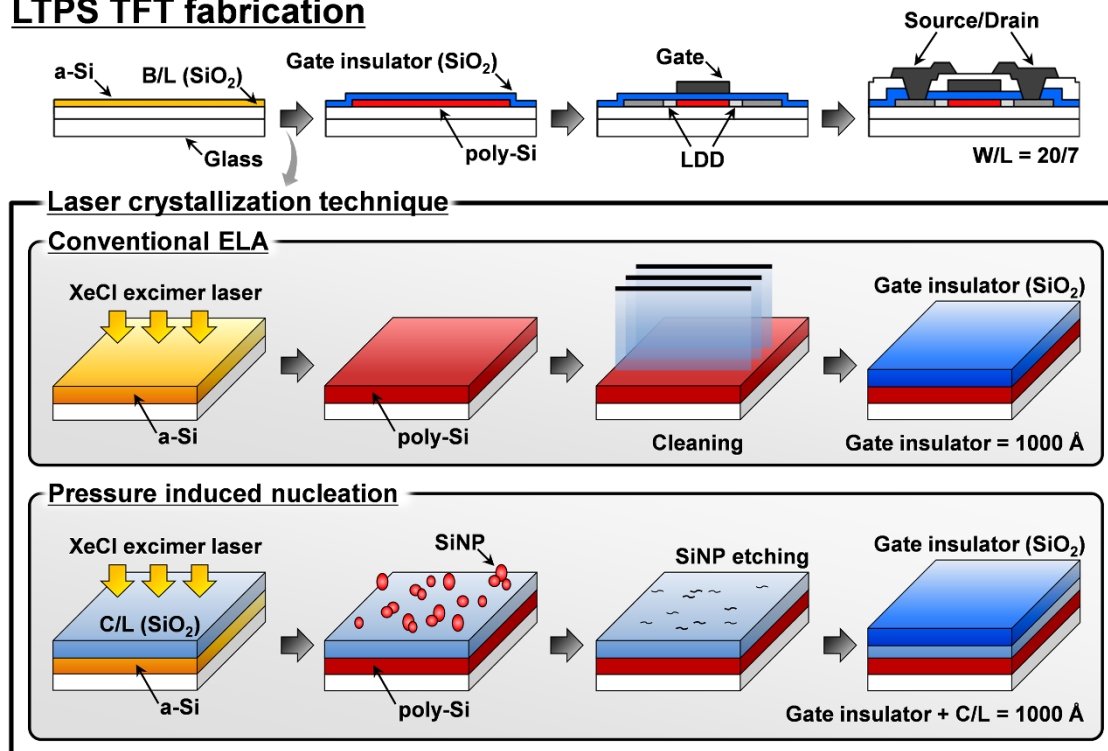
LTPS TFT fabrication

Figure 1 | Schematic illustration of the LTPS TFT fabrication scheme. Two different of laser crystallization techniques were used: conventional ELA and the PIN process.
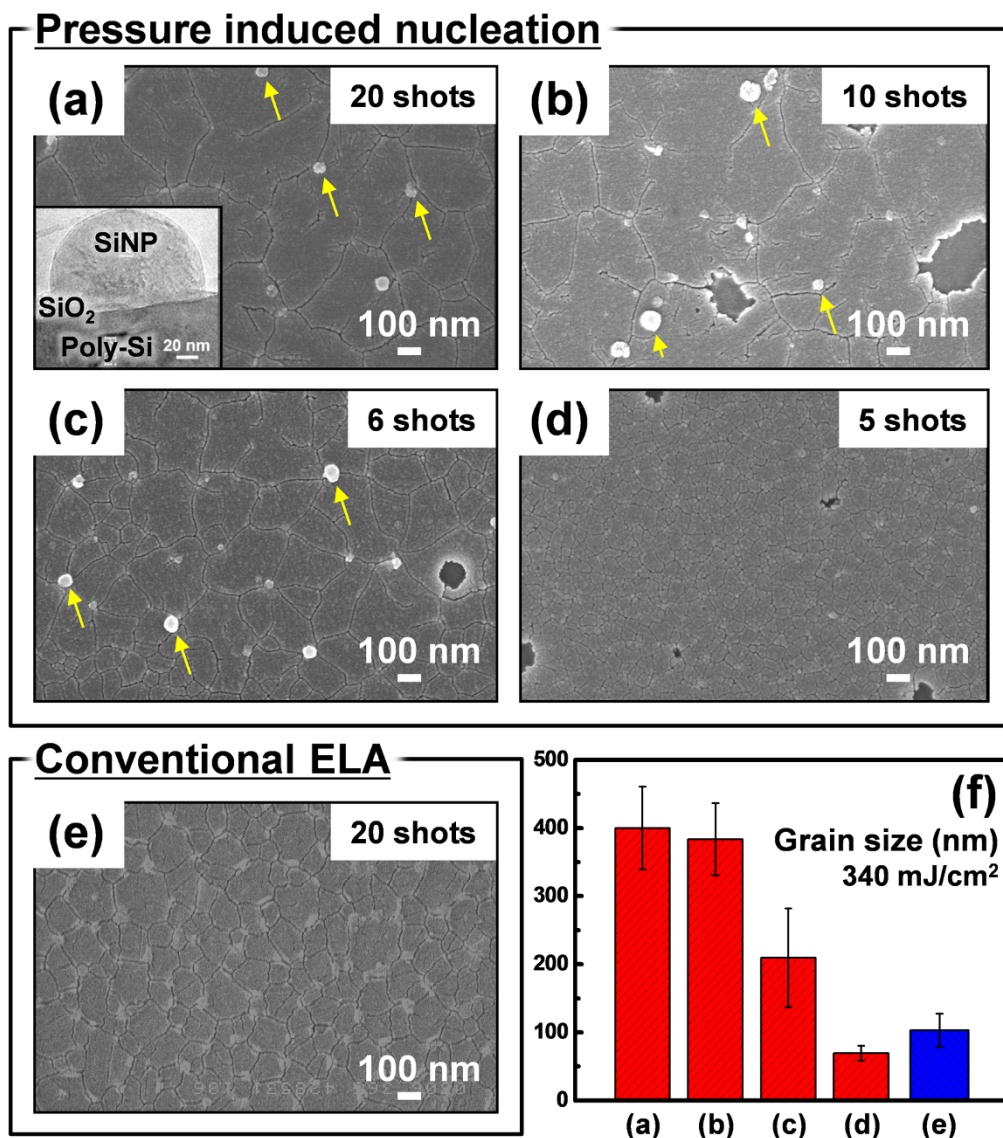
Figure 2 | **SEM images showing the microstructure of the poly-Si thin films.** (a), Secco-etched poly-Si thin film with a 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 using 20 laser exposures. Inset is cross-sectional HR-TEM image showing the SiNP, SiO$_2$ C/L, and poly-Si thin film. (b), Secco-etched poly-Si thin film with 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 using 10 exposures. (c), Secco-etched poly-Si thin film with a 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 using 6 exposures. (d), Secco-etched poly-Si thin film with a 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 using 5 exposures. (e), Secco-etched poly-Si thin film crystallized using conventional ELA. (f), The grain size distribution of the as-prepared samples.

width, respectively; in the devices fabricated as part of this work, the channel dimensions were $L = 7$ μm and $W = 20$ μm.

As shown in Fig. 3b, the number of laser exposures over 6 leads to the similar electrical characteristics of the poly-Si TFTs. The μ_{FET} are over 100 cm^2/Vs for 20, 10, and 6 exposures. However, for fewer than 6 exposures, μ_{FET} decreased abruptly. This is related to the grain size of the poly-Si thin film (see Fig. 2). However, unlike μ_{FET}, there was no variation in V_{th} with the number of laser exposures. It follows that there was no significant effect on the interface between the poly-Si and SiO$_2$ gate insulator during the laser crystallization because SiO$_2$ C/L is covering poly-Si in PIN mechanism. Therefore, it can be concluded that the dramatic reduction of the number of laser exposures from 20 to 6 is possible through grain growth enhancement by PIN mechanism.

The PIN process results in a larger grain size with less laser energy density, and this leads to better performance of the poly-Si TFTs, even though the formation of SiNPs occurred. Because these SiNPs can degrade the electrical properties playing as trap sites at the interface and inside the gate insulator, we carried out an additional SiNP

etching process prior to the fabrication of the poly-Si TFTs to achieve higher TFT performances.

Figures 4a–c shows tilted-surface SEM images of the poly-Si thin films formed using the PIN process following etching of the SiNPs, and Fig. 4d shows tilted-surface SEM images of the poly-Si thin films formed using the conventional ELA process. All the poly-Si thin films were crystallized at 340 mJ/cm^2 and with six laser exposures. The SiNPs were etched using dry etcher, and the etching time was varied from 15 s to 45 s. The poly-Si surfaces fabricated using the PIN process exhibited no SiNPs and were covered with the SiO$_2$ C/L until an etching time of 30 s. After an etching time of 45 s, however, the SiO$_2$ C/L surface became damaged and had the appearance of potholes (see Fig. 4c). With the conventional ELA films, a relatively rough surface of the poly-Si thin film was observed compared to PIN films, as shown in Fig. 4d. This is attributed to protrusions formed due to the rapid melting and solidification processes, as well as the difference in density between the liquid Si and crystalline Si.

We fabricated poly-Si TFTs using the PIN process following etching of SiNPs; the transfer characteristics and electrical parameters are
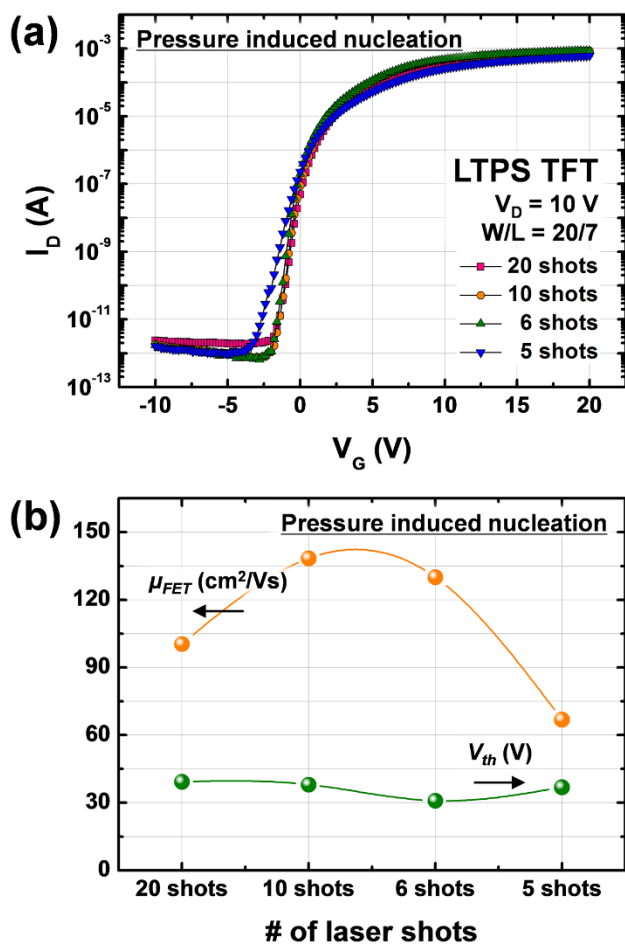
Figure 4 | Tilted SEM images showing the microstructure of poly-Si thin films. (a), A poly-Si thin film with a 15-nm-thick SiO_2 C/L crystallized at 340 mJ/cm^2 following etching of the SiNPs for 15 s. (b), A poly-Si thin film with a 15-nm-thick SiO_2 C/L crystallized at 340 mJ/cm^2 following etching for 30 s. (c), A poly-Si thin film with a 15-nm-thick SiO_2 C/L crystallized at 340 mJ/cm^2 following etching for 45 s. (d), A poly-Si thin film with no SiO_2 C/L crystallized at 340 mJ/cm^2.

Figure 3 | Electrical properties of poly-Si TFTs. (a), The transfer characteristics of the poly-Si TFTs with a 15-nm-thick SiO_2 C/L crystallized at 340 mJ/cm^2 with various numbers of laser exposures. (b), The variation in μ_{FET} and V_{th} with the process conditions.

shown in Fig. 5. The smooth and uniform surface between the poly-Si and SiO_2 C/L was preserved during laser crystallization, deposition of the gate insulator, and the subsequent etching of the SiNPs. With these devices, we find a high field-effect mobility of $\mu_{FET} > 160$ cm^2/Vs, together with a low threshold voltage of $V_{th} < 2$ V. This higher μ_{FET} was achieved after etching of SiNPs compared to the the μ_{FET} (130 cm^2/Vs) shown in Fig. 3b. However, in contrast to the results shown in Fig. 3b, variation in V_{th} was observed with the SiNP etching time. The TFTs with the SiO_2 C/L etched for 45 s exhibited a relatively low mobility of $\mu_{FET} = 90$ cm^2/Vs and a high threshold voltage of $V_{th} = 2.3$ V, as shown in Fig. 5b. This is attributed to the effects of etching on the interface between the poly-Si layer and the SiO_2 C/L and is consistent with the damage observed from the SEM images after the 45-s etch (see Fig. 4). Consequently, control over the SiNP etch time is important.

To further investigate the effects of the interface quality of PIN process, we studied on the removal of the two conventionally essential cleaning processes (prior to laser irradiation and prior to deposition of the gate insulator) on the performance of the poly-Si TFTs. Both the poly-Si TFTs crystallized using the PIN and conventional ELA methods exhibited a high μ_{FET} and low V_{th} following the cleaning processes. However, these cleaning processes were more significant on the poly-Si TFT crystallized using the conventional ELA method than on the poly-Si TFT crystallized using the PIN method, as shown in Fig. 6. Differences in μ_{FET} of a factor of 3, and in V_{th} of a factor of 10, were observed in the poly-Si TFTs crystallized using conventional ELA with and without the cleaning process, as shown in
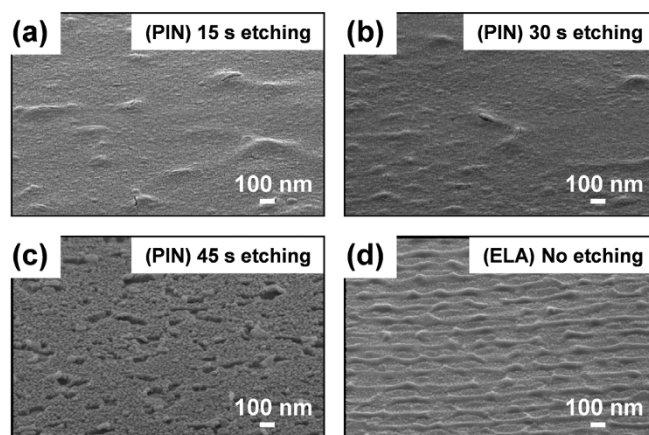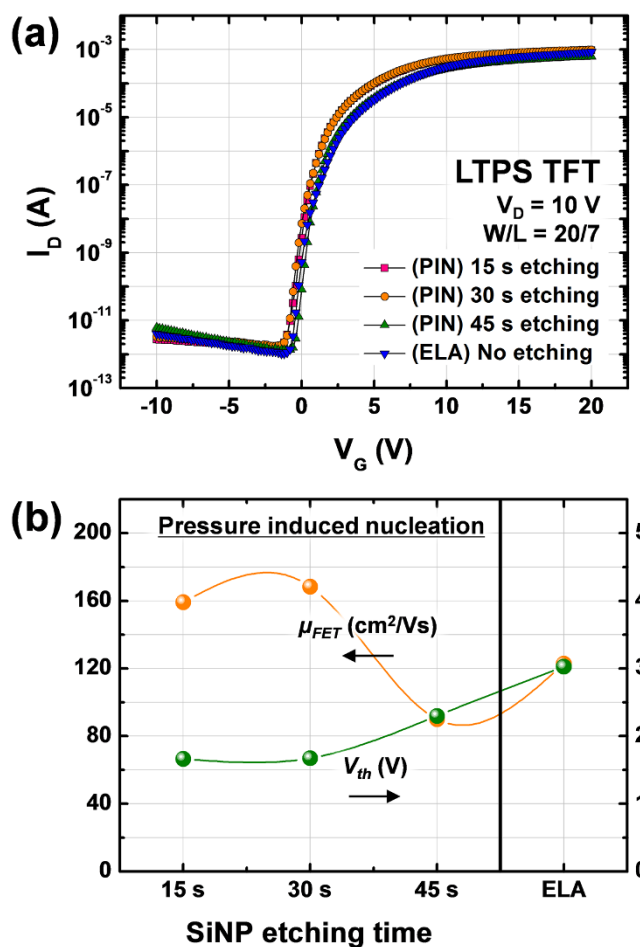

Figure 5 | Electrical properties of poly-Si TFTs. (a), The transfer characteristics of poly-Si TFTs with a 15-nm-thick SiO_2 C/L crystallized at 340 mJ/cm^2 after etching of SiNPs. (b), The variation in μ_{FET} and V_{th} depending on the process conditions.
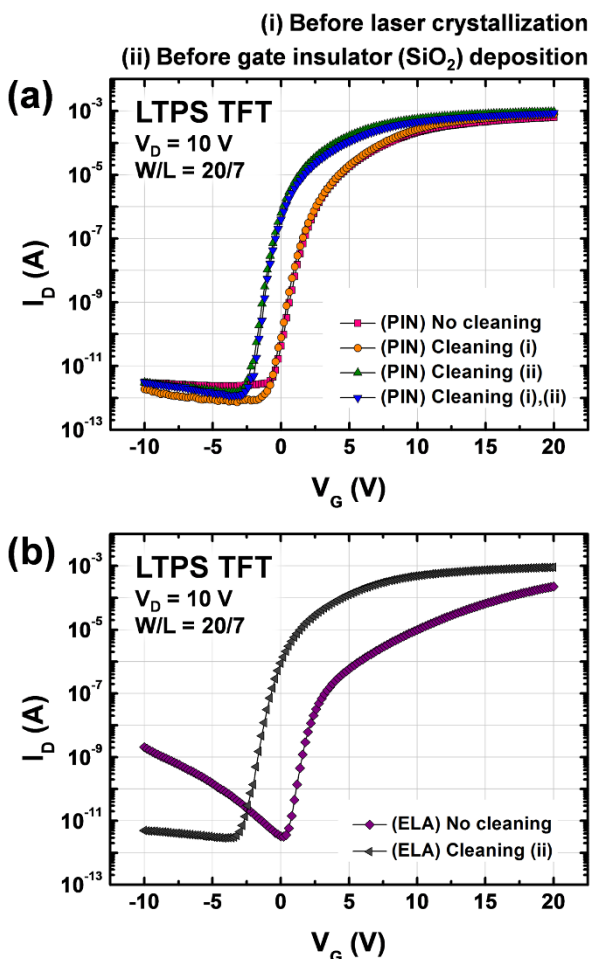
Figure 6 | **Electrical properties of poly-Si TFTs.** Transfer characteristics of poly-Si TFTs with a 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 with different cleaning processes: prior to laser irradiation and the deposition of the gate insulator. (a), PIN and (b), conventional ELA.
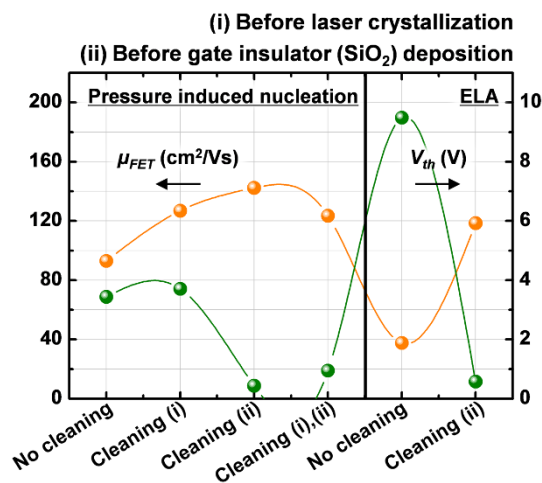

Figure 7 | **Electrical properties of poly-Si TFTs.** The variation in μ_{FET} and V_{th} of the poly-Si TFTs with a 15-nm-thick SiO$_2$ C/L crystallized at 340 mJ/cm^2 depending on the cleaning process employed during fabrication.

achieved using only six laser exposures (compared with 20 for conventional ELA).

Methods

First, a 200-nm-thick SiO$_2$ blocking layer (B/L) was deposited on a 0.7-mm-thick glass substrate using plasma-enhanced chemical vapor deposition (PECVD). The B/L protects the TFT from impurities in the glass during the subsequent processes. A 50-nm-thick a-Si layer was then deposited on the B/L using PECVD, with no break in the vacuum system. Dehydrogenation was carried out at 430°C for 90 minutes to decrease the hydrogen content of the a-Si film, because residual hydrogen may lead to small explosions during the subsequent laser crystallization.

During conventional laser crystallization of an a-Si thin film for LTPS TFT fabrication, an XeCl excimer laser (λ = 308 nm) is used to irradiate an a-Si thin film, which converts it to a poly-Si, and where no other films are deposited on top of the silicon layer. However, in this work, a 15-nm-thick SiO$_2$ C/L was deposited on top of the a-Si thin film prior to irradiation with the excimer laser. Sequential deposition was used to form the B/L to the C/L, with no break in the vacuum system during PECVD, resulting in a clean interface between the poly-Si active layer and the SiO$_2$ gate insulator.

Following laser irradiation, the TFTs were fabricated via a typical LTPS process, including active layer patterning, deposition of a 100-nm-thick SiO$_2$ gate insulator, patterning of the gate electrodes, ion implantation and activation, deposition of an inter-insulating layer, and the deposition and patterning of metal contacts and interconnects. Moreover, cleaning process split tests were carried out during LTPS TFT fabrication: one set of devices underwent a cleaning process prior to laser irradiation and another prior to the deposition of the gate insulator layer. After that, the fabricated LTPS TFT performances were measured using an HP 4156C system.

Fig. 7. This is attributed to the break in the vacuum system for deposition of the gate insulator in the conventional ELA. Without the cleaning process prior to deposition of the gate insulator, impurities remain at the interface between poly-Si and SiO$_2$ gate insulator, which act as trap sites. On the contrary, the PIN process has an advantage because of the interface preservation between poly-Si and SiO$_2$ C/L, which can lead the removal of cleaning process before SiO$_2$ gate insulator deposition needed in the poly-Si TFT crystallized using the conventional ELA method.

We have described a method to improve the performance of LTPS TFTs using PIN. In the PIN process, the regional solidification temperature varies due to variations in the pressure during laser irradiation of the a-Si layer, and the resulting laterally grown poly-Si grains that form are larger than those that form using conventional ELA; a four-fold increase in the grain size was observed compared with conventional ELA using the same laser exposure conditions. SiNPs also formed, and following the etching of these SiNPs, TFTs with favorable performance metrics were fabricated. The improvements in performance are attributed to this increase in the grain size, as well as the preservation of the interface between the poly-Si and the gate insulator, because the SiO$_2$ C/L was deposited on the a-Si with no break in the vacuum system. This interface preservation becomes possible to remove the cleaning process (prior to gate insulator deposition). The TFTs formed using the PIN process exhibited a high field-effect mobility of $\mu_{FET} > 160$ cm^2/Vs, which was

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Acknowledgments

Author contributions

S.J.K. and M.-K.K. contributed equally to this work. S.J.K. and M.-K.K. wrote the main manuscript text and S.J.K. prepared figures 1-7. The project was guided by H.J.K. All authors reviewed the manuscript.

Additional information

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