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Review article

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Industry perspective on power electronics for electric vehicles

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Abstract

Driven by the global effort towards reduction of carbon dioxide emissions from cars, the gradual phase out of fuel cars accompanied by the rise of electric vehicles (EVs) has become a megatrend. Despite the rapid growth of electric vehicle markets worldwide, the leading manufacturers recently announced notable price reductions to compete for market shares. From the technology perspective, for fast charging and extended driving range, more electric vehicles now shift to 800-V batteries with the traction inverters based on wide-bandgap SiC, which can lead to higher efficiency and higher power densities compared with the Si counterparts. However, to further reduce the SiC substrate and epitaxy cost remains a challenge. By contrast, for the DC–DC converters and onboard chargers of electric vehicles, the power switches based on GaN enable fast switching, which can significantly reduce the module form factors. However, the high-voltage reliability concerns associated with the heteroepitaxial defects affect the widespread adoption of GaN in electric vehicles. In this Review, we present a comprehensive discussion of the state-of-the-art power electronics for electric vehicles based on Si, SiC and GaN technologies from the device to circuit and module levels. Various competing technologies are evaluated in consideration of not only efficiency but also cost and reliability, which constitute the three main pillars supporting the continuous growth of electric vehicle power electronics.

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Key points

- By increasing the electric vehicle (EV) battery voltage from 400 V to 800 V, the power densities and efficiencies of the traction drive system, including the motor and inverter, can be enhanced, and the battery charging time can be reduced.
- Under the 800-V battery architecture, the 1,200-V SiC metal oxide semiconductor field-effect transistors are the best options for the traction inverters because of the lower switching loss, smaller form factor, higher thermal conductivity and wider bandgap for high-temperature operations. However, how to further reduce the SiC substrate and epitaxy cost remains a challenge.
- For DC–DC converters and onboard chargers to achieve high-power densities, the switching frequency needs to be sufficiently high for reducing the capacitor and transformer sizes. In this regard, the GaN high electron mobility transistors with low $R_{on}×Q_g$ will be the best options. However, how to further improve the reliability by reducing the heteroepitaxial defects is critical for the widespread adoption in EVs.
- For the EV power modules with high-power densities, the power cycling reliability relies on layout designs with low parasitics and building materials with high thermal conductivities and well-matched thermal expansions. After all, efficiency, cost and reliability are the three main pillars of EV power electronics.

Introduction

Currently, vehicle electrification is revolutionizing the automotive industry. To reduce carbon dioxide emissions from cars, governments have adopted policies, aiming at zero-emission sales globally by 2040 and, in some leading markets, by 2035. To this end, the emergence of electric vehicles (EVs), which generally include battery EVs and plug-in hybrid EVs, has become a megatrend. According to the International Energy Agency and the EV Volumes, the global EV sales exceeded 14 million in 2023, with China accounting for more than 8 million[1,2] (Fig. 1a). Although the global EV penetration rate was only 15.8% in 2023, it is expected to grow to about 20% in 2024 (ref. 2). At present, the power electronics constitutes about US$1,400 per EV. According to the Yole Intelligence, the global market for power electronics in EVs is expected to reach US$29 billion by 2028 (ref. 3).

Recently, both Tesla and BYD announced price cuts in a bid to expand the market shares of their EVs. Tesla reduced the prices of its Model 3 and Model Y in major markets including Europe, USA and China. Similarly, BYD, a prominent Chinese automaker, announced price reductions for its Dynasty models and Ocean series. The keen competition for market share among leading EV companies makes EVs much more affordable than before, with the prices of some cheapest models even lower than the fuel counterparts. To lower the sale price without compromising the performance, innovations in batteries and powertrains become critical. In 2018, Tesla first used SiC metal oxide semiconductor field-effect transistors (SiC MOSFETs) in the traction inverters of its Model 3, which can yield higher power densities and higher efficiencies than those based on conventional Si insulated-gate bipolar transistors (Si IGBTs). However, mainly owing to the limited availability of high-quality SiC wafers, the prices of SiC MOSFETs remain high compared with Si IGBTs. To this end, by extracting heat from the power modules more efficiently, Tesla optimized their powertrain system to achieve the same power with less SiC material used, indicating that thermal management is another key to obtain a well balance among efficiency, cost and reliability.

Other concerns for EV adoption are the short driving range and long charging time. In 2022, the average driving range of an EV was 337 km (ref. 4). Despite a big leap from 230 km since 2018, it is still not sufficient to resolve the 'range anxiety' of customers. Increasing the battery voltage from 400 V to 800 V cuts the required current by half to deliver the same power, resulting in thinner copper wires and smaller electronic components in the power modules, which can save space and extend the driving range. Most importantly, the 800-V EVs can be charged at ≥250 kW, reducing the charging time to less than 30 min. The adoption of an 800-V battery requires the power switches in the traction inverter to be able to withstand high drain voltages up to 1,200 V when the power switch turns off, for which the SiC MOSFETs are the most promising technology. Compared with the conventional Si IGBTs, SiC MOSFETs have lower switching loss, faster switching speed and smaller device footprint. Although GaN high electron mobility transistors (GaN HEMTs) can switch at even higher frequencies, their reliability under off-state high drain bias condition remains a concern.

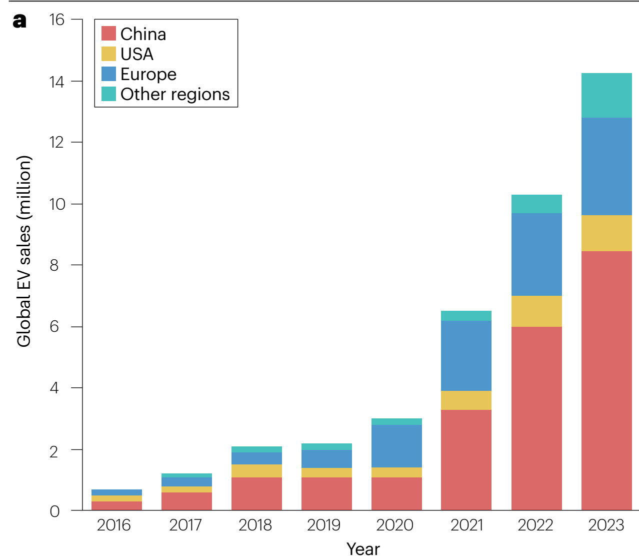
In the power electronics system of an EV (Fig. 1b), the 800-V battery as the source of traction power can be charged directly by the fast-charging station or through the onboard charger (OBC), which converts the AC electricity of the grid to 800-V DC. The charging and discharging processes are monitored and regulated by the battery management system (BMS). Then the traction inverter converts the 800-V DC voltage of the battery into three-phase pulse width modulation (PWM) signals, which drive the motor to create the specific torque and speed. The six power switches consisting of SiC MOSFETs inside the traction inverter are controlled by the microcontroller unit. The low-voltage battery, which provides the DC electricity needed by the onboard accessories, is charged by the DC–DC converter. Because the negative terminal of the low-voltage battery is connected to the chassis of the EV, the DC–DC converter also provides galvanic isolation. For the OBC and DC–DC converter to achieve high-power densities, the switching frequencies need to be sufficiently high to reduce the capacitor and transformer form factors. To this end, GaN HEMTs with small gate capacitances are the most promising technology.

In this Review, we present a comprehensive discussion of the state-of-the-art power electronics for EVs based on Si, SiC and GaN technologies from the device to circuit and module levels. The various device structures of Si IGBTs, SiC MOSFETs and GaN HEMTs, which affect their blocking voltage rating and current rating, switching performance, cost and reliability, are discussed and compared. Then, the circuit topologies of 800-V traction inverters, OBCs and DC–DC converters with superior power densities and efficiencies are shown. Moreover, recent developments in EV power modules, with the goals of integrating complementary functionalities, lowering stray inductance, extracting heat efficiently and ensuring power cycling reliability, are elaborated. Finally, the remaining challenges and opportunities of SiC and GaN technologies, which are critical for the further development of EV power electronics, are pointed out.

Power devices for EVs

Si IGBTs

Since the invention by Baliga at General Electric in 1979 (ref. 5), Si IGBTs have undergone continuous improvements to remain the most widely used power switches in the powertrains of EVs. Si IGBTs adopt



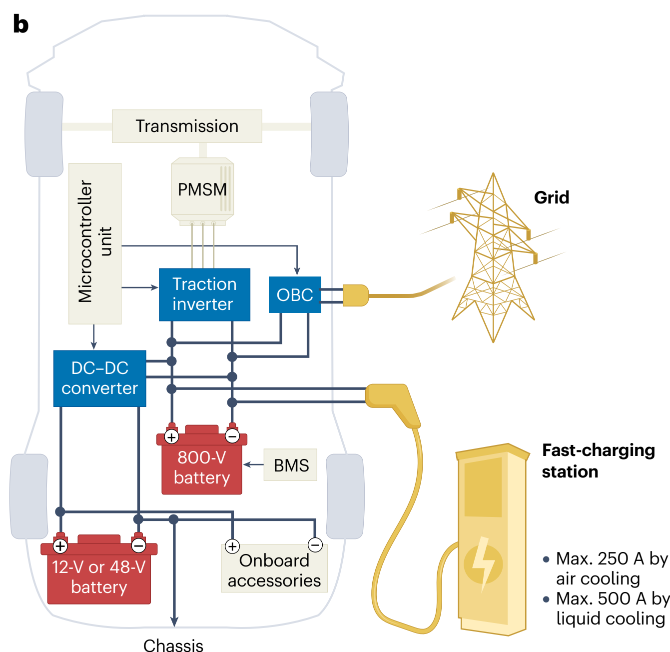


Fig. 1 | Electric vehicle market and power electronics system of electric vehicles. a, Global electric vehicle (EV) sales from 2016 to 2023 (ref. 1). **b**, Illustration of the power electronics system in an EV, including the high-voltage battery for providing the traction power and the low-voltage battery for providing the DC electricity needed by the onboard accessories. The 800-V battery can be charged by either the fast charging station or the onboard charger (OBC). The traction inverter converts the 800-V DC link voltage into three-phase pulse width modulation signals for driving the motor, such as the permanent magnet synchronous motor (PMSM). The DC–DC converter charges the low-voltage battery, while providing galvanic isolation. The output power range and the state-of-the-art power density of the traction inverters are 100–400 kW and >40 kW l^{-1}, DC–DC converters 1–7 kW and >5 kW l^{-1} and OBCs 11–22 kW and >3 kW l^{-1}, respectively. BMS, battery management system.

a conventional vertical double-diffused metal-oxide semiconductor (VDMOS) structure, with a collector terminal at the bottom and the gate and emitter terminals on the top (Fig. 2a). When the voltage difference between the gate and emitter (V_{GE}) is smaller than the threshold voltage (V_{th}), the Si IGBT is turned off and the large voltage difference between the collector and emitter (V_{CE}) drops across the depletion region in the n$^-$ drift layer. Therefore, the n$^-$ drift layer needs to be sufficiently thick, so that the peak electric field does not exceed the breakdown electric field of Si (0.3 MV cm^{-1}). A typical n$^-$ drift layer thickness for the IGBT blocking voltage rating of 1,200 V is about 100 µm. By contrast, with a positive gate voltage for $V_{GE} > V_{th}$, an inversion layer of electrons, which constitutes the n-channel, is formed underneath the gate oxide. When $V_{CE} > 0$ V, electrons flow from the n$^+$ emitter through the n-channel to the n$^-$ drift layer, whereas holes are injected from the p$^+$ substrate to the n$^-$ drift layer, making the n$^-$ drift layer flooded with bipolar charge carriers flowing in opposite directions. Consequently, the Si IGBT starts to conduct the collector current (I_C). With the bipolar conduction and a large device area, the Si IGBTs can achieve high current ratings (Fig. 3a), despite the relatively thick n$^-$ drift layer.

Relative to the planar gate structure, the trench gate structure exhibits superior properties characterized by about 20% lower collector–emitter saturation voltage ($V_{CE,sat}$), which is the collector-to-emitter voltage drop at the rated I_C (ref. 6) (Fig. 2b). The smaller $V_{CE,sat}$ means the less power dissipation ($V_{CE,sat} \times I_C$) of the Si IGBT during the conduction time. However, one major issue of the trench gate IGBTs is the high collector saturation current ($I_{C,sat}$) and the poor short circuit ruggedness, which can be resolved by adopting well-designed cell geometry and optimizing the carrier concentration profile[7]. The micro-pattern trench technology introduced by Infineon can further increase the IGBT channel width by using narrow parallel trenches separated by sub-micron mesas, leading to the further reduction of $V_{CE,sat}$ (refs. 8,9). Another example, by introducing an n-type hole-barrier layer around the p-well, the planar gate IGBT keeps more holes in the n$^-$ drift layer, leading to higher conductivity and lower $V_{CE,sat}$ (ref. 10). However, if the doping concentration of the hole-barrier layer is too high, the voltage blocking capability of the device may become compromised.

Growing an n$^+$ homoepitaxial layer, also known as the punch-through (PT) layer, on a thick p$^+$ substrate has been a potent solution for controlling the electric field distribution in the n$^-$ drift layer of an Si IGBT. When the device is turned off, the n$^-$ drift layer is fully depleted of charge carriers, and the depletion region permeates into the PT layer but does not completely penetrate through to the p$^+$ substrate. Similar concept has also been applied for the n-type field-stop (FS) layer of the trench gate IGBT[11]. Either PT or FS layers are designed to improve voltage-blocking capability for high-voltage power switching, such as in EV traction inverters, while keeping the n$^-$ drift layer thin and therefore the $V_{CE,sat}$ low. At the same time, having an n$^+$ layer on the p$^+$ substrate can hinder the injection of excess holes into the n$^-$ drift layer. As a result, fewer holes need to be removed in the n$^-$ drift layer during the turn-off transient, leading to a smaller tail current and a lower switching loss. It is worth noting that the non-punch-through (NPT) structures, consisting of a high purity float-zone substrate as the n$^-$ drift layer with the p-type collector grown on the backside, have also found wide applications[12]. Having a lightly doped collector to keep the hole injection low and a long carrier lifetime in the float-zone substrate, the NPT Si IGBTs can offer the advantage of fast switching, without the expense of reduced voltage blocking capability. Furthermore, the NPT IGBT has a positive temperature coefficient, making it more suitable for device parallelization which is desirable in the EV traction inverter.

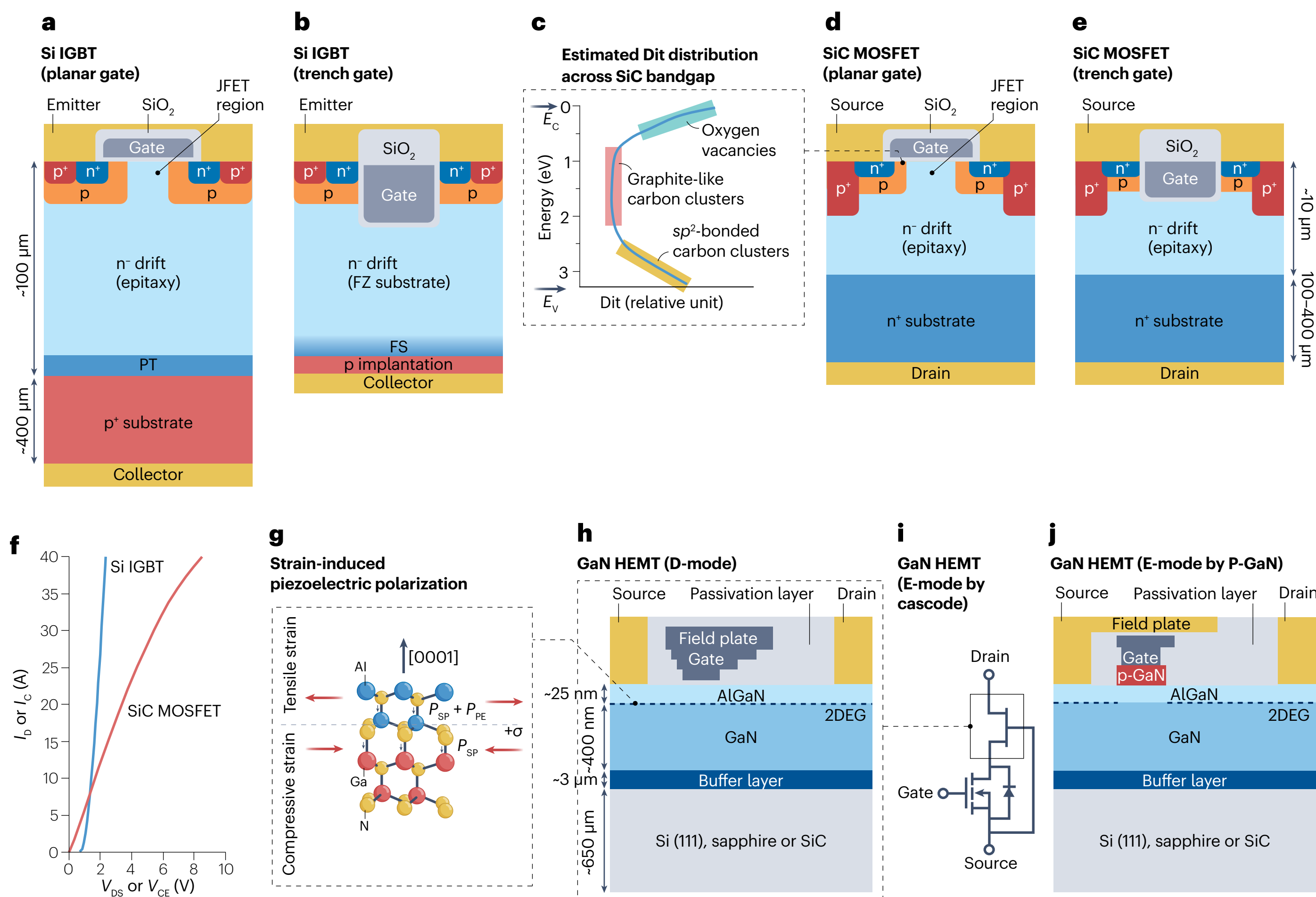


Fig. 2 | Power devices for electric vehicles. a,b, Cross-sections of Si insulated-gate bipolar transistors (IGBTs) with planar gate (**a**) and trench gate (**b**). **c**, Estimated density of interface traps (Dit) of charge carriers across the SiC energy bandgap. **d,e**, Cross-sections of SiC metal oxide semiconductor field-effect transistors (MOSFETs) with planar gate (**d**) and trench gate (**e**). **f**, I_D–V_{DS} curve of an Infineon trench gate SiC MOSFET (blocking voltage = 650 V, current rating = 31 A) and the I_C–V_{CE} curve of an Infineon trench gate Si IGBT (blocking voltage = 650 V, current rating = 34 A). **g**, Spontaneous polarization (P_{SP}) and strain-induced piezoelectric polarization (P_{PE}) at the AlGaN/GaN interface, resulting in the formation of 2D electron gas. **h**, Cross-section of a D-mode GaN high electron mobility transistor (HEMT) with a gate-connected field plate design for $V_{GS} = 0\ V > V_{th}$. **i**, Cascode configuration composed of a high-voltage D-mode GaN HEMT in series with a low-voltage Si MOSFET. **j**, Cross-section of an E-mode GaN HEMT with a p-type GaN gate and a source-connected field plate design for $V_{GS} = 0\ V < V_{th}$. Here, the thicknesses of the epitaxial layers of the Si IGBTs and SiC MOSFETs are estimated based on the blocking voltage rating of 1,200 V. FS, field-stop; FZ, float-zone; JFET, junction field-effect transistor; PT, punch-through.

For Si IGBTs, a trade-off exists between $V_{CE,sat}$ and turn-off switching loss, which is the energy loss occurring during the turn-off transient (Fig. 3a, inset). Although more holes in the n⁻ drift layer contribute to higher conductivity and lower $V_{CE,sat}$, it also entails a larger tail current and, therefore, a higher switching loss during the turn-off transient. The trade-off can be minimized through various PT or FS technologies, such as the thin PT by Toshiba[13], soft PT by ABB[14,15] and light PT by Mitsubishi[16]. Moreover, in addition to the efforts towards continuous lowering of conduction loss and switching loss, monolithically integrating the IGBTs with antiparallel diodes for reverse conducting (RC) is another emerging field of research[17,18], especially for the applications in EV traction inverters. For examples, Infineon's RC-DA IGBT 5, the X-series RC IGBT of Fuji Electric and the 2nd Gen RC IGBT of Mitsubishi Electric have incorporated the antiparallel freewheeling diodes (FWDs) on the same substrate.

SiC MOSFETs

SiC power devices are promising for high-power density and high efficiency applications, as revealed in 1989 by the figure of merit of Baliga[19]. However, the progress was limited by the SiC crystal growth, epitaxy and processing techniques until 2001 when the first commercial SiC Schottky diode was released by Infineon. For the SiC MOSFETs, additional issues related to the gate oxide impeded its development, because the high density of interface traps (Dit) of charge carriers between the SiC and SiO_2 lowers the electron mobility and causes threshold voltage instabilities. In 1997, Li et al.[20] found that post-oxidation annealing in nitric oxide, the so-called nitridation, could reduce Dit to the level of $10^{10}\ eV^{-1}\ cm^{-2}$. Thereafter, continuously improving the channel mobility and gate oxide reliability has been a core research area in the SiC community. Meanwhile, remarkable improvements in the

wafer scale crystal growth have led to 150 mm, and most recently to 200 mm, SiC wafers with virtually no defects. In 2018, the 650-V SiC MOSFETs from STMicroelectronics were used in the traction inverters of Tesla Model 3, which revolutionized the EV power electronics and generated tremendous interest in SiC. Compared with the Si IGBTs, the SiC MOSFETs also adopt the VDMOS structure, but need only about

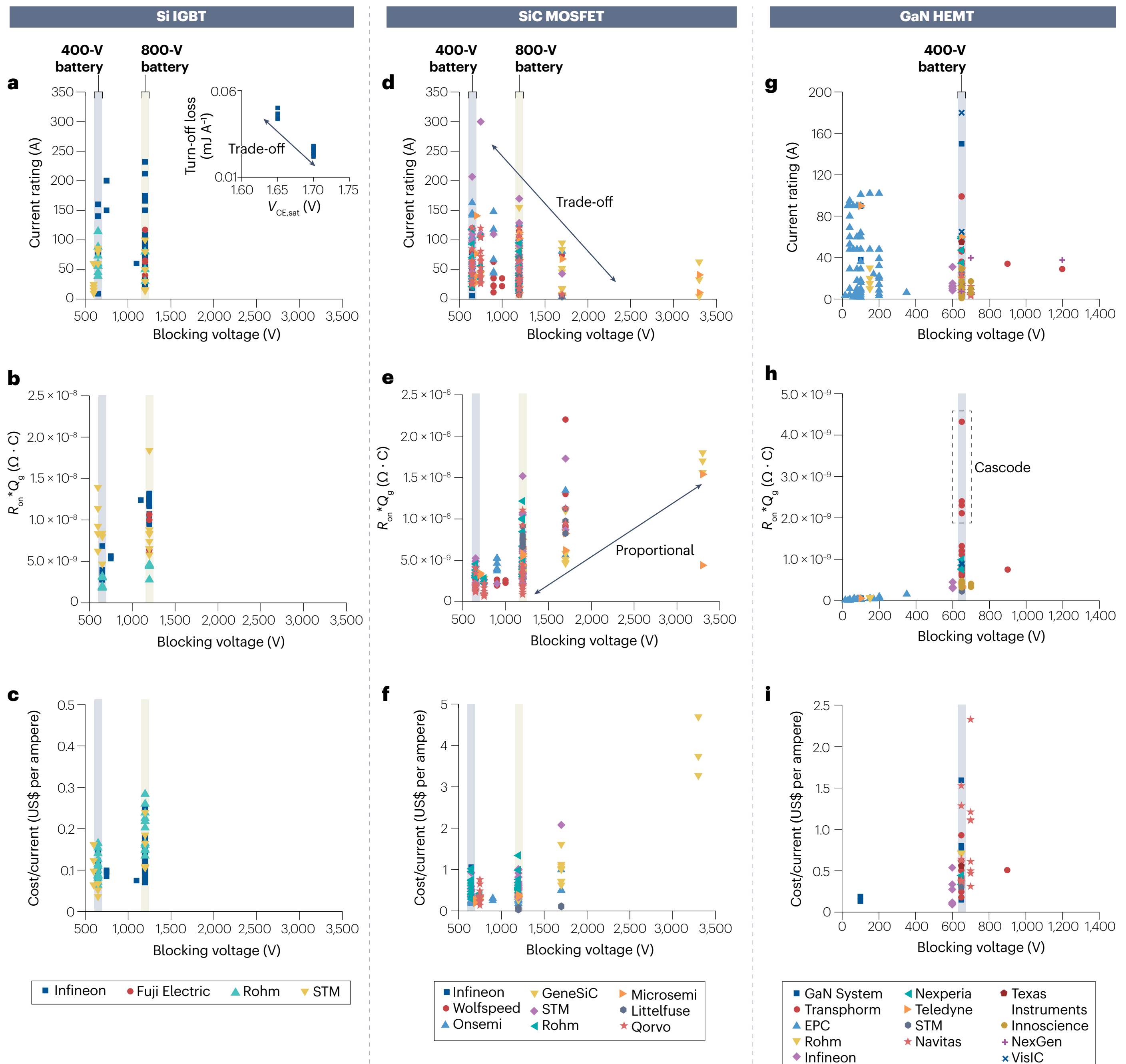


Fig. 3 | Performance and cost comparisons for electric vehicle power devices. a–c, Current rating (**a**), $R_{on} \times Q_g$ (**b**) and cost per current (**c**) versus blocking voltage rating for the Si insulated-gate bipolar transistors (IGBTs) from different companies. Here, the R_{on} of Si IGBTs is calculated as $V_{CE,sat}$ divided by the current at which $V_{CE,sat}$ is obtained. The inset in **a** shows the turn-off switching loss versus $V_{CE,sat}$ for the Infineon MPT Si IGBTs. **d–f**, Current rating (**d**), $R_{on} \times Q_g$ (**e**) and cost per current (**f**) versus blocking voltage rating for the SiC metal oxide semiconductor field-effect transistors (MOSFETs) from different companies. **g–i**, Current rating (**g**), $R_{on} \times Q_g$ (**h**) and cost per current (**i**) versus blocking voltage rating for the GaN high electron mobility transistors (HEMTs) from different companies. Particularly, for the cascode-based E-mode GaN HEMTs from Transphorm, as highlighted by the grey dashed circle in **h**, the R_{on} is larger owing to two devices in series, leading to the larger $R_{on} \times Q_g$ ratings. Note that the cost per current is defined as the discrete cost divided by the discrete current rating. The 650-V and 1,200-V blocking voltage ratings are intended for the 400-V and 800-V battery systems, respectively.

10-μm thick n^- drift layers with the doping concentration about 10^{16} cm^{-3} to achieve the blocking voltage rating of 1,200 V (Fig. 2d). Owing to the high breakdown electric field of SiC (2.5 MV cm^{-1}), the SiC MOSFETs can withstand off-state high drain bias with relatively thin depletion layers. Also because of the thin n^- drift layers, the SiC MOSFETs can achieve low on-resistance (R_{on}) by virtue of unipolar conduction, which is beneficial for fast switching. By contrast, Si IGBTs with about 100-μm thick n^- drift layers need bipolar conduction to achieve low R_{on}, which inevitably lead to high turn-off switching loss owing to the tail current. Another significant advantage of the SiC MOSFETs is the high thermal conductivity of SiC (300–400 W m^{-1} K^{-1}), which is close to that of copper (380–400 W m^{-1} K^{-1}). This property makes the extraction of heat from the power devices more efficient. Therefore, the SiC MOSFETs exhibit a greatly reduced switching loss relative to Si IGBTs, while offering similar blocking voltage ratings and lower R_{on} in smaller form factors.

Despite the superior performance, the fabrication of SiC MOSFETs is much more challenging than the Si IGBTs. First, the SiC boule is synthesized by the physical vapour transport method at >2,100 °C, with the growth rate only about 2 cm per week. Among more than 200 polytypes, 4H-SiC is the commonly used crystal structure for fabricating SiC MOSFETs. By contrast, the Si ingot can be produced by more efficient melt growth methods, such as the Czochralski process at >1,400 °C, with the growth rate about 2 m per 2–3 days. Furthermore, compared with Mohs hardness scale of diamond of 10, the Mohs hardness scale of SiC is 9, which complicates the wafering process, such as slicing, lapping, grinding and chemical mechanical polishing. Besides, the SiC substrates tend to have higher densities of crystallographic defects, especially those detrimental for device performance, such as triangle carrots, micropipes and basal plan dislocations. Therefore, multimodal, non-destructive and in-line production compatible inspection techniques are necessary for identifying those detrimental surface/subsurface defects and improving the device production yield. For example, the KLA Candela and Lasertec SICA88, which mainly use optical and photoluminescence inspections, are the widely used equipment models for this purpose. Finally, the device fabrication on SiC substrates is much more complex than that on Si. Given that thermal diffusion in SiC is negligible, the doping has to be done by 'hot' (>550 °C) ion implantation, followed by high-temperature (>1,600 °C) activation annealing, during which a temperature-resistant carbon cap is needed to avoid silicon desorption. Another critical step in the SiC MOSFET fabrication is the nitridation process for Dit reduction and channel mobility enhancement. Overall, the high cost of SiC wafers remains the most critical issue faced by the SiC industry, with the substrate and epitaxy costs constituting more than a half of the average die cost[21]. Therefore, to ensure stable supply of SiC wafers at competitive price, the leading integrated device manufacturers of SiC MOSFETs, such as Infineon, Wolfspeed, STMicroelectronics, Rohm and Onsemi, have either opted for its own wafer production or formed partnerships (even double sourcing) with SiC wafer suppliers, such as Wolfspeed, Coherent, SiCrystal, SK Siltron, GT Advanced, Soitec, Sanan IC, Tankeblue and SiCC.

For SiC MOSFETs with a blocking voltage rating of 1,200 V, the channel resistance constitutes about 50% of total R_{on} (ref. 22). For lower blocking voltage ratings, the channel resistance constitutes an even bigger portion of total R_{on}. For example, about 85% of total R_{on} comes from channel for 650-V SiC MOSFETs. The electron mobility in the channel is mainly affected by the interfacial traps, originating from carbon clusters and oxygen vacancies at the SiC/SiO_2 interface (Fig. 2c) formed during the thermal oxide growth[23,24]. In addition to the post-oxidation nitric oxide (NO or N_2O) annealing commonly used in the SiC industry[25], using pre-oxidation H_2 etching to remove carbon clusters and SiO_2 deposition without oxidation of SiC can reduce Dit to 3×10^{10} cm^{-2} eV^{-1} and increase the electron mobility to >80 cm^2 V^{-1} s^{-1} (refs. 26,27). Apart from the channel mobility optimization, other methods aimed at lowering R_{on} have been demonstrated. For example, doping at the junction field-effect transistor (JFET) region[28], adding a current spreading layer through implantation[29] and self-aligned channel and source contact[30] have been achieved. Led by Infineon and Rohm, the trench gate SiC MOSFETs have shown great potential in reducing R_{on}. Compared with the planar gate, the trench gate structure with a vertically aligned channel can reduce the cell pitch from 6 μm to 3 μm (Fig. 2e). Furthermore, the adverse JFET effect, which limits the current flowing between the p-wells, of the planar gate SiC MOSFETs is eliminated, and the mobility in the trench gate channel on the (11–20) plane is about five times higher than that in the planar gate channel on the (0001) plane. Therefore, the trench gate SiC MOSFETs can usually achieve low $R_{on,sp}$ (<3 mΩ cm^2)[31,32]. Despite improved performance, the gate oxide layer at the bottom corners of the trench gate is directly exposed to high electric field owing to the off-state high drain bias. By contrast, the gate oxide under the planar gate is well protected by the depletion layer at the JFET region. To prevent early breakdown, the bottom corners of the trench gate are made into a round shape and the gate oxide thickness is larger at the bottom and thinner at the sidewall[33]. Therefore, the fabrication of trench gates requires an exquisite combination of reactive ion etching and oxide formation.

Commercial SiC MOSFETs have the blocking voltage ratings ranging from 650 V to 3,300 V (Fig. 3d), among which the 650-V and 1,200-V SiC MOSFETs are mainly intended for the traction inverter applications in the 400-V and 800-V battery EVs, respectively. Meanwhile, the current ratings range mostly between 10 A and 200 A. There is a trade-off between the blocking voltage rating and current rating (Fig. 3d). When the blocking voltage rating increases, which requires a thicker drift layer and inevitably leads to a larger R_{on}, the current rating has to decrease to keep the on-state heat generation ($I_D^2 \times R_{on}$) almost unchanged. $R_{on} \times Q_g$, in which Q_g is the amount of gate charge needed to turn the device on and off, is often used as a parameter to evaluate the switching capability. If the R_{on} is reduced owing to a larger device area, Q_g will also increase. When the blocking voltage rating increases, the drift layer thickness and R_{on} increase, leading to larger $R_{on} \times Q_g$ (as indicated by the proportional line in Fig. 3e). With respect to $R_{on} \times Q_g$ of 1,200-V Si IGBTs (Fig. 3b), the 1,200-V SiC MOSFETs have a slightly lower $R_{on} \times Q_g$, indicating that the SiC MOSFETs are more suitable for fast switching applications than the Si IGBTs. However, owing to the high cost of SiC substrate and epitaxy, the cost per current of SiC MOSFETs (Fig. 3f) is much higher than that of Si IGBTs (Fig. 3c). Next, we compare the I_D–V_{DS} curves of a trench gate SiC MOSFET and a trench gate Si IGBT (Fig. 2f), both of which have similar blocking voltage and current ratings. When the output current is below 10 A, the SiC MOSFET exhibits a linear I_D–V_{DS} relationship, with the R_{on} about 150 mΩ. However, the R_{on} gradually increases as the I_D increases, when the device gradually enters into the saturation region. By contrast, the Si IGBT has a diode-like turn-on behaviour owing to the built-in potential between the p-type collector and the n^- drift layer. However, once turning on, with the help of bipolar conduction, the R_{on} of the Si IGBT gradually decreases as the I_C increases. For the Si IGBT curve in Fig. 2f, the R_{on} reaches 140 mΩ at 10 A and drops to 88 mΩ at 20 A.

During the power switching operation, SiC MOSFETs need to withstand high drain voltage when the device is turned off. The off-state high

drain bias reliability can be enhanced by using sufficiently thick drift layers (typically 5.5 μm for 650-V and 10 μm for 1,200-V blocking voltage rating) and properly designed guard rings. This reliability metric can be evaluated by a high-temperature reverse bias (HTRB) test[34,35]. By contrast, to fully turn on SiC MOSFETs for low R_{on} and to ensure operation in the positive temperature coefficient condition, that is, larger R_{on} with higher junction temperature (T_j), for the safety of parallelization, the recommended on-state gate bias is 15–20 V. Given the typical gate oxide thickness of SiC MOSFETs is only 40–50 nm for the planar gate and about 80 nm for the trench gate, the electric field across the gate oxide layer is strong. The gate oxide reliability is mainly affected by the extrinsic defects in the gate oxide layer owing to epitaxy defects or impurities in the oxide layer. The devices with extrinsic gate oxide defects must be detected during the burn-in screen test. Meanwhile, the intrinsic strength of gate oxide can be enhanced by lowering the Dit at the SiO_2/SiC interface and by increasing the oxide thickness[36]. The gate oxide reliability can be evaluated by the high-temperature gate bias (HTGB) test and the time-dependent dielectric breakdown (TDDB) test[37], whereas the V_{th} drift owing to charge trapping in the oxide layer can be probed by the bias temperature instability (BTI) test[38].

GaN HEMTs

The concept of using a heterojunction to enhance the electron mobility in a transistor was first proposed by Mimura et al. in 1979 (ref. 39). GaN HEMT was first developed in 1993 and commercialized by Eudyna Device in 2006 (ref. 40). Unlike the VDMOS structures adopted by the Si IGBTs and SiC MOSFETs, GaN HEMTs feature a lateral device structure, with top drain, source and gate terminals (Fig. 2h). Wurtzite GaN has a hexagonal crystal structure, which exhibits spontaneous polarization owing to different electro-negativities of Ga and N atoms[41]. When a AlGaN layer is heteroepitaxially grown on a GaN layer, the lattice mismatch between the two materials results in piezoelectric polarization (Fig. 2g), which induces a 2D electron gas (2DEG) at the interface even at zero gate bias[42]. Therefore, GaN HEMT is normally on, so that a negative threshold voltage is required to pinch off the channel, the condition known as the depletion mode (D-mode). When $V_{GS} > V_{th}$ and $V_{DS} > 0$ V, GaN HEMT is on and the electrons in the 2DEG move with a mobility up to 2,200 $cm^2 V^{-1} s^{-1}$. Considering that current is proportional to the product of the charge carrier density and mobility, although the electron density is limited in the 2DEG, a high current can still be achieved owing to the high electron mobility. When $V_{GS} < V_{th} < 0$ V, the GaN HEMT turns off and the discontinued 2DEG is sandwiched between the GaN and AlGaN layers with large bandgaps of 3.4 eV and 4.3 eV, respectively.

However, in the lateral device structure, exceedingly strong electric field may appear at the drain side, bottom corner of the gate. Therefore, gate or source field-plate designs are generally necessary to evenly distribute the electric field[43]. Furthermore, as the whole device is built upon heteroepitaxial layers, the crystal defects, such as threading dislocations, may cause breakdown under high drain bias[44,45]. Overall, compared with Si IGBTs and SiC MOSFETs, which are vertical and built upon homoepitaxial layers, the GaN HEMTs have lower blocking voltage ratings, mostly below 700 V (Fig. 3g). Therefore, it is the quality of the epitaxial layers, including the buffer, GaN and AlGaN layers, that determines the GaN HEMT performance and reliability, particularly the blocking voltage ratings[46,47]. It is worth noting that the GaN power devices using vertical structures, such as current aperture vertical electron transistors, FinFETs and VDMOSFETs, have shown higher blocking voltages and higher power densities compared with the conventional GaN HEMTs[48]. Nevertheless, owing to the small gate capacitances, the GaN HEMTs (Fig. 3h) have much lower $R_{on} \times Q_g$ ratings than SiC MOSFETs (Fig. 3e) and Si IGBTs (Fig. 3b), making them well suited for fast switching applications, such as DC–DC converters and OBCs in EVs.

The normally on D-mode GaN HEMT requires a specially designed gate driver to provide a negative gate bias to remain in the off state, which inevitably increases power consumption. Furthermore, once the gate driver fails and the device is continuously on, serious reliability issues may occur in the power electronics system. Therefore, GaN HEMTs with a normally off characteristic ($V_{th} > 0$ V), called the enhancement mode (E-mode), are preferred. Several approaches have been proposed to realize E-mode GaN HEMTs[49]. Among them, the cascode configuration, which consists of a high-voltage D-mode GaN HEMT in series with a low-voltage Si MOSFET, is an cost-effective approach used by companies, such as Transphorm and Nexperia[50] (Fig. 2i). When the Si MOSFET is on, the V_{GS} of the D-mode GaN HEMT ($V_{GS,GaN}$) is slightly below zero, the D-mode GaN HEMT turns on simultaneously. When the Si MOSFET is in off state, the $V_{GS,GaN}$ becomes very negative, turning the D-mode GaN HEMT off to withstand the high drain bias. The major concern for the cascode configuration is the additional parasitic inductance resulting from the wire bonding between the Si MOSFET and D-mode GaN HEMT[51]. Furthermore, the R_{on} of the two devices in series is higher than that of a single device, as manifested by the larger $R_{on} \times Q_g$ ratings of the 650-V Transphorm GaN HEMTs (Fig. 3h). Another way of achieving E-mode HEMTs is via a p-type GaN gate (Fig. 2j), which can be formed by heteroepitaxy followed by etching or selective re-growth. The companies that use p-GaN gate HEMTs are GaN Systems and efficient power conversion (EPC). In a HEMT with a p-type GaN gate on an AlGaN layer, 2DEG under the gate region is depleted by the p-GaN/AlGaN/GaN p–i–n-like structure, resulting in normally off property[52]. Therefore, a positive V_{GS} is needed to restore the 2DEG under the gate region. The typical V_{th} for commercial p-GaN gate HEMTs is 1–2 V. By optimizing Mg doping in the p-GaN gate and AlN barrier design, the V_{th} can be further increased to above 2 V for avoiding false turn-on. The p-GaN gate HEMTs suffer from a high gate leakage current[53], which limits their blocking voltage ratings and leads to low TDDB reliability.

For the sake of cost–effectiveness, heteroepitaxy on foreign substrates, such as Si (111), sapphire and SiC, is often used. Particularly, GaN-on-Si is currently the most popular technology for fabricating GaN HEMTs[54]. IQE and EpiGaN are the leading GaN-on-Si epiwafer manufacturers, whereas TSMC provides the most reliable GaN-on-Si foundry service. However, the lattice constant mismatch and the different coefficients of thermal expansion between the epitaxial layers and foreign substrate lead to warpage, cracks and defects, which limit the production yield and reliability. The major reliability issues for GaN HEMTs include dynamic R_{on} degradation owing to the high off-state drain bias and the V_{th} shift under positive or negative gate bias. Both issues are closely related to charge trapping near the interfaces between the passivation dielectric and the AlGaN layer and between other epitaxial layers. To ensure high reliability of GaN HEMTs in practical converter applications, research has been focused on improving R_{on} and V_{th} stabilities under high drain bias and hard-switching conditions. It is worth noting that growing GaN epitaxial layers on the sapphire and SiC substrates for smaller lattice mismatch has become a popular trend, as the cost of both substrates has been greatly reduced owing to the fast-growing LED and EV industries. The SiC substrates can also provide better thermal conductivity, whereas the low thermal

conductivity (26 W m^{-1} K^{-1}) issue of sapphire can be resolved by thinning the substrate thickness through backside grinding. Finally, even with the GaN-on-Si technology, the cost per current of 650-V GaN HEMTs (Fig. 3i) is still comparable with that of 650-V SiC MOSFETs (Fig. 3f) and much higher than that of 650-V Si IGBTs (Fig. 3c). However, considerable cost reduction is expected in the following years as the production and quality of epiwafers continue to progress.

Circuit topologies for power conversions

Traction inverters

Traction inverters and motors are at the heart of the EV powertrain, for producing the specific torque and speed according to the demand of the driver (Fig. 1b). A traction inverter converts the DC voltage of the battery into three PWM signals, which are then applied to the stators of the motor to form three alternating sinusoidal current

Glossary

2D electron gas
(2DEG). In GaN high electron mobility transistors, 2DEG is formed at the interface between the AlGaN and GaN layers, as a result of the lattice mismatch-induced piezoelectric polarization. The 2DEG, connecting the drain and source terminals, constitutes the channel of a normally on D-mode GaN high electron mobility transistor, which can be pinched off by applying a negative threshold voltage at the gate.

Bias temperature instability
(BTI) BTI is a general reliability issue affecting Si, SiC and GaN-based devices. BTI refers to the degradation of threshold voltage over time owing to the application of gate bias at an elevated temperature.

Blocking voltage rating
When a power switch is off, the maximum continuous voltage drop across the power switch that the power switch does not breakdown is blocking voltage rating. For SiC metal oxide semiconductor field-effect transistors and Si insulated-gate bipolar transistors, the breakdown usually happens as avalanche breakdown in the n^- drift layer.

Conduction loss
When a power switch is on, the square of the conducting current multiplied by the on-resistance ($I_D^2 \times R_{on}$) is the conduction loss.

Current rating
When a power switch is on, the maximum continuous current flowing through the power switch that the junction temperature of the power switch remains below its maximum rating ($T_{j,max}$) is current rating. When measuring the current rating, the case temperature (T_c) or heatsink temperature ($T_{heatsink}$) is held at a specific level.

Density of interface traps
(Dit). Dit is the density of interfacial traps originating from carbon clusters and oxygen vacancies at the SiC/SiO2 interface. Dit, which is formed during the thermal oxide growth on the SiC surface, can lower the electron mobility and cause threshold voltage instabilities. Therefore, post-oxidation annealing in nitric oxide is usually needed to reduce the Dit level.

Direct bonded copper
(DBC). DBC is a critical component in a power module, consisting of a ceramic layer sandwiched between two copper plates. The ceramic layer, composed of Si_3N_4, AlN, Al_2O_3 or BeO, is for heat conduction and high-voltage isolation, whereas the copper plate is for circuit wiring and heat spreading. Semiconductor dies are attached to the top copper plate by soldering or sintering, whereas the bottom copper plate connects to the baseplate by soldering.

Freewheeling diode
(FWD). A diode antiparallel to a power switch for absorbing flyback voltage generated by an inductive load is FWD. The flyback voltage occurs when there is a sudden change in the current flowing through the inductive load.

High-temperature gate bias
(HTGB) HTGB is the accelerated lifetime test for evaluating and qualifying the gate oxide reliability of the power device. For the EV application, according to the AEC-Q101 standard, the typical testing condition includes high temperature (150 °C or 175 °C), gate stress at 100% rated V_{GS} and duration of 1,000 h. Zero failure out of 77 samples multiplied by three lots can pass the qualification.

High-temperature reverse bias
(HTRB). HTRB is the accelerated lifetime test for evaluating and qualifying the ability to withstand off-state high drain bias of the power device. For the electric vehicle application, according to the AEC-Q101 standard, the typical testing condition includes high temperature (150 °C or 175 °C), drain stress at 100% rated blocking voltage and duration of 1,000 h. Zero failure out of 77 samples multiplied by three lots can pass the qualification.

$I_{C,sat}$
The collector current of an insulated-gate bipolar transistor, at which the current starts to saturate as the V_{CE} increases, is $I_{C,sat}$. When measuring $I_{C,sat}$, the V_{GE} is biased at a specific voltage larger than the threshold voltage.

On-resistance
When a power device (SiC metal oxide semiconductor field-effect transistor or GaN high electron mobility transistor) is on, the total resistance between the drain and source terminals is the on-resistance (R_{on}). Specific on-resistance ($R_{on,sp}$) is the area-normalized R_{on}, which can be obtained by multiplying R_{on} with the current conducting area of the power device.

Q_g
The gate charge required to fully turn on/off a power device is Q_g, which takes into account the varying input capacitance and varying gate voltage during the transient time.

Switching loss
During the transient time when a power switch turns on/off, the voltage drop across the power switch decreases/increases and the current flowing through the power switch increases/decreases. The integration of the voltage waveform multiplied by the current waveform over the transient time is the turn-on/off switching loss. If the overlap between the voltage and current waveforms is significant, leading to high switching loss, the condition is called hard switching. On the contrary, if the overlap between the voltage and current waveforms is negligible, leading to low switching loss, the condition is called soft switching.

Thermal resistance
Thermal resistance multiplied by heat current (W) is equal to the temperature difference (°C) needed for the heat transfer.

Time-dependent dielectric breakdown
(TDDB). TDDB is a phenomenon that occurs in Si, SiC and GaN-based devices with time-dependent breakdown in the insulating dielectrics. TDDB refers to the gradual degradation or failure of a dielectric layer owing to the application of a constant electric field over an extended period of time.

$V_{CE,sat}$
When an insulated-gate bipolar transistor is on, the collector-to-emitter voltage drop at a rated I_C and a specific temperature is $V_{CE,sat}$. A smaller $V_{CE,sat}$ means that the insulated-gate bipolar transistor has a smaller R_{on}. Generally, there is a trade-off between the $V_{CE,sat}$ and turn-off switching loss for insulated-gate bipolar transistors.

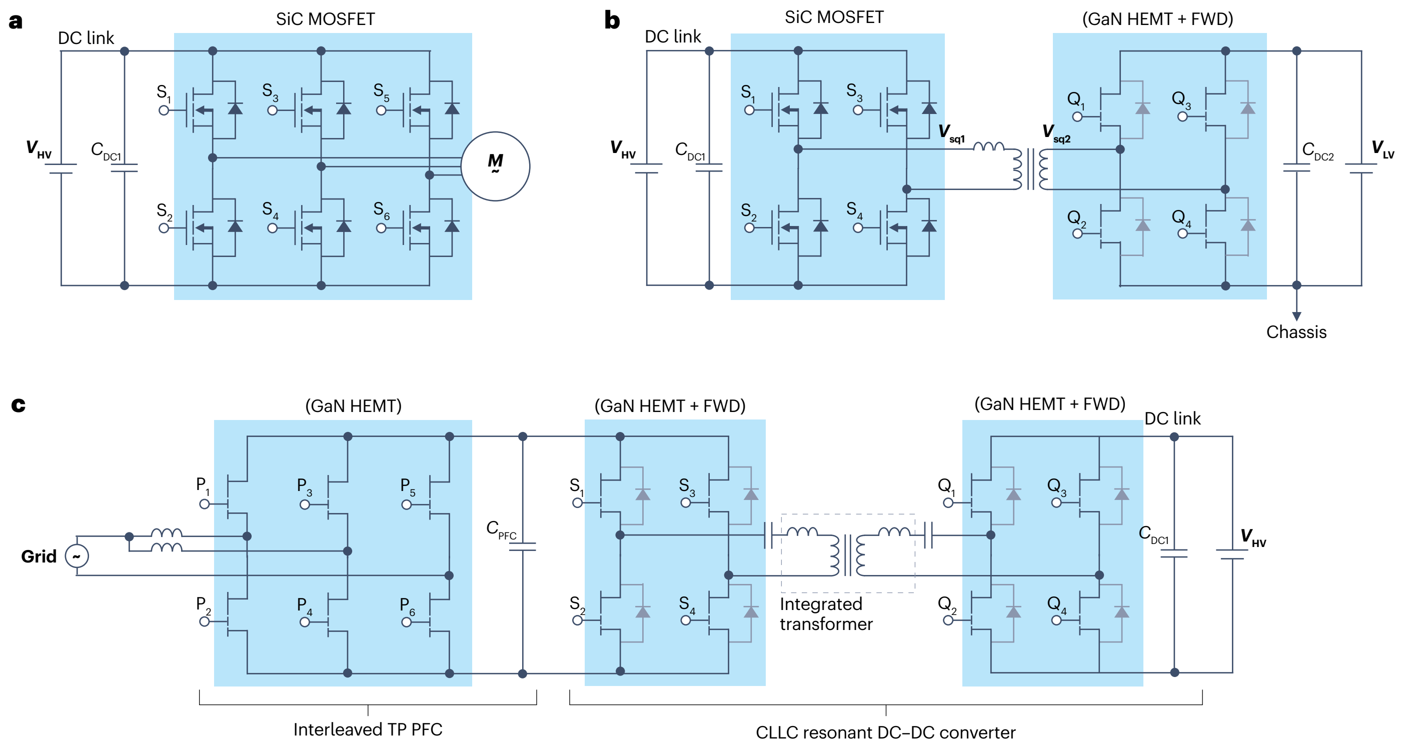


Fig. 4 | Circuit topologies for electric vehicle power modules. **a**, Circuit topology of a two-level/three-phase inverter, in which V_{HV} represents a high-voltage battery and C_{DC1} represents a DC link capacitor for protecting the battery and power switches from large current and voltage spikes. For V_{HV} = 800 V, the best options for power switches $S_{1,2,3,4,5,6}$ are 1,200-V SiC metal oxide semiconductor field-effect transistors (MOSFETs). **b**, Circuit topology of a dual-active-bridge-isolated bidirectional DC–DC converter, in which V_{LV} represents a low-voltage battery. The direction and amplitude of the power transmission between the low-voltage battery and high-voltage battery can be easily modulated by adjusting the phase difference between the AC square waves at both ends of the transformer (V_{sq1} and V_{sq2}). For V_{HV} = 800 V and V_{LV} = 48 V, the best options for power switches $S_{1,2,3,4}$ are 1,200-V SiC MOSFETs, and 100-V GaN high electron mobility transistors (HEMTs) with antiparallel freewheeling diodes (FWDs) for absorbing flyback voltages are the best options for power switches $Q_{1,2,3,4}$. The negative terminal of the low-voltage battery is connected to the vehicle chassis. Therefore, galvanic isolation achieved by the transformer is critical. **c**, Circuit topology of an all-GaN-based two-stage bidirectional onboard charger (OBC), consisting of an interleaved totem pole power factor correction (TP PFC) and a capacitor-inductor-inductor-capacitor (CLLC) resonant DC–DC converter for charging a 400-V battery. The circuit topology is based on the Texas Instruments 6.6-kW bidirectional OBC[76]. At high switching frequencies, the transformer leakage inductance can be utilized for the resonant inductance to enable both reduced cost and size. The resonant energy stored in the LC resonant tank makes the transformer current close to sinusoidal around the resonant frequency. The best options for power switches $P_{1,2,3,4,5,6}$ are 650-V GaN HEMTs, which do not have body diodes, resulting in reduced reverse recovery loss. For V_{HV} = 400 V, the best options for power switches $S_{1,2,3,4}$ and $Q_{1,2,3,4}$ are 650-V GaN HEMTs for achieving high switching frequencies. For driving every power switch, opto-isolation between the driver and controller ICs is usually required. Most importantly, for each half-bridge, it is critical to prevent short-circuit, which occurs when the two switches in the same leg are on simultaneously. The sudden surge in current will seriously damage the power switches. Therefore, it is necessary to avoid false turn-on caused by gate control signal ringing and include dead time in the pulse width modulation waveform design for some cases.

signals, each 120° phase apart. The rotating magnetic field synthesized by the alternating stator current cuts the rotor, and the current induced in the rotor interacts with the rotating magnetic field to produce magnetic torque. The torque of a PMSM is proportional to the stator current, whereas the speed is proportional to the frequency of the PWM signals. Owing to its simplicity and minimum wear of components, a two-level inverter consisting of three half-bridges in parallel is the most widely used topology[55] (Fig. 4a). In general, the power switches of the inverters operating under 400-V battery systems require 650-V blocking voltage ratings, so that the switches can handle stray-inductance (L_{stray})-induced V_{DS} overshoots ($L_{stray} \times dI_D/dt$) during turn-off transients. Similarly, the 800-V inverters require 1,200-V rated power switches. Although the half-bridge/full-bridge modules based on Si IGBTs are commercially available in 650 V and 1,200 V (Fig. 5a), those based on SiC MOSFETs are predominantly offered in 1,200 V (Fig. 5c). Although the blocking voltage ratings of commercial GaN HEMTs can rarely reach 1,200 V (Fig. 3g), 800-V traction inverters based on 650-V GaN HEMTs can be still implemented by using a three-level active neutral point clamped topology[56]. However, because GaN HEMTs do not have body diodes such as SiC MOSFETs, antiparallel SiC Schottky barrier diodes as the FWDs are generally required. Six power switches of the two-level inverter are controlled by a microcontroller unit through various sinusoidal PWM schemes to increase the utilization ratio of the DC link voltage and to decrease the total harmonic distortion, which otherwise may cause torque fluctuations and power losses[57]. Most importantly, with respect to the 400-V powertrain, the inverter driving an 800-V rated motor under an 800-V battery system has significantly lower conduction loss ($I_D^2 \times R_{on}$), as only a half of the phase current is required to drive the motor of the same power[58].

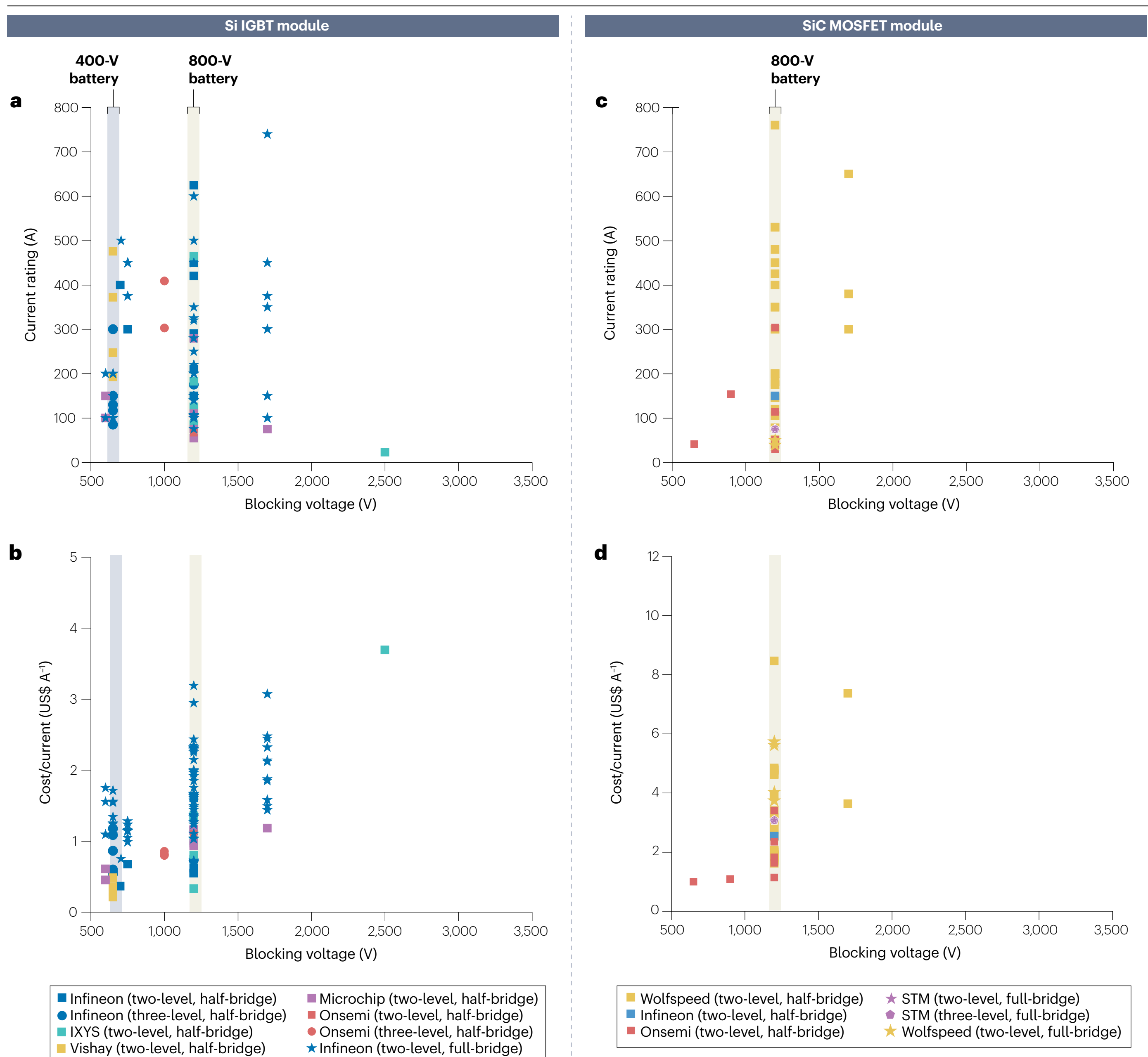


Fig. 5 | Performance and cost comparisons for electric vehicle power modules. a,**b**, Current rating (**a**) and cost per current (**b**) versus blocking voltage rating for Si insulated-gate bipolar transistor (IGBT) modules from different companies. **c**,**d**, Current rating (**c**) and cost per current (**d**) versus blocking voltage rating for SiC metal oxide semiconductor field-effect transistor (MOSFET) modules from different companies. Note that the cost per current here is defined as the module cost divided by the module current rating.

Under the double-pulse testing condition, an SiC MOSFET half-bridge module has only 1/8 of the switching loss of its Si IGBT counterpart[59]. The Si IGBT module suffers from a higher turn-on loss owing to a larger current overshoot caused by the reverse recovery of FWD and from a higher turn-off loss owing to the tail current for dissipating holes in the drift layer. By contrast, although an SiC MOSFET module can switch faster with less loss, it is associated with a stronger electromagnetic interference owing to high dV_{DS}/dt and dI_D/dt (up to 20×10^9 V s^{-1} and up to 5×10^9 A s^{-1} during turn-on transient)[60]. High dV_{DS}/dt and dI_D/dt also cause serious ringing and crosstalk. In a practical powertrain application instead of double-pulse testing, the SiC MOSFET inverter can still offer about three times less switching loss than the Si IGBT inverter, but the conduction losses of the two inverters are comparable[61]. Despite the superior performance, owing to the high cost of SiC substrate and epitaxy as mentioned previously, the 1,200-V SiC MOSFET modules have two times higher cost per current (US$ A^{-1}) than

the 1,200-V Si IGBT modules (Fig. 5b,d). To break the trade-off between cost and performance, further research on lowering the proportion of material cost in the average die cost of SiC MOSFETs is urgently needed. The key specifications of recent EV traction inverters from academic and industrial institutes operating under the DC link voltages of 800 V are listed in Table 1. For standard 800-V inverters based on 1,200-V SiC MOSFETs, power densities higher can 40 kW l^{-1} have been achieved, with the overall efficiencies near unity. In addition to the most commonly used two-level/three-phase topology, two-level/six-phase and four-level/three-phase topologies have also been demonstrated[62,63]. Furthermore, unlike the conventional two-level topology in which all power switches are for hard switching and stressed under a 800-V DC link voltage during commutation, a hybrid T-type three-level configuration based on GaN HEMTs and Si IGBTs is proposed by GaN Systems for reduced switching losses[64]. Finally, the switching frequencies of the traction inverters (Table 1) lie between 5 kHz and 50 kHz, which is well suited for SiC MOSFETs with a reduced switching loss and smaller device footprints with respect to Si IGBTs[65].

DC–DC converters

DC–DC converters or auxiliary power modules in EVs provide low-voltage DC power needed for electrical accessories, including headlights, interior lighting, wipers and so on (Fig. 1b). As the driving automation moves beyond the Society of Automotive Engineers (SAE) level 2, EVs consume much more electricity to process the vast amount of information from the advanced driver-assistance system (ADAS) and the sensors for millimetre-wave and light-wave detection and ranging (LIDAR). Compared with other topologies with less number of switches, a dual-active-bridge-isolated bidirectional DC–DC converter has eight switches for high-power transmission and is capable of soft switching and bi-directional power transfer owing to its symmetric structure[66] (Fig. 4b). By applying soft switching technique, a power switch has almost zero switching loss when turning on and off. To achieve high-power densities, the transformer and capacitor form factors have to be small, which require the switches to operate in a range from a few hundred kilohertz to a few megahertz. Despite the high switching frequency, the overall switching loss can be low owing to soft switching. Although SiC MOSFETs and GaN HEMTs are designed to turn on and off in the aforementioned frequency range, the core loss and copper loss of the transformer could increase, as the skin effect, in which AC current flow is concentrated near the copper wire surface, becomes prominent at high frequencies[67]. Significant research has been devoted to the optimization of high-frequency transformers, such as the utilization of multistrand Litz wire and the adoption of high-frequency ferrite core materials[68,69]. The key specifications of recent DC–DC converters from academic and industrial institutes for high DC link voltages (~800 V) to low DC voltages conversion are listed in Table 1. The DC–DC converters have the output power between 1 kW and 7 kW. Particularly, the converter based on GaN HEMTs has demonstrated a power density above 10 kW l^{-1} with the switching frequency of 700 kHz (ref. 70).

Onboard chargers

As mentioned previously, the convenience of charging is one key factor that determines the widespread adoption of EVs. High-voltage batteries of an EV can be charged off-board at fast-charging stations, such as an 800-V ABB Terra HP, which deliveries DC power directly to the battery, or through its own OBC (Fig. 1b). Nowadays, bidirectional OBCs are gaining much attention because the large battery capacity of EVs can be used for transportation, as well as vehicle-to-x charging. For example, vehicle-to-load can power electronic devices through standard onboard AC sockets; vehicle-to-home can power household appliances through interconnection with a local home grid, and vehicle-to-grid provides ancillary services to the grid (that is, valley filling at low demand and discharging surplus electricity at high demand), making the grid more resilient and stable as the EV fleet grows[71,72]. A standard OBC consists of two stages: a power factor correction circuit to rectify and compensating the lagging current and a DC–DC converter to provide galvanic isolation and charge the high-voltage battery with the requested voltage and current (Fig. 4c). Compared with the classic boost converter, the totem-pole power factor correction topology does not include a rectifying diode bridge at the input, leading to a 50% reduction in total power loss owing to diode conduction loss[73]. On the DC–DC converter side, the CLLC resonant converter features the same zero voltage switching technique as the conventional LLC, while having a symmetrical resonant tank, making it well suited for bi-directional operation[74]. Currently, the average EV battery capacity is 50 kWh (ref. 75). At the same time, high-end EVs, such as Mercedes-Benz EQS 450+, Audi Q8 e-tron GT and BMW iX xDrive 50, have the battery capacities larger than 105 kWh. To ensure the battery can be fully charged overnight, the output power of the OBC needs to match the battery size. Taking the Texas Instruments 6.6-kW bidirectional OBC based on GaN HEMTs, for example, the OBC can charge a 50-kWh battery from 20% to 80% in 4.5 h (ref. 76). However, for larger battery sizes, OBCs with a three-phase grid connection and a level-2 charging power (from 7 kW to 22 kW) are required, such as a 22-kW OBC in Porsche Taycan. Table 1 lists the key specifications of recent OBCs from academic and industrial institutions for charging high-voltage (~800-V) batteries of EVs. With three-phase AC inputs from the grid, the OBCs can achieve output power from 11 kW to 22 kW, whereas the state-of-the-art power densities can exceed 3 kW l^{-1} with near unity efficiencies.

EV power modules

Benefits of 800-V powertrain

To date the powertrains of most EVs operate on 400-V architectures, powered by 96 Li-ion battery cells in series, each having a peak voltage of 4.2 V. However, limited by the maximum currents of fast-charging cables (250 A by air cooling and 500 A by liquid cooling)[77] and the charging rate allowed by the BMS, a 400-V battery pack can only be charged at the maximum power of 200 kW. Therefore, to achieve the goal of charging a 100-kWh battery in under 20 min, the benchmark set for the next-generation ultrafast charging EVs, it is imperative to shift from 400-V to 800-V battery systems. For example, 800-V Porsche Taycan Turbo S with a battery capacity of 93.4 kWh can be charged from 5% to 80% state of charge in 22.5 min (ref. 78). Besides, increasing DC link voltage to 800 V can extend the motor speed range, reducing the maximum torque needed to produce the same traction power[58]. Considering that the motor size is roughly proportional to its torque capability, the motors with higher DC link voltages can potentially have smaller form factors and higher power densities. For example, the power density of the 2010 Toyota Prius motor with 650-V DC link is 45% higher than that of the 2004 model with 500-V DC link[79]. However, a higher DC link voltage requires a thicker insulator with a higher dielectric strength for preventing partial discharge at the slot insulation, which could increase the motor size. In general, doubling the DC link voltage from 400 V to 800 V means that the required current for delivering the same power

Table 1 | Key specifications of recent traction inverters, DC–DC converters and onboard chargers

800-V traction inverter

References	Year	DC link voltage (V)	Output power (kW)	Power density ($kW\,l^{-1}$)	Efficiency (%)	Switching frequency (kHz)	Circuit topology	Semiconductor type
McMaster Automotive Resource Centre[62]	2023	800	100	40	97	30	Two-level Six-phase	1,200-V SiC MOSFET
University of Arkansas[98]	2023	1,000	200 (peak)	43 (peak)	99	10	Two-level Three-phase	1,700-V SiC MOSFET
NXP[99]	2023	800	200	NA	99	NA	Two-level Three-phase	1,200-V SiC MOSFET
Politecnico di Torino/National New Energy Vehicle Technology Innovation Center[100]	2022	800	400	52	NA	20–50	Two-level Three-phase	1,200-V SiC MOSFET
University of Texas at Austin[101]	2021	800	300	44	99	30	Two-level Six-phase	1,200-V SiC MOSFET
University of Bristol[63]	2021	1,200	100	19	99	5	Four-level Three-phase	1,200-V SiC MOSFET
VisIC/Hofer[102]	2021	800	100	50	99	40	Three-level Three-phase	650-V GaN HEMT
University of Arkansas[103]	2020	800	150	86	99 (simulated)	10–15 (simulated)	Two-level Three-phase	1,200-V SiC MOSFET
Continental Engineering Services[104]	2020	820	246	14 (including connectors)	NA	NA	Two-level Three-phase	1,200-V SiC MOSFET
GaN Systems[64]	2018	800	150	NA	NA	10	Hybrid T-type Three-level Three-phase	650-V GaN HEMT and 1,200-V Si IGBT

800-V DC–DC converter

References	Year	Input–output voltages	Output power (kW)	Power density ($kW\,l^{-1}$)	Efficiency (%)	Switching frequency (kHz)	Circuit topology	HV/LV semiconductor type
University of Tennessee[105]	2023	180–900 VDC/ 6–16 VDC	3	NA	97 (peak)	80	DAB (current-fed)	SiC MOSFET/ Si MOSFET
Inha University[106]	2023	400–800 VDC/ 13–15 VDC	2.1	5.2	95	200	Phase shift Full-bridge	SiC MOSFET/ Si MOSFET
BorgWarner[107]	2023	220–800 VDC/ 12 VDC	7.2	1.4	92	NA	NA	NA
Belfuse[108]	2023	400–800 VDC/ 9–16 VDC	4	0.6	93	NA	NA	NA
Seoul National University of Science and Technology/ Hyundai Motor Company[70]	2021	460–780 VDC/ 11.5–15.1 VDC	1.2	10.2 (not including heatsink)	93	700	Input series Half-bridge	GaN HEMT
University of Arkansas[109]	2021	700–800 VDC/ 48 VDC	5	5	97	100	LLC	SiC MOSFET/ Si MOSFET

800-V OBC

References	Year	Input–output voltages	Output power (kW)	Power density ($kW\,l^{-1}$)	Efficiency (%)	Switching frequency (kHz)	Circuit topology	Semiconductor type
Universidad de Zaragoza/ ETH Zurich[110]	2023	Three-phase 85–265 VAC/ 550–850 VDC	11	3.7 (not including transformer)	PFC: 97 DC–DC: 98.5	PFC: 100 DC–DC: 100	PFC: boost DC–DC: DAB	SiC MOSFET
Virginia Tech[111]	2022	Single-phase 240 VAC/600–800 VDC	11	3.2	98 (peak)	PFC: 350 DC–DC: 500	PFC: TP DC–DC: CLLC	SiC MOSFET
Myongji University[112]	2022	Three-phase 380 VAC/650–900 VDC	11	1	96	PFC: 20 DC–DC: 140	PFC: boost DC–DC: CLLC	SiC MOSFET

Table 1 (continued) | Key specifications of recent traction inverters, DC–DC converters and onboard chargers

800-V OBC (continued)								
References	**Year**	**Input–output voltages**	**Output power (kW)**	**Power density ($kW\,l^{-1}$)**	**Efficiency (%)**	**Switching frequency (kHz)**	**Circuit topology**	**Semiconductor type**
Korea Aerospace Research Institute[113]	2022	Three-phase 380 VAC/460–800 VDC	11	5.3	97 (peak)	150	PFC: TP DC–DC: DAB (current-fed)	SiC MOSFET
Inha University, Incheon[114]	2022	NA/380–710 VDC	3.3	NA	98	175–185	PFC: NA DC–DC: LLC (variable PFC output)	SiC MOSFET
Wolfspeed[115]	2021	Three-phase 304–456 VAC/ 200–800 VDC	22	8	98 (peak)	PFC: 45 DC–DC: 140–250	PFC: TP DC–DC: CLLC	SiC MOSFET
Ovartech[116]	2021	Three-phase 323–437 VAC/ 440–740 VDC	20	1.7	95	NA	NA	NA
Innoelectric[117]	2021	Three-phase 382–480 VAC/ 400–900 VDC	22	0.8	94	NA	NA	NA

Specifications shown are from academic and industrial institutes operating under the DC link voltages around 800 V. DAB, dual-active bridge; HEMT, high electron mobility transistor; HV, high voltage; IGBT, insulated-gate bipolar transistor; LV, low voltage; MOSFET, metal oxide semiconductor field-effect transistor; NA, not available; OBC, onboard charger; PFC, power factor correction; TP, totem pole; VAC, volts alternating current; VDC, volts direct current.

is reduced by half, which implies a smaller cable diameter and a lower weight, hence the extended driving range. Nevertheless, upgrading from 400-V to 800-V battery will double the number of the BMS, raising the cost by 30% (ref. 58). The examples of EV models adopting 400-V battery systems include Tesla Model S and Y, Nissan Leaf, BMW iX and Mercedes EQS, whereas those adopting 800-V battery systems include, for example, Maserati GranTurismo Folgore, Lotus Eletre, Porsche Taycan, Lucid Air Dream, Cadillac Lyriq, Audi e-tron, Hyundai Ioniq 5, Genesis GV60, Kia EV6, Xpeng G9, BYD Seal and other BYD models on the e-platform 3.0.

Module integration

Further increase in power densities and efficiencies could be achieved via integration of modules with complementary functionalities into a single module. For example, a non-isolated three-phase interleaved cascaded buck-boost OBC can share a part of its boost pole to form another full-bridge DC–DC converter, which charges the low-voltage battery from the high-voltage battery[80]. By sharing some semiconductor devices and mechanical parts, the charging of both high-voltage and low-voltage batteries can be achieved in one module, increasing the power density by 18% at similar efficiency. The e-POWER system developed by NISSAN integrates a 400-V battery, a maximum 100-kW motor, a maximum 24 $kW\,l^{-1}$ Si IGBT inverter and a dedicated high-efficiency internal combustion engine as the electricity generator into one powertrain module. The wheels are purely driven by the motor, whereas the engine starts to generate electricity for powering the inverter only at high speed when the engine is most efficient[81]. The US Department of Energy sets a 2025 power density target of 33 $kW\,l^{-1}$ for a 100-kW traction drive system, including the inverter and motor. The standard 800-V inverters based on 1,200-V SiC MOSFETs can achieve power densities higher than 40 $kW\,l^{-1}$ (Table 1). By contrast, most EV motors, although occupying a vast majority of the traction drive system volume, have power densities less than 10 $kW\,l^{-1}$ (ref. 82). To further improve the power density of the motor, it is crucial to increase the rotational speed of the motor and to optimize the rotor structure.

Die parallelization

The current rating of a single power switch (Fig. 3a,d,g) is usually insufficient to meet the current rating of a power module (Fig. 5a,c). When multiple discretes or dies are paralleled to form a power switch with a higher current rating, optimum parallelization is necessary to balance the gate control signals among the paralleled power devices. Unbalanced gate control, caused by different stray inductances of the gate control loops, can cause uneven power losses and non-uniform thermal distributions, which can in turn lead to thermal runaway and module failures[83]. To prevent this outcome, first, the paralleled devices must have positive temperature coefficients, that is, larger R_{on} with higher T_j. Generally, a V_{GE} of Si IGBTs above 10 V or a V_{GS} of SiC MOSFETs above 15 V can ensure the power devices operate in the positive temperature coefficient condition[84]. Second, the impact of parasitic source inductance (L_S, usually around 10 nH) can be reduced by using the Kelvin source pin. Without the Kelvin pin, during the turn-on transient, I_D rapidly increases and a positive L_S-induced voltage equal to $L_S \times (dI_D/dt)$ is generated, which lessens the effective gate bias and therefore increases the switching loss. Similar phenomenon occurs during the turn-off transient. With the help of the Kelvin source pin, the parasitic source inductance-induced voltage in the gate control loop becomes $L_K \times (dI_G/dt)$, in which L_K is the Kelvin pin stray inductance (Fig. 6a). Since I_G the gate current for charging or discharging the gate capacitance is much smaller than I_D, the adverse effect of parasitic source inductance is much alleviated. Third, the gate control loops need to be as short as possible, to minimize the oscillation and transient voltage drop owing to the parasitic gate resistance ($R_G \times I_G$) and parasitic gate inductance ($L_G \times (dI_G/dt)$). Finally, the control signal path layout designs for all paralleled power devices need to have similar length and width, so that the stray inductance of each gate control loop is close to each other[83].

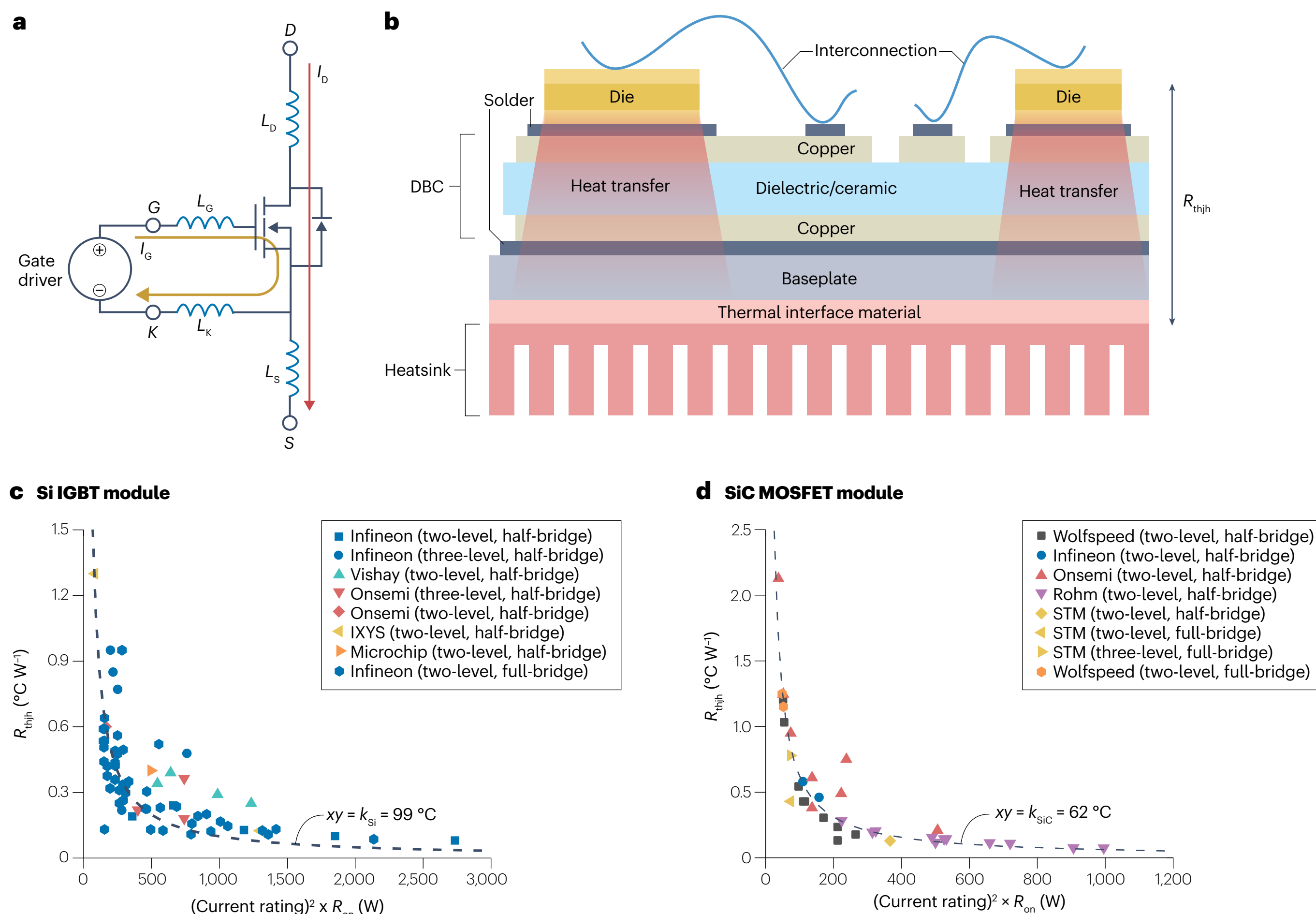


Fig. 6 | Parasitic inductance and thermal resistance of electric vehicle power modules. a, Schematic illustration of an SiC metal oxide semiconductor field-effect transistor (MOSFET) with an additional Kelvin source pin. The L_D, L_S, L_K and L_G represent the stray inductances for the drain, source, Kelvin pin and gate terminals, respectively. **b**, Cross-section illustration of a conventional electric vehicle power module, including semiconductor dies, die attachment and interconnection, direct bonded copper (DBC), baseplate, thermal interfacing material and heatsink. **c**, Thermal resistance from power device to heatsink (R_{thjh}) of various commercial Si insulated-gate bipolar transistor (IGBT) modules versus the square of the module current rating multiplied by the on-resistance (R_{on}) of a power switch in the module. **d**, R_{thjh} of various commercial SiC MOSFET modules versus the square of the module current rating multiplied by the R_{on} of a power switch in the module.

Thermal resistance

In the process of power conversion, conduction, switching, reverse recovery and other energy losses of a power switch are transformed into heat, which elevates the junction temperature and affects the performance and reliability of the power device and its package. The maximum junction temperatures ($T_{j,max}$) of commercial power devices are typically in the range of 150–175 °C, whereas some SiC MOSFETs can have $T_{j,max}$ up to 200 °C. One critical functionality of the power module is to enable efficient heat extraction from the power devices, to maintain the working junction temperature below $T_{j,max}$ at all times. The heat is transferred from the die surface, where the power device is located, through the semiconductor substrate, direct bonded copper (DBC), baseplate, thermal interfacing material and, finally, to the heatsink (Fig. 6b). The heat generated by a conducting power switch in a module can be estimated by the square of the module current rating multiplied by the power switch R_{on}. Then $R_{thjh} \times ((\text{current rating})^2 \times R_{on}) \approx T_{j,max} - T_{heatsink}$, in which R_{thjh} is the thermal resistance (°C W^{-1}) from the power device to heatsink and $T_{j,max} - T_{heatsink}$ is the temperature difference between the power device and heatsink. For commercial Si IGBT modules (Fig. 6c), the R_{thjh} is inversely proportional to ((current rating)$^2 \times R_{on}$) and the fitted constant $T_{j,max} - T_{heatsink} = k_{Si}$ is equal to 99 °C, indicating that the module generating more heat requires smaller R_{thjh}. In comparison, for commercial SiC MOSFET modules (Fig. 6d), a similar inverse proportion relationship is observed but the fitted constant $T_{j,max} - T_{heatsink} = k_{SiC}$ is equal to 62 °C, indicating that the $T_{heatsink}$ for SiC MOSFET modules is higher than that for Si IGBT modules, as $T_{j,max}$ is similar for both devices. The thermal conductivity of 4H-SiC (300–400 W m^{-1} K^{-1}) is two times higher than that of Si (170 W m^{-1} K^{-1}), making the heat extraction from SiC MOSFETs more efficient. Also, owing to the large energy bandgap of 4H-SiC (3.3 eV), the off-state leakage current of the SiC MOSFET, which is proportional to the square of the intrinsic carrier concentration, remains low at high temperatures. Therefore,

the power modules based on SiC MOSFETs require less cooling than those based on Si IGBTs.

Die attachment and interconnection

In SiC MOSFET dies, the drain metallization layer at the bottom can be attached to the top copper layer of the DBC by soldering, which however requires a careful selection of the melting temperature of the solder, thermal conductivity and coefficients of thermal expansion. Meanwhile, alternative methods, such as silver-sintering and transient liquid-phase bonding[85], could further improve the power cycling reliability. By contrast, the source and gate metallization layers on the die surface are connected to the DBC through Al wire bonding. As the diameters of the Al bond wires are only 300–400 µm, resulting in a high current density and a low thermal capacity, the Al bond wires are often subject to rapid and extensive temperature fluctuations. As a result, wire-lift off may occur after prolonged accumulation of stress. To tackle the thermal–mechanical reliability issue, advanced bonding techniques, such as ribbon bonding and direct lead bonding, have been proposed[86,87]. Moreover, to further eliminate parasitic inductance, planar and pressure-based bondless interconnections have been demonstrated[88]. In general, the goal is to increase the contact area with the dies, thereby enhancing the current carrying capacity and reducing the thermal resistance. It is important to note that adopting these new techniques may require modifications to the die metallization layers, which may increase the manufacturing costs.

DBC, baseplate and heatsink

The DBC plays an important role in a power module by providing electrical insulation, mechanical support and thermal conduction. The ceramic layer sandwiched between the two copper plates ensures electrical insulation, while having high thermal conductivity (Si_3N_4 60 W m^{-1} K^{-1}, AlN 170 W m^{-1} K^{-1}, Al_2O_3 33 W m^{-1} K^{-1} and BeO 270 W m^{-1} K^{-1})[89]. The circuits are formed on the top copper plate and the bottom copper plate is attached to the baseplate by soldering. Recently, various substrates similar to DBC have been demonstrated to further improve the power cycling reliability, such as DBC with a meshed bottom plate, direct bonded aluminium, direct plated copper, active metal brazing and insulated metal substrate[90,91]. The baseplate, on which the DBC is soldered, provides heat dissipation and robust mechanical support. Typically, the baseplates are made of AlSiC or Cu. To achieve low thermal expansion and to maintain high thermal conductivity, alloys of W-Cu, Mo-Cu and Cu-Mo-Cu are used. The other side of the baseplate connects to the heatsink through a very thin layer of the thermal interfacing material, such as thermal paste that eliminates air gap between the baseplate and heatsink and enhances thermal conductivity. For the heatsink design, the circular pin-fins with cool water passing through horizontally are commonly used for the EV applications. Other fin configurations, such as flat and elliptical fins, and microchannels have also been explored[92].

Encapsulation and packages

Typically, a thin layer of polyimide, which has the breakdown electric field of 1–2.8 MV cm^{-1}, is applied on top of the bare dies to provide electrical insulation and prevent leakage current. Then, an additional layer of silicone gel, epoxy resin or silicone elastomer is deposited on the polyimide layer to protect the module against environmental factors. The total thickness of the encapsulation depends on the blocking voltage and temperature ratings. Currently, investigations of ceramic encapsulants are underway, as the inorganic encapsulants tend to have higher thermal conductivity than organic counterparts[93]. In particular, there are several standardized half-bridge or full-bridge packages based on SiC MOSFETs on the market developed by teir-1 suppliers, such as the HybridPACK by Infineon, the ACEPACK DRIVE by STMicroelectronics, the XM3 by Wolfspeed, the AHPM15 by Onsemi, the E/G-type by Rohm, the SEMITRANS by Semikron Danfoss, the Viper by BorgWarner, the NX-type by Mitsubishi, the Suijin by Hitachi, the REVOSIC by Denso and the CSL-type by Bosch. Each of these package designs has its own proprietary innovative features of the module structures and packaging materials, highlighting the rapid technological advancements of 800-V SiC powertrains in the EV industry.

Outlook

By shifting the battery voltage from current 400 V to 800 V, the module power densities can be increased and the battery charging time can be reduced. Under the 800-V battery architecture, the traction inverters based on SiC MOSFETs can achieve higher efficiencies than those based on Si IGBTs, mainly because of the lower switching losses. Moreover, the SiC MOSFETs are more suitable for high-temperature operations, because of the higher thermal conductivity and larger energy bandgap of SiC. However, owing to the high cost of the SiC substrate and epitaxy, the cost per current (US $ A^{-1}) of SiC MOSFET modules is about two times higher than that of Si IGBT counterparts. Therefore, finding strategies to lower the proportion of material cost in the average die cost is likely to become the major challenge faced by the SiC industry. Recently, several SiC substrate engineering solutions, such as the 'cold split' technology developed by Siltectra, which precisely splits one SiC wafer into two with no kerf loss, and the 'smart cut' technology developed by Soitec, which precisely cuts a thin layer of crystalline SiC from the boule and transfers it onto a different substrate, have shown the great potential to significantly lower the SiC substrate cost. Furthermore, several integrated device manufacturers, such as Wolfspeed, Infineon, STMicroelectronics and Sanan joint venture, Rohm, Onsemi and Bosch, have recently announced to expand their front-end device manufacturing and substrate production capacity by upgrading from 150 mm to 200 mm SiC wafers. With more production volume available, the price of SiC MOSFETs can be lower, which in turn will lead to more adoption and higher demand of 800-V traction inverters in EVs. From the fabrication process perspective, in addition to the post-oxidation nitric oxide annealing and the pre-oxidation H_2 etching for reducing Dit, using high-κ gate dielectrics with ultrawide bandgaps, such as Al_2O_3, AlN and AlON, is also promising for SiC MOSFETs to further reduce the gate leakage current and to improve the TDDB reliability[94].

For the DC–DC converters and OBCs to achieve high-power densities, the switching frequency needs to be sufficiently high to reduce the capacitor and transformer sizes. To this end, although not widely used in EVs at present, GaN HEMTs with low $R_{on} \times Q_g$ are ideal for fast-switching. However, commercial E-mode p-GaN HEMTs usually suffer from V_{th} instability and TDDB. To further improve the p-GaN gate reliability is critical for the wider applications of GaN HEMTs in EVs. Currently, the promising solutions include engineering the gate/p-GaN junction and optimizing the Mg-doping concentration in the p-GaN layer[95] (Fig. 2j). Meanwhile, dynamic R_{on}, which is mainly due to charge trapping in the buffer and passivation layers and/or near the interface between the passivation layer and AlGaN layer (Fig. 2j), degrades the performance of GaN HEMTs in converter applications. Refining the carbon doping in the buffer layer, using engineering substrates (for example, GaN-on-QST) for less threading dislocations and

optimizing the field-plate and passivation layer are so far the main research directions for resolving the dynamic R_{on} issue[96].

Finally, it is desirable for the power modules in EVs to have smaller form factors and lighter weights for extending the driving range. However, it becomes challenging to efficiently extract and dissipate heat from the power modules with very high-power densities. To this end, layout designs with low parasitics and building materials with high thermal conductivities and well-matched expansions are critical to ensure sufficient power cycling reliability. Particularly, silver-sintering with exceptional thermal and electrical conductivity has been applied for attaching SiC MOSFET dies to DBC (Fig. 6b) by several leading EV manufacturers such as Tesla and BYD. For heat dissipation, double-sided cooling, which has already been used in Infineon's HybridPACK DSC and Onsemi's VE-Trac modules, is an emerging technology in module thermal management[97]. Combined together, efficiency as well as reliability and cost constitute the three main pillars to support the continuous growth of the EV power electronics.

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