

## ARTICLE

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# An adapted method for analyzing 4H silicon carbide metal-oxide-semiconductor field-effect transistors

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Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are key devices for next-generation power electronics. However, accurate determination of device parameters from 3-terminal characteristics is hampered by the presence of interface traps. Here we present a method that, in contrast to previous evaluation schemes, explicitly considers those defects. A well-tractable parametrization of the SiC/SiO<sub>2</sub>-specific interface trap spectrum is introduced that reflects the body of known data. With this ingredient, we develop an analysis that targets for an accurate determination of device parameters from simple 3-terminal characteristics. For its validation, we investigate MOSFETs with significantly different defect densities. The resulting parameters – charge carrier density, mobility and threshold voltage – are in excellent agreement with Hall effect investigations on the very same devices, avoiding systematic errors inherent to conventional evaluation techniques. With this adapted scheme, 4H-SiC power MOSFETs, even packaged, can be meaningfully characterized, speeding up innovation cycles in energy-saving power electronics.

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Silicon carbide (SiC) is the most important wide-bandgap semiconductor material for next-generation power electronic devices. The commercialization of SiC devices started in 2001 with the introduction of the first 4H-SiC-based Schottky diode<sup>1</sup>. A great challenge for SiC technology is the fabrication of metal-oxide-semiconductor field-effect transistors (MOSFETs). Such unipolar transistors are, e.g., a power-saving substitution for silicon-based insulated-gate bipolar transistors (IGBTs) as power switches<sup>2</sup>. A material peculiarity is the high density of defects at the 4H-SiC/SiO<sub>2</sub> interface near the conduction band edge, which gives a limitation that has been partially resolved by the introduction of a post-oxidation annealing (POA) process in nitric oxide (NO)<sup>3,4</sup>. That paved the way for commercial 4H-SiC MOSFETs. Nevertheless, there is still room for substantial performance improvements: despite nitridation processes, the density of interface traps ( $D_{it}$ ) is still at a very high level compared to, e.g., silicon MOSFET devices<sup>5,6</sup>. The performance of a MOSFET is often characterized by extraction of the mobility and the threshold voltage from 3-terminal characteristics<sup>7,8</sup>. In such commonly used evaluation schemes, originally developed for silicon based devices, the  $D_{it}$  is neglected and the inversion charge carrier density in the MOSFET channel is estimated from a simple plate capacitor approximation. Applied to SiC, this leads to an underestimation of the charge carrier drift mobility<sup>6,9</sup>. To experimentally distinguish between mobility and inversion charge carrier density, Hall-effect measurements in the MOSFET channel are the method of choice. They are, however, time-consuming and require special geometries with additional probes. This requirement is incompatible with typical power MOSFET designs with vertical channels (VMOS, Trench MOS).

The aim of this work is to provide a method for analyzing the performance of 4H-SiC n-MOSFETs of any geometry from a simple 3-terminal characterization. It includes the specific distribution of defects at the 4H-SiC/SiO<sub>2</sub> interface into the modeling of the drain current. A best fit to experimental transfer characteristics results in a reliable determination of the charge carrier mobility, the threshold voltage and the  $D_{it}$  in the energy range relevant for the MOSFET performance, without the need of Hall-effect measurements.

## Results

**Modeling.** The density of interface states in 4H-SiC MOS structures has been extensively studied. A common observation is a relatively flat distribution in the bandgap with an exponential increase towards the conduction band edge  $E_C$ <sup>10–12</sup>. Whereas the former part is often assigned to carbon-related defects directly at

the interface<sup>10,13</sup>, the increase towards  $E_C$  stems from electron traps in the oxide near the 4H-SiC/SiO<sub>2</sub> interface, so-called near interface traps (NITs)<sup>14</sup>. Those traps exhibit a rather sharp distribution in energy close to the conduction band edge of 4H-SiC<sup>15–17</sup>. Their microscopic origin is still unclear, but intrinsic defects in amorphous SiO<sub>2</sub><sup>18</sup> as well as extrinsic carbon-related defects near the interface<sup>19</sup> have been suggested.

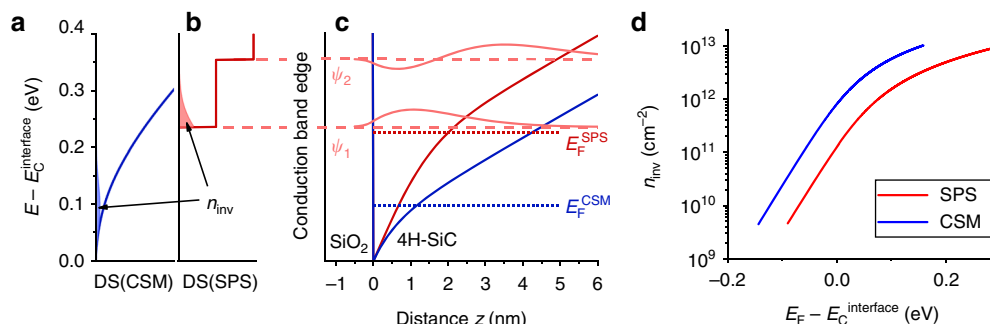
We propose an empirical parametrization that summarizes the body of findings in Eq. (1). The constant  $D_0$  reflects the above mentioned flat distribution of traps directly at the interface. The Gaussian term expresses the observed exponential increase of the density of NITs towards  $E_C$  and respects an overall finite number of defects.

$$D_{it} = D_0 + \frac{D_1}{\sigma \cdot \sqrt{\pi/2}} \cdot \exp\left(-\frac{2 \cdot (E - E_0)^2}{\sigma^2}\right). \quad (1)$$

A width in the range of  $\sigma = (100 \dots 200)$  meV and a position in the range of  $E_0 - E_C = (10 \dots 150)$  meV of the Gaussian part is consistent with the majority of reported experimental studies. This parametrization is the key ingredient to the subsequent method.

Transport in the channel is crucially determined by the inversion charge carrier density  $n_{inv}$  as a response to the gate voltage and is directly affected by the density of interface traps (Eq. (1)). The link between  $n_{inv}$  and  $V_G$  is the surface Fermi potential  $\phi_S = (E_F - E_i^{interface})/e$ .  $V_G$  is determined by Eq. (5) (see methods section).

$n_{inv}(\phi_S)$  can be calculated either by using the quasi-classical charge sheet model (CSM)<sup>20</sup> or by self-consistently solving the Schrödinger–Poisson equations (SPS)<sup>21,22</sup>. The CSM uses the 3D density of states in the conduction band to calculate the inversion charge carrier density by integration of the electron density in the inversion channel. It will turn out that this is an oversimplification relevant for our problem. The CSM introduces an artificial offset to the surface Fermi potential at a given charge carrier density, because it neglects the formation of 2D sub-bands in the inversion layer. Figure 1a and b compares the density of states in the inversion channel, Fig. 1c the band bending in the semiconductor and Fig. 1d  $n_{inv}$  as a function of  $\phi_S$ . For MOS parameters taken from the samples discussed later the CSM analysis introduces an error of more than 50 meV to  $\phi_S$ , as compared to the more refined SPS calculations. In the following, only the SPS analysis is employed.



**Fig. 1** Charge sheet model vs. Schrödinger–Poisson–Solver. **a** along the  $z$ -axis projected density of states in the inversion channel used in the charge sheet model (CSM); **b** density of states calculated using a Schrödinger–Poisson–Solver (SPS),  $E_F^{CSM}$  and  $E_F^{SPS}$  are the positions of the Fermi energy calculated via CSM and SPS respectively; **c** conduction bands of 4H-SiC calculated via CSM (blue) or SPS (red),  $z = 0$  denotes the 4H-SiC/SiO<sub>2</sub> interface, **d** dependence of the inversion charge carrier density  $n_{inv}$  from the surface Fermi potential  $\phi_S = (E_F - E_i^{interface})/e$ . The formation of the 2D sub-bands leads to a shift of at least 50 meV of the Fermi energy further into the conduction band compared to the quasi-classical solution of the CSM

With  $V_G(\phi_S)$ ,  $Q_{sc}(\phi_S)$  and  $n_{inv}(\phi_S)$ , the transfer characteristics  $I_D - V_G$  can be calculated using

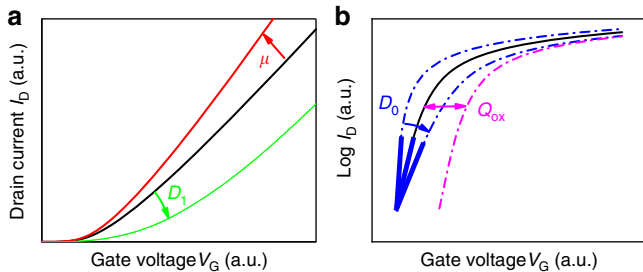
$$I_D = \frac{W}{L} \cdot e \cdot n_{inv}(\phi_S(V_G)) \cdot \mu \cdot (V_D - I_D R_S), \quad (2)$$

where  $W$  and  $L$  denotes the width and the length of the inversion channel, respectively, and  $R_S$  is the series resistance. The charge carrier mobility  $\mu$  can either be assumed constant, or more specific models can be implemented. Since Coulomb scattering is typically the dominating mobility limiting mechanism in lateral 4H-SiC n-MOSFETs, we opted for a power law description that reflects the potential screening with increasing charge carrier density<sup>23</sup>:

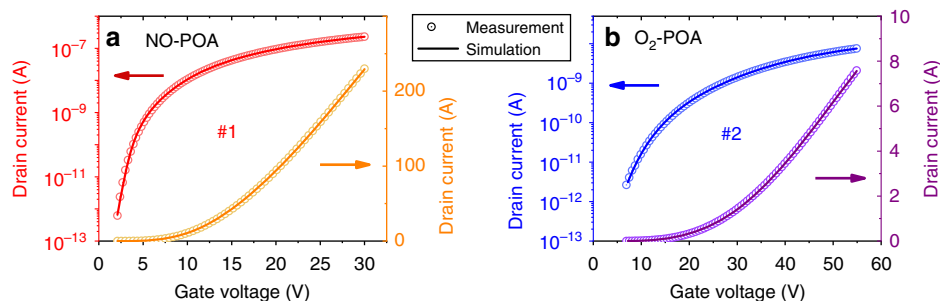
$$\mu(n_{inv}) = \mu_0 \cdot \left( \frac{n_{inv}}{n_0} \right)^\zeta, \quad (3)$$

with  $n_0$  and  $\zeta$  being an arbitrary reference value and an empirical exponent, respectively.

Figure 2 illustrates the effect of different parameters on the transfer characteristics on a linear and on a logarithmic scale, see in particular the figure caption. It turns out that each of the parameters  $\mu$ ,  $D_1$ , and  $D_0$  affects specific features of the shape of the transfer characteristics and can, thus, be well distinguished. In contrast, the neutral level  $E_n$  and the fixed oxide charge  $Q_{ox}$  both



**Fig. 2** Influence of model parameters. Scheme of the influence of the important simulation parameters on the transfer characteristic of a 4H-SiC n-channel metal-oxide-semiconductor field-effect transistor on **a** a linear and **b** a logarithmic scale. The constant part of the  $D_{it}$ -distribution  $D_0$  primarily adjusts the slope of the curve at low gate voltages on the logarithmic scale. The fixed oxide charge  $Q_{ox}$  shifts the gate voltage. The mobility  $\mu$  adjusts the slope at high gate voltages on the linear scale and the Gaussian part of the  $D_{it}$ -distribution  $D_1$  smears out the onset of the drain current and shifts the threshold voltage (which also does the parameter  $D_0$ , but  $D_0$  is already determined by the subthreshold region)



**Fig. 3** Comparison of measurement and simulation. Transfer characteristics of sample #1 (**a**) and sample #2 (**b**). The symbols represent the measured drain currents and the solid line is a best fit using our modeled  $D_{it}$ , Eq. (1). The data are shown on a linear and a logarithmic scale to show the excellent agreement of model and experiment

shift the curve on the  $x$ -axis and cannot be independently determined.

**Analysis.** In order to test the proposed evaluation scheme, MOSFETs with Hall bar geometries were designed and fabricated using an industrial process. They allow for measurements of Hall effect as well as of 3-terminal characteristics on the same device. Two series of samples with drastically different  $D_{it}$  were produced by variation of the process gas of the post-oxidation annealing (POA): nitric oxide (sample #1) and oxygen (sample #2).

Figure 3 shows the transfer characteristics of two of the investigated Hall-MOSFETs. During the measurement, a sufficient measurement delay after each gate voltage change ensured relaxation of the interface defect occupation into thermodynamical equilibrium. The symbols represent the measurement data and the lines are the least square fits of the model including the general shape of the  $D_{it}$  (Eq. 1). Table 1 summarizes the extracted performance parameters and compares the results to two frequently used conventional methods for performance analysis of MOSFETs and to results obtained by Hall-effect investigations. The Hall-effect method is the only one that independently and directly measures the charge carrier density and the Hall mobility. Therefore, it is the most reliable method and is taken as benchmark.

From Table 1 it can be seen that the two conventional methods based on transfer characteristics clearly underestimate the mobility due to negligence of interface traps. This effect becomes more pronounced for higher  $D_{it}$  and, remarkably, even leads to a deviation by more than one order of magnitude in the case of sample #2. This drastic discrepancy of the all-important parameter  $\mu$  could so far be resolved only in Hall-effect measurements requiring specific sample structures<sup>6,9,24,25</sup>. In contrast, the mobility values of our adapted method are in excellent agreement with the benchmark values obtained by Hall effect.

Furthermore, the introduced method delivers reliable values for the threshold voltage  $V_T$ , i.e., the onset of strong inversion ( $\phi_S = -\phi_B$ ). These values are much lower than the values extracted from linear extrapolation in conventional methods. This is obvious because the  $D_{it}$  close to  $E_C$  causes a soft turn-on of the transfer characteristics with notable deviation from linearity.

**Comparison to gate voltage-dependent Hall-effect investigations.** For closer analysis the proposed method is compared to Hall-effect measurements for various gate voltages, see Fig. 4. We find excellent agreement for the extracted inversion charge carrier densities and the charge carrier mobilities between both methods, for both samples (see Fig. 4a, b). In contrast to the large difference

in  $n_{\text{inv}}$ , both devices have nearly identical charge carrier mobilities, depending only on the charge carrier densities, a fact that would have been overlooked by traditional evaluation schemes of 3-terminal measurements. An apparent difference of roughly a factor of two can rather be traced back to a generally lower charge carrier density in sample #2 than to a mobility enhancement by nitridation. An analysis of an extended data set, including nominally identical Hall-MOS devices with POAs in nitric oxide and oxygen shows that the difference in the curves displayed in Fig. 4b is rather within the device-to-device variation than a systematic influence of the post-oxidation treatment. Exponents  $\zeta$  in the power law in the range of 0.1...0.4 have been extracted. Altogether, nitridation of the oxide does not affect the charge carrier mobility, but strongly the field-effect efficiency, in agreement with previous studies<sup>6</sup>.

From Hall-effect measurements it is also possible to derive the density of interface traps  $D_{\text{it}}$ <sup>26,27</sup>. The results are presented in Fig. 4c (symbols). The evaluation scheme is described in the methods section. As expected, post-oxidation annealing in nitric oxide strongly reduces the density of interface traps. Moreover, these data provide an independent reconfirmation that our initial assumption which lead to Eq. (1) is valid: the  $D_{\text{it}}$  has a maximum near the conduction band edge of 4H-SiC. The solid curves represent the  $D_{\text{it}}$  distribution according to Eq. (1) with the parameters  $D_0$ ,  $D_1$ ,  $E_0$ , and  $\sigma$  extracted from 3-terminal measurements (Fig. 3) using our proposed method. The comparison to the point-by-point analysis from Hall-effect measurements displays a nearly quantitative agreement. The predictive power of our method is remarkable, as it results from a

quick 3-terminal measurement without the need of special geometries for time-consuming Hall-effect investigations. Hence, this method can be applied to vertical power MOSFET geometries as well, for which Hall-effect analysis is not applicable. Note again that the proposed method benefits from the very specific  $D_{\text{it}}$  distribution at 4H-SiC/SiO<sub>2</sub> interfaces.

## Discussion

We present a method that resolves the fundamental problem that in 3-terminal 4H-SiC n-channel MOSFET devices the charge carrier mobility is always underestimated by all available evaluation schemes (e.g., field-effect mobility or effective mobility). This underestimation stems from the negligence of interface traps which are all-important in 4H-SiC. However, their qualitative spectral distribution  $D_{\text{it}}$  is well known. It displays a strong Gaussian distribution near the conduction band edge, responsible for the soft turn-on commonly observed in 4H-SiC MOSFETs. Our model parametrizes this  $D_{\text{it}}$  by four parameters, among which two are confined within small boundaries. Using this model and taking quantum confinement into account by a self-consistent solution of the Schrödinger–Poisson equations, we precisely simulate the transfer characteristics. In turn, by fitting the parameters to measured data, our method allows an accurate determination of charge carrier mobility  $\mu$ , threshold voltage  $V_T$  and density of interface traps  $D_{\text{it}}$ . This adapted method has been successfully tested on two sets of 4H-SiC Hall-MOSFETs with drastically different  $D_{\text{it}}$  by comparing the results to Hall-effect investigations on the very same devices. We find excellent agreement between the results of these two independent methods, such that we can claim predictive power to our analysis scheme that can, however, be applied to any 3-terminal MOSFET geometry including packaged state-of-the-art power MOSFET devices.

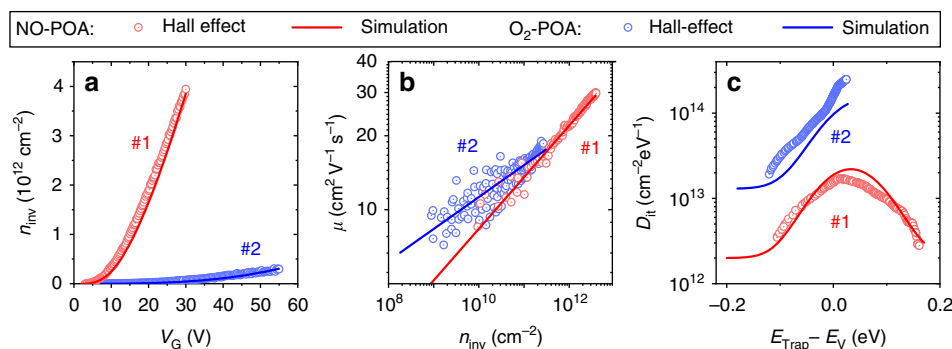
## Methods

**Experimental.** The Hall-MOSFET structures were fabricated using an industrial process. Their channel has a length of 200  $\mu\text{m}$  and a width of 32  $\mu\text{m}$ . The distance of the 4-point probes for the conductivity measurement is 100  $\mu\text{m}$ . The oxide has a thickness of 80 nm and was deposited using a PECVD process with a subsequent annealing step in different atmospheres: nitric oxide for MOSFETs with low  $D_{\text{it}}$  and oxygen for MOSFETs with high  $D_{\text{it}}$ . The p-well was formed using ion implantation with an aluminum concentration of  $[\text{Al}] = 1.5 \cdot 10^{17} \text{ cm}^{-3}$ .

All measurements were performed at room temperature using an Agilent E5270B Precision Measurement Mainframe with Agilent E5287A High Resolution SMUs connected to each sample contact. To reach quasi thermodynamic equilibrium, the transfer characteristics were recorded using a double staircase sweep with a delay that minimized the hysteresis between the two sweep directions. The magnetic field during the Hall measurements was  $\pm 0.65 \text{ T}$ . For the Hall

Sample	Method	$\mu$ (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	$V_T$ (V)	$D_{\text{it}}^{\text{max}}$ (cm <sup>-2</sup> eV <sup>-1</sup> )
#1	Field effect <sup>8</sup>	21.0	14.1	—
	Ghibaudo <sup>7</sup>	18.8	13.3	—
	Hall effect	29.4	—	$5.7 \cdot 10^{12}$
	This work	28.1	2.2	$2.8 \cdot 10^{12}$
#2	Field effect <sup>8</sup>	0.42	28.8	—
	Ghibaudo <sup>7</sup>	0.43	29.0	—
	Hall effect	17.2	—	$3.1 \cdot 10^{13}$
	This work	19.3	7.1	$1.8 \cdot 10^{13}$

To compare the different evaluation schemes, the mobility has been averaged in the gate voltage range of 27 V to 30 V for sample #1 and 50 V to 55 V for sample #2. The density of interface traps has been extracted at  $E_T = E_C - 0.1 \text{ eV}$



**Fig. 4** Benchmarking of the adapted method against Hall effect. The results of the Hall-effect investigations are shown as symbols and the simulation using the extracted parameters from the fit of the transfer characteristics is shown as solid lines: **a** charge carrier density  $n_{\text{inv}}$ , **b** charge carrier mobility  $\mu$ , and **c** density of interface traps  $D_{\text{it}}$ . For both samples, the results of our method agree well with the benchmark data obtained by Hall effect. Especially in the case of sample #2 when a high defect density at the interface is involved this is a substantial improvement compared to conventional mobility extraction schemes out of the transfer characteristics (e.g.,  $\mu_{\text{FE}}^{\text{max}} = 0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ )

measurements as well as for the conductivity measurements  $I$ - $V$  curves were recorded in the linear regime of the output characteristics. This ensures linearity between the applied current and the measured voltage. Hall constant and conductivity were then calculated from the slopes of the curves. For the evaluation of the inversion charge carrier density a Hall scattering factor of  $r_H = 1$  has been assumed. This is in agreement with previous experiments on bulk material, which determined a Hall scattering factor between  $r_{H,bulk} = 0.95$  and  $r_{H,bulk} = 1.00$  for electron transport in 4H-SiC at 300 K<sup>28</sup>.

**Simulation of the drain current.** For simulating the drain current, the following formula has been used, which includes the conductivity of the channel and the series resistance  $R_S$ :

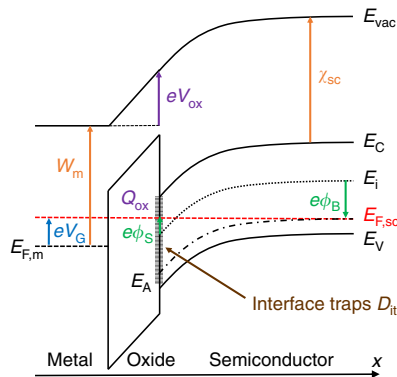
$$I_D = \left[ \left( \frac{W}{L} \cdot e \cdot n_{inv}(\phi_S(V_G)) \cdot \mu \right)^{-1} + R_S \right]^{-1} \cdot V_D, \quad (4)$$

The evaluation of Eq. (4) requires the calculation of  $\phi_S(V_G)$  and  $n_{inv}$ .

Figure 5 shows a schematic of the band bending and the relevant materials parameters with the applied gate bias  $V_G > 0$ .  $W_m$  denotes the work function of the gate metal,  $\chi_{sc}$  the electron affinity in the semiconductor,  $E_{F,m}$  and  $E_{F,sc}$  the Fermi energy in the metal and semiconductor, respectively, and  $E_A$  the acceptor level. The Fermi potential is defined as  $\phi(x) = (E_{F,sc} - E_i(x))/e$  with the intrinsic energy  $E_i(x)$  as point of reference. With this at hand, it is easy to derive the following formula for the gate voltage:

$$V_G(\phi_S) = \frac{W_m}{e} - \frac{\chi_{sc}}{e} - \frac{E_C - E_i}{e} + \phi_S + V_{ox}(\phi_S). \quad (5)$$

The voltage drop over the oxide capacitor  $V_{ox}$  can be calculated by using the charge in the semiconductor  $Q_{sc}$ , the charge trapped in interface traps  $Q_{it}$  and the



**Fig. 5** Band schematic of the metal-oxide-semiconductor capacitor

fixed oxide charge  $Q_{ox}$ :

$$V_{ox}(\phi_S) = - \frac{Q_{sc}(\phi_S) + Q_{it}(\phi_S) + Q_{ox}}{C_{ox}}. \quad (6)$$

The interface trapped charge  $Q_{it}$  is obtained by integration of the parametrized  $D_{it}$  (Eq. 1) over the trap energy. The typical approach is to introduce a neutral level  $E_n$ , where all interface defects above  $E_n$  add a negative charge to the interface when occupied and all interface defects below  $E_n$  add a positive charge to the interface when unoccupied. Those defects are often referred to as acceptor-like and donor-like, respectively.  $Q_{it}$  was calculated as follows:

$$Q_{it}(\phi_S) = e \int_{-\infty}^{E_n} \frac{D_{it}(E)}{1 + 2 \cdot \exp\left(\frac{-\Delta E(\phi_S)}{k_B T}\right)} dE - e \int_{E_n}^{\infty} \frac{D_{it}(E)}{1 + \frac{1}{2} \cdot \exp\left(\frac{\Delta E(\phi_S)}{k_B T}\right)} dE. \quad (7)$$

For the multiplicity of the states involved, we opted for a consistent description for both cases. Since the exact degeneracy of the states is not known, we assumed a value frequently used for donor-like defects for all interface traps. This seems natural because the important interface traps for the performance of the devices are energetically close to the conduction band edge. It leads to the factor 2 in the case of unoccupation and to the factor 1/2 in the case of occupation in Eq. (7). Note that the evaluation results remain essentially unaffected upon a different choice of multiplicities. For the calculation of  $Q_{sc}(\phi_S)$  see the next paragraph.  $\phi_S(V_G)$  is obtained by numerical inversion of Eq. (5).

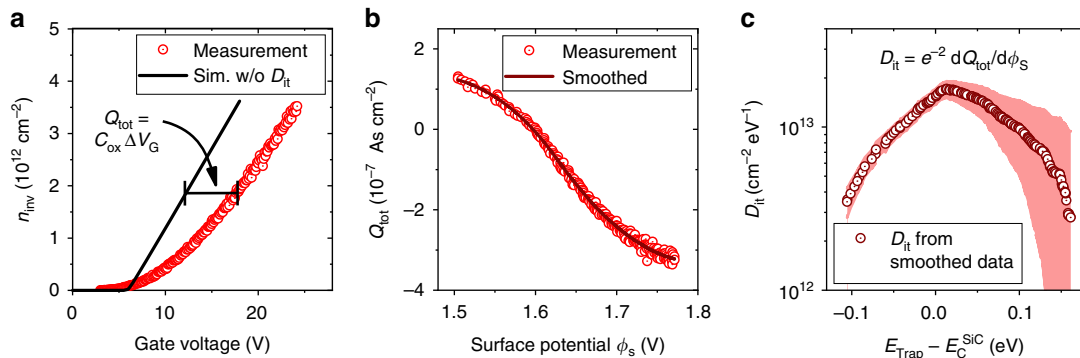
To calculate  $n(\phi_S)$  and  $Q_{sc}(\phi_S)$  two methods were used. The first one is the charge sheet model for silicon carbide proposed by Arnold<sup>20</sup>. It's a semiclassical model, where both relations are calculated by integration over the space charge region. The second method used employs the Schrödinger–Poisson solver of Snider et al.<sup>21,22</sup> to simulate the band bending and the ground states of the 2D sub-bands in the inversion channel. For the calculation of the total charge in the semiconductor  $Q_{sc}(\phi_S)$  the electron charge density, the hole charge density and the charge density of ionized dopants are integrated over the space charge region. The surface Fermi potential  $\phi_S$  is given by  $(E_F - E_i)/e$  at the interface. The inversion charge carrier density  $n_{inv}$  is calculated by integrating the electron density over the inversion channel.

**Evaluation of the density of interface traps from Hall-effect investigations.**

Figure 6 shows the evaluation of Hall-effect measurements obtained on sample #1 as example. In Fig. 6a the measured inversion charge carrier density  $n_{inv}$  is plotted and compared to the SPS-simulated  $n_{inv}$  for an ideal MOSFET with identical parameters, but without fixed oxide charge  $Q_{ox}$  and interface traps  $D_{it}$  (black solid curve). A point-by-point analysis of the gate voltage difference  $\Delta V_G = V_{G,ideal} - V_G$  delivers the total trapped charge  $Q_{tot}$  as a function of  $n_{inv}$  with

$$Q_{tot} = Q_{ox} + Q_{it}(\phi_S) = C_{ox} \cdot \Delta V_G. \quad (8)$$

The surface Fermi potential  $\phi_S$  is calculated by inverting the result for  $n_{inv}(\phi_S)$  from the Schrödinger–Poisson solver discussed in the previous section. While  $Q_{ox}$  is independent of the surface Fermi potential  $\phi_S$ , the interface trapped charge  $Q_{it}$



**Fig. 6** Evaluation of the density of interface traps  $D_{it}$  from Hall-effect measurements. The  $D_{it}$  in **c** is derived from the deviations of the Hall-effect data from the simulation assuming no  $D_{it}$ . The measurement error can be read off the weak scatter of the measurement data in **a** and **b**, resulting in the shaded error margin in **c**



varies with  $\phi_s$ . This gives access to the density of interface traps (Fig. 6c):

$$D_{it} = \frac{1}{e^2} \cdot \left| \frac{dQ_{it}}{d\phi_s} \right| = \frac{1}{e^2} \cdot \left| \frac{dQ_{tot}}{d\phi_s} \right|. \quad (9)$$

The surface Fermi potential is linked to the energy position of traps in the bandgap by  $\phi_s = (E_F - E_{it}^{interface})/e$  with  $E_{it} \approx E_F$ .

### Data availability

The data that support the findings of this study are available from the corresponding author upon request.

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### Author contributions


M.H., H.B.W., and M.K. designed research; M.H. J.L., G.P., H.B.W., and M.K. performed research; G.P. provided samples; M.H. analyzed data; M.H., H.B.W., and M.K. wrote the manuscript.

### Additional information

**Competing interests:** The authors declare no competing interests.

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