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Highly stretchable graphene nanoribbon springs by programmable nanowire lithography

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Graphene nanoribbons are ideal candidates to serve as highly conductive, flexible, and transparent interconnections, or the active channels for nanoelectronics. However, patterning narrow graphene nanoribbons to <100 nm wide usually requires inefficient micro/nano fabrication processes, which are hard to implement for large area or flexible electronic and sensory applications. Here, we develop a precise and scalable nanowire lithography technology that enables reliable batch manufacturing of ultra-long graphene nanoribbon arrays with programmable geometry and narrow width down to ~50 nm. The orderly graphene nanoribbons are patterned out of few-layer graphene sheets by using ultra-long silicon nanowires as masks, which are produced via in-plane solid–liquid–solid guided growth and then transferred reliably onto various stiff or flexible substrates. More importantly, the geometry of the graphene nanoribbons can be predesigned and engineered into elastic two-dimensional springs to achieve outstanding stretchability of >30%, while carrying stable and repeatable electronic transport. We suggest that this convenient scalable nanowire lithography technology has great potential to establish a general and efficient strategy to batch-pattern or integrate various two-dimensional materials as active channels and interconnections for emerging flexible electronic applications.

INTRODUCTION

The outstanding electronic transport,[1] mechanical,[2] and optical properties[3] of graphene have made it an ideal candidate for constructing flexible and transparent electronics, detectors and biosensors.[4–10] In order to be integrated into planar circuitry, as conductive interconnections[11–13] or active channels, the graphene film has to be patterned into narrow ribbons with controlled width and precise spatial arrangement.[14–17] Usually, graphene nanoribbons (GNRs) of tens of nanometers wide are etched out of graphene monolayer, by using sophisticated electron beam lithography (EBL),[18] which is unfortunately too expensive to implement for large-scale flexible electronics. In contrast, self-assembly GNRs can be synthesized from molecules in solution environment,[19,20] by unzipping multi-walled carbon nanotubes[21] or by reducing graphene oxide flakes,[22] which provide promising approaches to fabricate nearly perfect GNR segments.[23,24] However, these self-assembled GNRs are usually short and randomly oriented, and achieving a precise location controls of these tiny segments remains still a formidable challenge. Recently, Al_2O_3 nano belts, formed at the step edges of graphene stacks, have been utilized to serve as nano-stripe masks for multilayer GNR patterning.[25] But this approach strongly relies on the initial positions of graphene stack edges, and the distribution and geometry of the as-produced GNRs are thus limited to discrete concentric ribbon circles.[25]

In parallel, tailoring the geometry of GNRs into elastic forms[26–29] has been recognized as the key to gain extra stretchability for the rigid graphene, which is rather flexible but not much stretchable. The maximum tolerable strains of graphene sheets, reported in the literature, ranges from 1 to 3%.[30–34] GNRs are of the same nature, but can be engineered into two-dimensional (2D) zigzag, serpentine springs,[8,29,30] or even 3D wrinkles.[26,27] Attaching straight GNRs to pre-strained polymers has been used to enforce a 3D out-of-plane buckling to achieve a high stretching up to 30%.[26] While the 3D buckling is convenient to implement, it kills also the precision control over the wrinkle formation. This poses a limitation for the 3D GNR wrinkles to be incorporated into more advanced integration circuitry, where a full planar processing compatibility is necessary. Meanwhile, designing 2D zigzag or serpentine GNR springs is also subject to a geometric constraint, that is the ratio of the bending radius over the GNR width, $g \equiv R_{bend}/D_{GNR}$, which has to be large enough (typically >20) to avoid local strain concentration effect (that will otherwise cause cracking).[35,36] In large-area electronics, the channel lengths of field effect thin film transistors (FETs or TFTs) are usually of $L_{ch} = 2$–3 μm.[35] Considering $R_{bend} \leq L_{ch}/2$, the ideal GNR channel width should be only $D_{GNR} < \frac{L_{ch}}{2g} \sim 100nm$, which is unfortunately far beyond the capacity of conventional lithography.

In this work, we propose and demonstrate a readily scalable and yet precise nanowire lithography (NWL) strategy, where ultra-long and orderly silicon nanowires (SiNWs), produced via a guided in-plane solid–liquid–solid (IPSLS) growth,[37–45] are transferred onto the monolayer or few-layer graphene sheet to serve as nano shadow masks. By this way, very thin GNRs of $D_{GNR} \sim 50$ nm can be reliably patterned over the large area wafer or flexible polymer substrates, with a programmable layout and geometry. Though NWL technology has been first explored by using masks of

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relatively simple, straight, and random SiNWs[46] grown via vapor–liquid–solid (VLS) mechanism,[47] or by printing organic nanowires via sequential electrohydrodynamic approach,[48,49] our approach represents indeed a higher level of manipulability and a new capability to efficiently batch-manufacture periodic ultra-long GNR array with pre-designable elastic line-shapes to achieve a largely enhanced stretchability >30%.

RESULTS

Nanowire mask fabrication and transferring

To carry out a NWL of GNRs into predesigned geometry of straight, bending, and even serpentine line-shapes, as depicted in Fig. 1a, the SiNW masks were firstly produced via an in-plane guided IPSLS growth.[38,39,41,43,45] The guiding edges are first etched in the wafer or glass substrates coated with a 500-nm SiO$_2$ layer, by lithography and inductively coupled plasma (ICP) etching, as illustrated schematically in Fig. 1c, which is followed by the deposition of indium (In) stripes lying crossing to the guiding edge lines at the ends. After H$_2$ plasma treatment in a plasma enhanced chemical vapor deposition (PECVD) system at 350 °C, the surface oxide of the In stripes were removed to allow the diffusion and agglomeration of In atoms into discrete droplets. Then, a thin precursor layer of hydrogenated amorphous Si (a-Si:H) was deposited at 150 °C by silane plasma to cover the whole sample surface (Fig. 1d). After that, In droplets were activated to move during an annealing in vacuum at 350 °C, by absorbing the a-Si:H layer to produce crystalline SiNWs behind. During this course, the extra a-Si:H coated on the vertical sidewall of step edges can help to attract the In droplet,[44,50,51] and thus lead them into a precise guided growth to produce in-plane SiNWs with designable geometries. The scanning electron microscopy (SEM) images of the as-grown SiNWs, following the guiding step edge lines, are shown in Supporting Information Fig. S1. At the end, the remnant a-Si:H layer were selectively etched off by using H$_2$ plasma at around 120 °C. Then, the samples were unloaded from PECVD and spin-coated with a thin PMMA layer, followed by immersing the samples in diluted HF solution to dissolve the underlying oxide layer and release the PMMA layer that holding the SiNWs. The floating PMMA pieces were collected and transferred onto graphene sheets on SiO$_2$/wafer or PDMS substrates. The graphene layers were obtained via exfoliation from bulk graphite or CVD growth on copper thin films (see the Methods section for more experimental details). At last, GNRs were etched out of the graphene sheets by a SiNW-masked oxygen (O$_2$) plasma etching. The remnant SiNWs can be removed later by dissolving the intermedium PMMA layer in acetone solution.

GNRs patterning and field-effect transistors

Figure 2a shows a photo image of an exfoliated graphene sheet on the SiO$_2$/Si substrate, where Ti(5 nm)/Au(50 nm) patterns were first fabricated upon the graphene to serve as Source (S) and Drain (D) electrodes and then spinning PMMA (~70 nm) for protection. After transferring a parallel array of SiNWs onto the graphene sheet, lying perpendicular to the electrodes (Fig. 2b), the exposed graphene layer and PMMA were selectively etched off by using O$_2$ plasma with the top SiNWs serving as the shadow masks, as seen in Fig. 2c. Finally, the SiNWs were removed (Fig. 2d), while the protected GNR segments can be clearly identified by atomic force microscopy (AFM) characterizations, as seen for example in the inset of Fig. 2d, where the GNR width is found to be D_{GRN} ~ 90 nm. According to the Raman spectra of the pristine graphene and the etched GNRs, as shown in Fig. 2e, f, respectively, the typical Raman peaks of bilayer graphene, featuring a relatively lower 2D peak compared with the G-band peak, are preserved in the etched GNR stripes, indicating that the NWL etching did not damage or modify the structural properties of the protected nano-sized segments.

Furthermore, the transport properties of the bilayer GNRs are also measured, in a bottom-gated field-effect transistor (FET) configuration, and shown in Fig. 2g. The channel current, with constant source–drain bias of V_{ds} = 0.1 V, can be effectively modulated by the gate voltage (V_g), where the Dirac point is located at V_{Dirac}~32V. Taking the bottom SiO$_2$ dielectric layer thickness of 285 nm, an average GNR channel width of D_{GNR} ~ 100 nm, the extracted carrier mobility in the GNRs is ~600 cm^2/Vs, which compares reasonably to the reported GNR FETs with similar channel width fabricated by EBL lithography.[52]

Dimension controls and bandgap engineering

Diameter of the GNRs has been a crucial parameter to tailor their properties, and an important way to open bandgap in the narrow GNR channels.[19,53] Obviously, the width of GNR can be tuned directly by choosing SiNW masks of different diameters, which can be controlled, shown in our previous work.[38,39,41,54] They are easily adjusted by the size of the leading catalyst droplets and the feeding balance condition during an in-plane growth. Figure 3a shows the evolution of the etched GNRs (see the AFM images presented in Fig. 3b as examples), against the diameter of the SiNW masks. The GNR width is found to scale linearly down to ~40 nm while choosing thinner SiNW masks and different plasma etching duration. It is worth noting that the etching duration also plays an important role in controlling the width of the as-produced GNRs. For instance, the produced GNRs with a longer etching duration of t = 60 s are found to be, on average, 40% thicker than those obtained with a shorter etching time of t = 30 s, which can be fitted by the linear scaling laws of D_{GNR} ~ 0.92D_{NW} and D_{GNR} ~ 0.67D_{NW} as noted in Fig. 3a, respectively.

To testify the tailoring capability of opened bandgap in the NWL-etched GNR channel, a FET device was fabricated with a single GNR channel, which was etched out of a monolayer graphene (as inferred from the Raman peaks in Fig. 3c), with a typical AFM image shown in the inset of Fig. 3d. For the as-produced GNRs, several pronounced Raman peaks can be observed, including the D band (~1340 cm^{-1}), G band (~1590 cm^{-1}), and 2D band (~2670 cm^{-1}). Meanwhile, the broad but relatively weaker peak appeared at ~2200 cm^{-1} is not considered as related to the GNR, as this peak was not consistently observed for the other GNRs with similar widths, as seen for example in Fig. S3. Instead, it could arise from the occasional contamination or impurities on the substrate around this specific GNR. The average width of this specific GNR is found to be around D_{GNR} ~5 nm. Under V_{ds} = 0.5 V bias at room temperature, the transport property reveals a significantly enhanced current on/off ratio up to 270, compared with the modulation factor of only 2–3 in the wider double-layer GNRs (see Fig. 2g). The linear output curves in Fig. 3e indicate also an Ohmic contact between the GNR channel and the S/D electrodes. This observation can be considered as a clear sign of opened bandgap in the narrow GNR channel due to the lateral confinement effect,[53] highlighting the capability of the NWL technology in defining the ultrathin channel width, without the need of elaborated EBL etching.

Geometry design of ultra-long GNRs

Due to the precise growth routine control of the in-plane SiNWs,[45] the geometry of the GNRs can be predesigned in a programmable way. To demonstrate this unique capability of NWL technology, the SiNWs are first grown into more complicated wire patterns, for example, the double-line patterns of "NJU", the abbreviation of Nanjing University, as schematized in Fig. 4a. The dark-field optical and SEM images of the engineered SiNW-letters, composed of continuous ultra-long SiNWs with length of > 300 μm, are shown in the upper and the middle panels in Fig. 4d, which are transferred to place upon a CVD-grown graphene film on flexible PDMS substrates later (see the Methods section for more
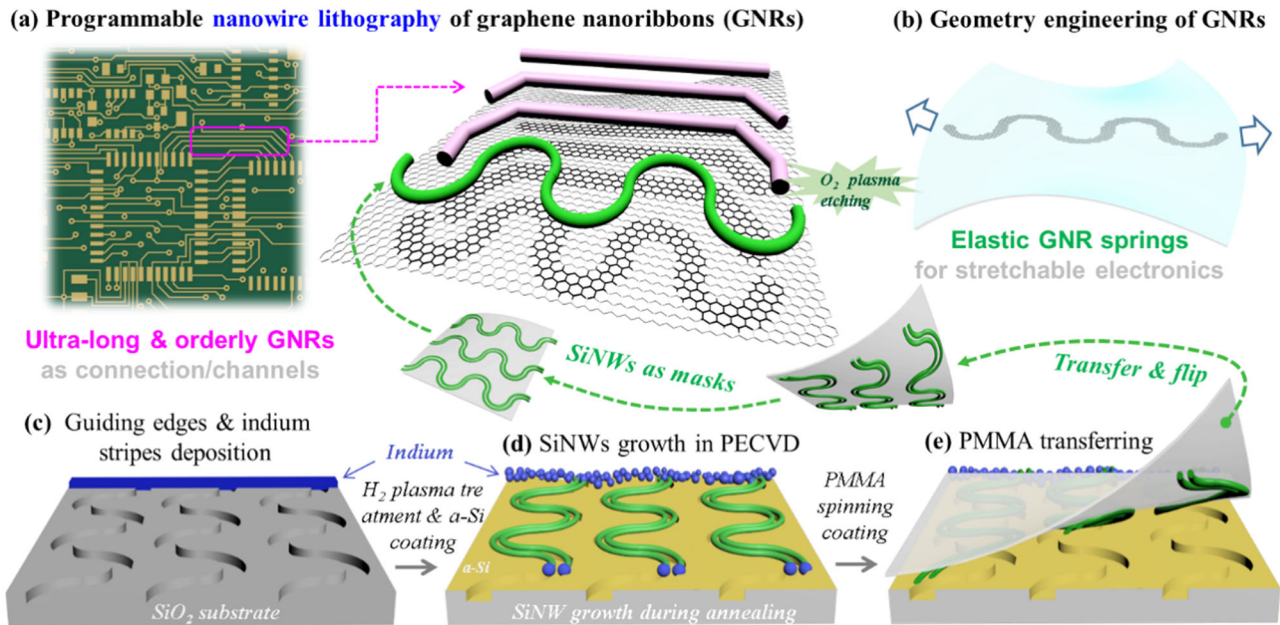
Fig. 1 Graphene nanoribbons (GNRs) fabrication via nanowire transfer and lithography. **a** illustrates schematically the NWL patterning of a single graphene sheet into parallel channels or elastic serpentine spring; the in-plane growth of silicon nanowires involves first (**c**) the guiding edge patterning and indium (In) catalyst strip deposition on the SiO$_2$/Si substrate, then (**d**) H$_2$ plasma treatment to form catalyst droplets (at 250 °C), amorphous Si precursor coating (at 150 °C) and annealing growth (at 350 °C); **e** depicts schematically the transferring of the as-produced SiNWs by spin-coating a thin layer of PMMA on the sample surface, and then detaching and flipping them to serve as nanowire mask for subsequent GNRs patterning
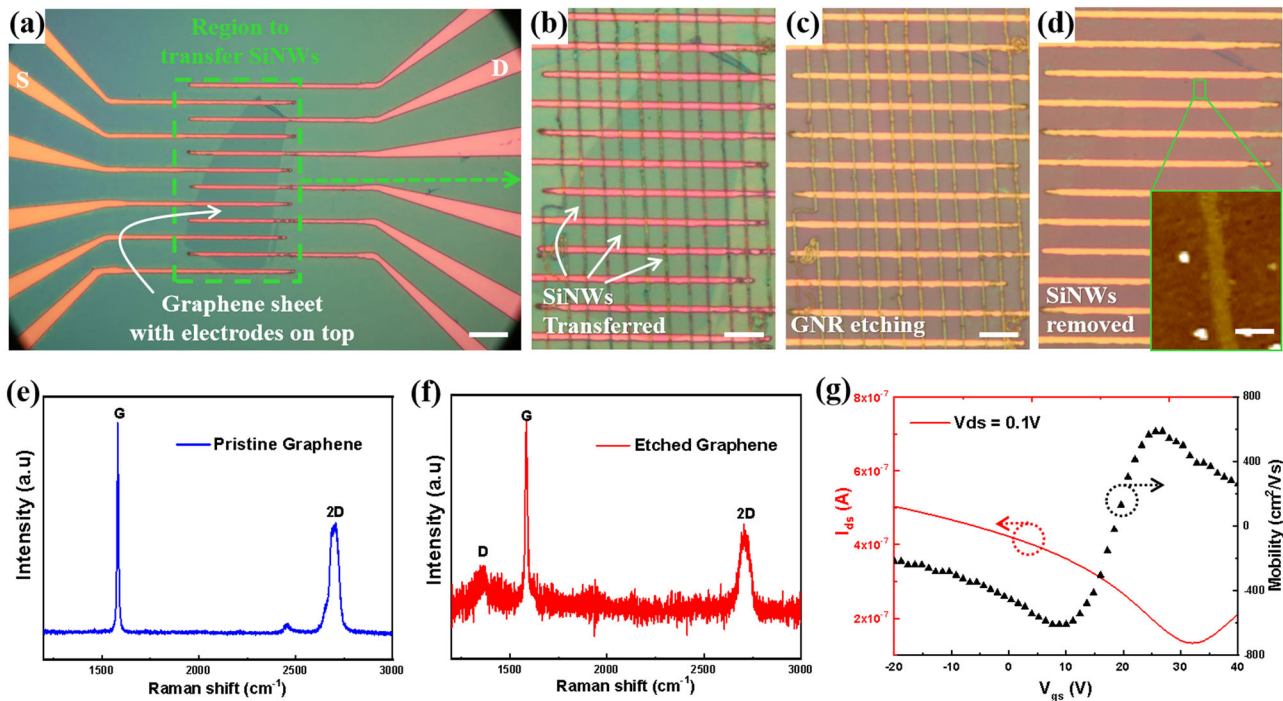

Fig. 2 GNR field-effect transistors (FETs) fabricated by nanowire lithography. **a** Photo image of an initial bilayer graphene sheet placed on the top of the SiO$_2$-coated wafer substrate and contacted by Ti/Au electrode fringes on the top and colorful due to the PMMA. **b**–**d** show the images after SiNW array transferring, oxygen plasma etching, and the removal of SiNWs, respectively. The inset of (**d**) shows the atomic force microscope image of the GNR segment in the region marked by a green rectangle in (**d**). Scale bar in (**a**) stands for 20 μm, while those in (**b**–**d**) are 10 μm, and that in the inset of (**d**) is for 200 nm. The Raman spectra of the pristine graphene and the etched GNRs are shown in (**e**, **f**), respectively, while (**g**) presents the transfer property and the extracted mobility curve of the GNR-FET device
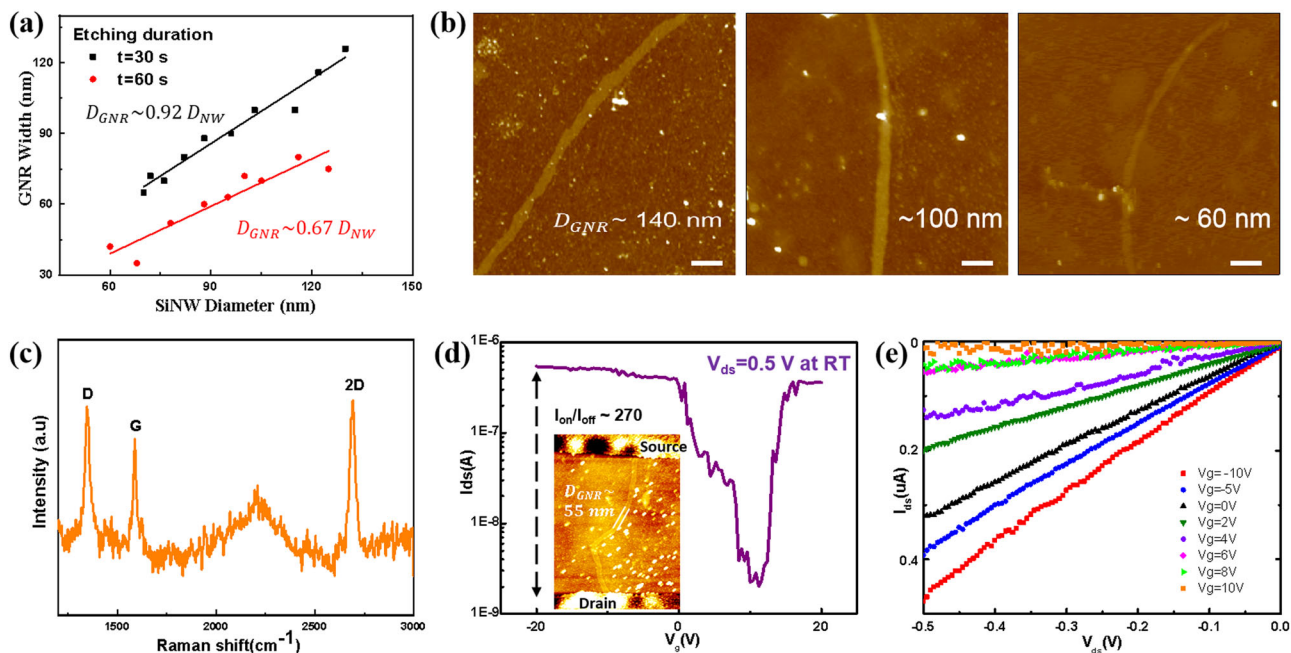
Fig. 3 Width control and electronic transport of ultra-thin GNRs. **a** Statistics and linear fittings from the evolution of the etched GNR widths with the diameters of masking SiNWs, with different plasma etching durations. **b** AFM images of GNRs with decreasing width (from left to right) produced by the SiNW lithography and etching. Scale bars are all for 200 nm. **c** Raman spectrum of the GNR etched out of a monolayer graphene sheet. **d**, **e** show the transport and output properties of a FET device fabricated by a single GNR channel, with a typical AFM image shown in the inset of (**d**)
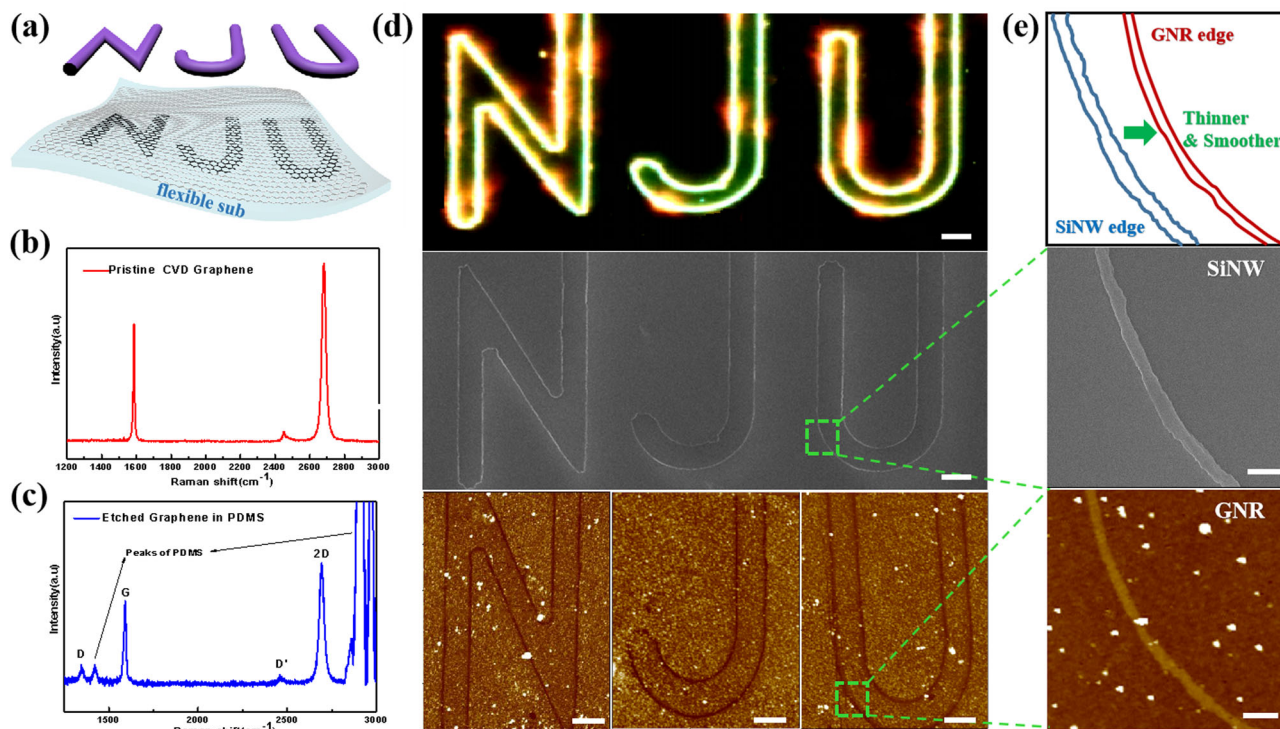

Fig. 4 Programmable geometry engineering of GNRs. **a** Schematic illustration of the transferring of programmed SiNWs to serve as the masks for etching GNRs into predesigned patterns on the soft PDMS substrate. **b**, **c** compare the Raman spectra of the pristine CVD-grown monolayer graphene sheet, transferred to PDMS sheet, before and after NWL plasma etching. **d** showcases the capability of NWL patterning to define continuous GNRs (on the wafer substrate) that form the double-line strokes of Nanjing University's abbreviation letters of "NJU", where the upper and the middle panels present the optical and SEM images of the SiNW-letters, while the bottom panel shows the AFM images of the GNR-letters. Scale bars in (**d**) are all for 2 μm. **e** provides a close scrutiny of the bending SiNW and GNR segments in the left-bottom corner of letter "U", and highlights the smoothing and thinning effects of the relatively rougher and wider SiNW, compared to the as-produced GNR part, during the NWL geometry transferring. Scale bars: 200 nm

experimental details for the CVD growth of graphene and transferring procedures). According to the Raman spectra of the pristine graphene and the etched GNRs (on PDMS), the graphene sheet and the GNRs are of monolayer. The final GNR-letters of "NJU" are also measured with AFM and presented in the lower panels of Fig. 4d. Interestingly, the etched GNR segment at the bending corner of letter "U" has a smoother and thinner edge profile compared with its SiNW mask, as witnessed more clearly in the highlighted edge-line comparison in Fig. 4e. This is indeed advantageous in order to reduce the impact of the edge roughness of SiNWs during their geometry transformation into GNRs. Meanwhile, it is worthy to note that, though NW lithography has been demonstrated by using VLS-grown SiNWs as masks,[46] the NWs are mostly straight, shorter and randomly placed, and thus the same for the produced GNRs. This could be a fundamental limitation for their large-scale device applications, where precise geometry, location and routine controls of the GNRs are necessary. In contrast, the programmable geometry control of the ultra-long GNRs demonstrated here boasts a much higher level of manipulability and spatial precision, which are

indispensable for building reliable and scalable deployment of various GNR-based applications.

Highly flexible GNR springs
A straightforward application of the geometric engineering capability is to batch-manufacture orderly arrays of GNR springs, via a procedure diagrammed schematically in Fig. 5a–g. Specifically, a monolayer graphene sheet was first grown by precipitation upon a copper (Cu) substrate in the CVD system, which was then contacted by Au electrodes, covered with a spin-coated PMMA layer and transferred to the soft PDMS substrate (Fig. 5a–d). After that, SiNW springs were grown and placed upon the PMMA/electrode/graphene (Fig. 5e). The optical microscope images of the transferred SiNW springs upon rigid SiO_2-coated wafer or soft PDMS substrates are provided in Supplementary Fig. S3. Then, a plasma etching was applied to transfer the elastic geometry directly onto the bottom graphene layer to produce 2D GNR springs, as seen for example in the optical microscope image presented in the top inset of Fig. 5f. Note that, for this specific
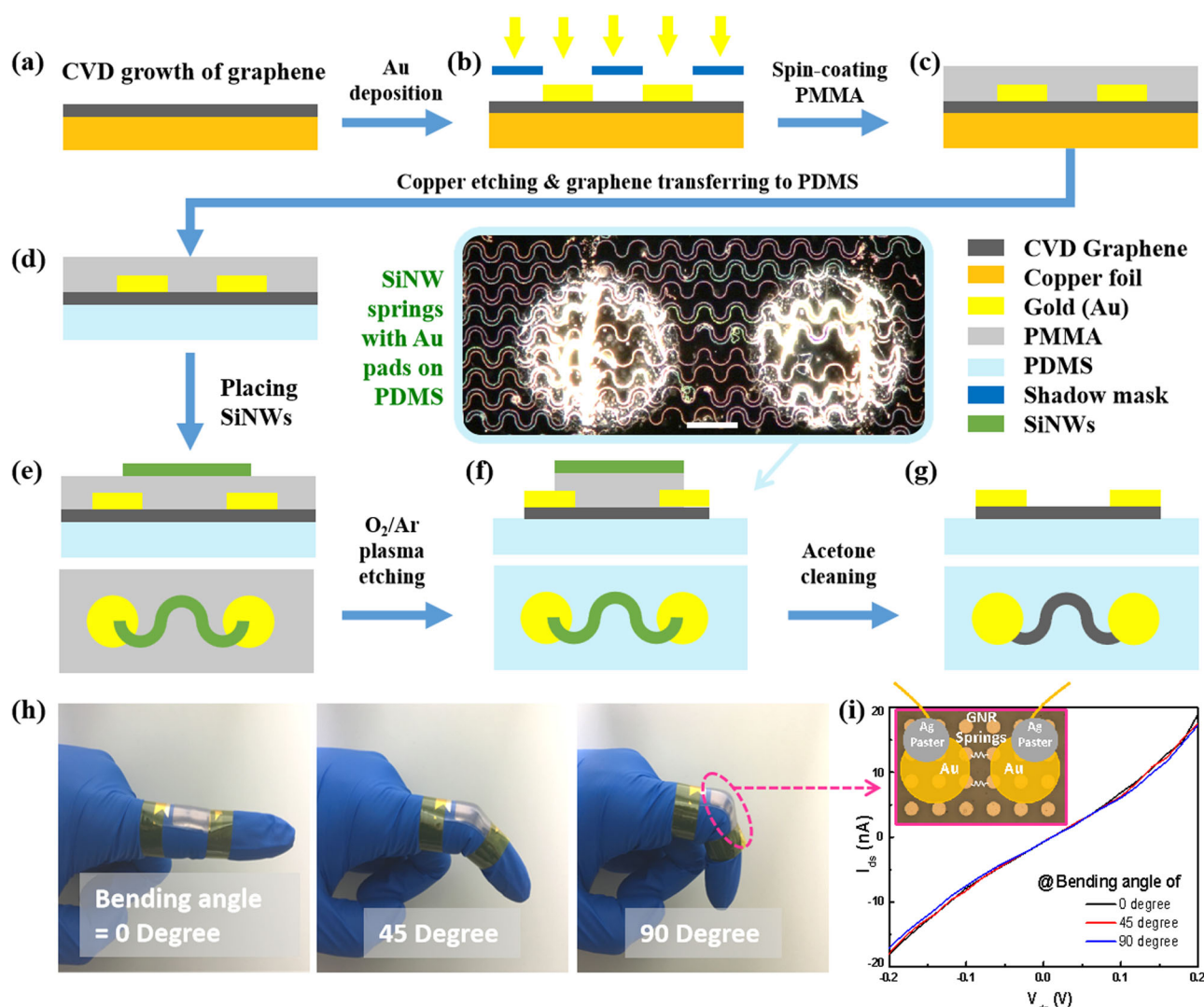

Fig. 5 Highly flexible GNR springs on PDMS. **a–d** illustrate schematically the CVD growth of graphene, electrode deposition and transferring of the graphene to soft PDMS substrate, which is followed by (**e**) positioning NW springs on top and (**f**) plasma etching to form SiNW/PMMA/GNR springs, as seen for example by the photo image in the top inset of (**f**). Scale bar: 40 μm. Finally, the SiNW masks and the PMMA layer are cleaned off by acetone to preserve only GNRs and electrodes, as depicted in (**g**). **h** shows a series of snapshots of GNR springs on PDMS attached to finger knuckle, bending to 0, 45, and 90°, while the corresponding measured current–voltage curves are shown in (**i**) with an inset illustrating the electrode layout and connections schematically

electrode configuration, there are usually 12–14 GNR springs found between the Au electrodes. At the end, the SiNWs together with the PMMA layer can be cleaned easily by an Acetone rinsing (Fig. 5g).

In order to test the flexibility of the tailored GNR springs, the PDMS sample with patterned GNR arrays was attached to finger knuckle and fixed at the two ends by conductive tapers, as seen in the photo images in Fig. 5h. The electrode connection configuration has been illustrated in the inset of Fig. 5i, where two Au/silver (Ag) paster pads are connected by 2–3 GNRs with a separation of ~50 µm. Remarkably, the current–voltage (IV) curves remain basically the same, as shown in Fig. 5i, even under large knuckle bending to 90°. More details of the IV characteristics measured under different bending angles are plotted in Supplementary Fig. S4a, while the evolution of the extracted GNR channel resistances during a complete bend-and-release cycle is shown in Fig. S4b. In addition, the bending stability of the GNR channel is also tested by recording the transport currents at 1V bias under repeating bending to 0, 45, and 90° (Fig. S4c), indicating a robust electric connection and high flexibility of the GNR spring channels.

Stretchability testing of GNR springs

In order to investigate the actual strains and deformations of the GNR spring channels, as well as the impact of strain on their electronic transport, the GNR springs/PDMS samples were subject to different coplanar stretching strains, and the IV curves are recorded and shown in Fig. 6a. It is interesting to see that, under stretching strain up to 25%, the transport currents still changed only slightly (<10%). The resistances of the GNR springs, which are extracted under difference strains and shown in Fig. 6b, are found to fluctuate around a narrow range of 70 ± 5 kΩ. Therefore, for this specific sample, there is no clear sign of piezo-resistance effect in these GNR samples, at least within the stretching extent up to 30%. Meanwhile, it is also critical to point out that, the stretching strain reported here was determined directly by measuring the channel length variation observed under the microscope. Though the GNR springs are invisible under optical microscope, in order to provide a straightforward impression of the local channel deformation, a series of photo images have been taken and displayed in Fig. 6d for the samples where the top SiNW masks are intentionally preserved to reveal how the spring channels can adapt to elongated stretching. However, all the experimental data
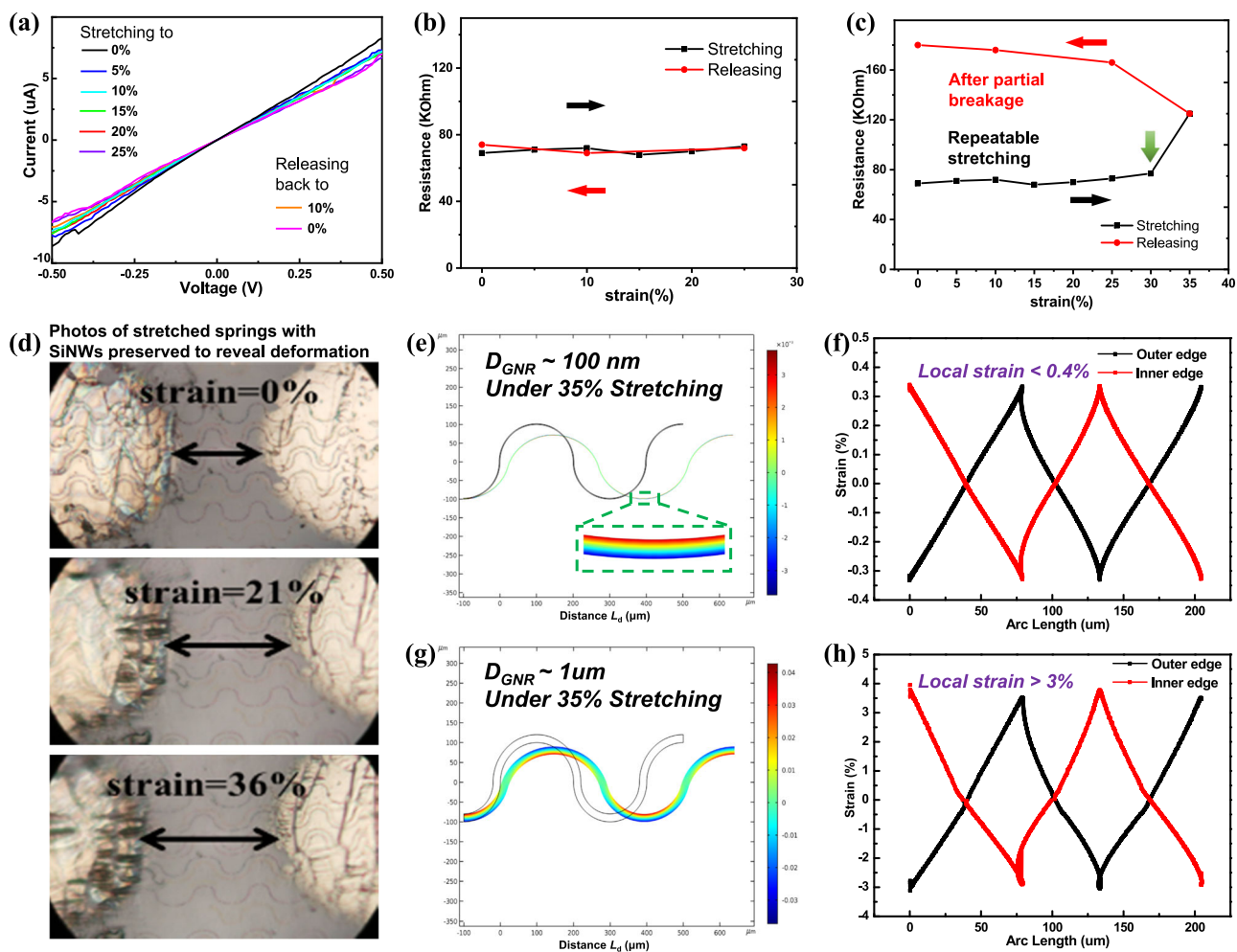
Fig. 6 Stretching tests of the geometry-engineered GNR springs. **a** shows the current–voltage (IV) characteristics of the GNR springs under different stretching strains. **b** presents the stable GNR springs' resistance under repetitive stretching to 25% and releasing back, until partial but permanent breakage happens, as witnessed in (**c**), when the stretching arrives at 35%. The photos in (**d**) are captured on a reference sample, where the SiNW masks are intentionally preserved, over (but not connected to) the GNRs, to showcase the spring channels' deformation under different stretching strains. Finite element simulations of the strain distributions in the stretched GNR springs, with a channel width of 100 nm or 1 µm, are shown in (**e**, **g**), respectively, while the local strains along the channel edges are extracted and displayed in (**f**, **h**)

of the stretched IV and resistance variations, as presented in Fig. 6a–c, were measured from the samples with only GNR spring channels (that is, the top SiNWs had been completely removed). The relatively constant channel resistance of the GNR springs can persist up to 30% stretching, as marked in Fig. 6c by the green arrow. After that, a partial but permanent breakage happened under further stretching to 35% strain, accompanied with an increase of the GNR channel resistance by ~130%, which can be assigned to the loss of part of the GNR spring connections.

DISCUSSION

Compared with the reported stretchability in the literature for various graphene nanostructures, as summarized in Table 1, which includes flat sheet, straight ribbons, 2D serpentine or zigzag springs, or 3D wrinkles, the 30% stretchability of the GNR springs accomplished here by NWL represents indeed a new record for all the planar graphene nanostructures. The maximum stretchability of rigid graphene sheet or straight nanoribbons has been limited to a range of 0.4–6%.[21,29–34,55] Patterning the graphene sheet into 2D GNR springs with a thick channel width of 20 μm extends this limit to around 10%.[56] Further elasticity improvement (to 30%[26]) can be obtained by the formation of out-of-plane 3D graphene wrinkles on pre-strained PDMS layers,[26,27] which is, however, not fully compatible to high-density planar circuit integration. Meanwhile, it is noteworthy that there is no clear sign of wrinkle formation on the GNR spring channels upon the PDMS substrate, as confirmed by optical microscopy observation and AFM characterization of the sample surface after stretching, see Fig. S5 for the typical AFM scanning images. The superior stretchability achieved here can be assigned to the unique capability of SiNW lithography to fabricate high-quality GNRs with elastic geometry and ultra-thin channel width (D_{GNR} = 50–100 nm). For example, as shown in Fig. 6e, finite element simulation (@COMSOL suite) of the strain distribution in a stretched GNR spring reveals that, for the NWL-fabricated GNR springs with a channel width of D_{GNR} ~10 nm and local bending radius of R_{bend} = 5 μm, 35% pulling strain can be very well accommodated by the elastic spring geometry. The maximum tensile (or compressive) strain found at the outer (or the inner) edge of the strained GNR is only 0.35% (see Fig. 6f), which is far below the fracture limit of graphene (of 2–6%[21,32–34,55]). In comparison, if the GNR width is increased to 1 μm, the local strain maxima will quickly increase by an order of magnitude to ~3% (Fig. 6g, h). Therefore, achieving a high geometric factor of $g = \frac{R_{bend}}{D_{GNR}} gt$ 50, as demonstrated in this work, has been the key to fabricate highly stretchable GNR spring channels. Importantly, these have been accomplished in a fully planar architecture, via a salable and low-cost manufacturing, making them ideal candidates to explore advanced stretchable electronic and sensor applications.

In summary, a novel nanowire lithography (NWL) strategy has been developed here to achieve an efficient, scalable, and precise nano-patterning of orderly graphene nanoribbons (GNRs) with controllable diameter down to 50 nm, which can be transferred and deployed reliably upon soft polymer substrates. Thanks to the capability of the geometry design, the GNRs can be predesigned and engineered into elastic 2D springs to achieve an outstanding stretchability up to 30%. This convenient NWL technology thus holds a strong promise to establish a general strategy for integrating various nano-channel patterns of 2D materials for developing flexible/stretchable electronics and sensors.

METHODS

SiNW masks preparation

The SiNWs were grown upon oxide-coated Si wafers or glass substrates, via an IPSLS growth mechanism, where a hydrogenated amorphous Si thin film is deposited upon a substrate surface to serve as the precursor layer, which is absorbed by In catalyst droplets to produce crystalline SiNWs. Specifically, (1) upon SiO$_2$/wafer or glass substrates, guiding step edges with predesigned geometry were defined by photolithography and etched into the SiO$_2$ layer by using ICP to a depth of 90~150 nm; (2) In stripes of nominally 10 -nm to 30 -nm thick and 2–3 -μm wide were deposited by thermal evaporation and lift-off procedure at the starting ends of guiding edges. The crossing points between the In stripes and the guiding lines defined the starting points for the growth of in-plane SiNWs; (3) then, the samples were loaded into a PECVD system, and subject to a H$_2$ plasma treatment at 300 °C, with SiH$_4$ gas flow rate, chamber pressure and RF power density of 13 SCCM, 140 Pa, and 125 mW/cm^2, respectively, for 1–3 min. During this course, the surface oxide of In stripes was removed and the droplets were allowed diffuse and agglomerate into separated nanoparticles; (4) After decreasing the substrate temperature to 150 °C, an a-Si thin film was deposited below the melting point of In, with 2 SCCM pure SiH$_4$ plasma, with 20 Pa pressure and 20 to 60 mW/cm^2 power density, for 2 min to 4 min; (5) when the substrate temperature was raised to 350 °C and kept in vacuum for 30–60 min, the In droplets started to grow by converting the a-Si layer into crystalline SiNWs; (6) the extra a-Si on the vertical sidewall of the guiding steps or grooves can help to attract the In droplets to move along and produce SiNWs with programmable geometry. At the end of the SiNW growth, the remnant a-Si layer can be selectively removed by using H$_2$ plasma etching at 180 °C.

CVD growth of graphene sheet

Monolayer graphene sheets were grown on copper foil by chemical vapor deposition. A piece of 25 μm-thick copper foil (99.8%, Alfa-Aesar) was heated to 1030 °C under hydrogen flowing at 100 sccm (400 mTorr) in a 3-inch-wide tubular quartz reactor for 30 min. Then a gas mixture of hydrogen (100 sccm) and methane (20 sccm, 420 mTorr) was introduced

Table 1. A comparison of the values of stretchability reported in the literature for various graphene sheets to that achieved in this work

No.	Graphene patterns	Substrate	Graphene width [μm]	Lithography	Max stretch [%]	Refs.
1	2D spring ribbons	Mica	2	UVL	0.37	[29]
2	Sheet	PDMS	>100	UVL	1	[30]
3	Ribbons	Suspend	20–50	EBL	1.5	[31]
4	Sheet	PDMS	20–50	UVL	2	[34]
5	Ribbons	Suspend	1.5–4	EBL	3	[32]
6	Ribbons	PDMS	0.1	EBL	3	[33]
7	Ribbons	PDMS	20	UVL	4.5	[55]
8	Sheet	PDMS	>100	–	6	[21]
9	2D springs	PET	20	Laser scribing	10	[56]
10	3D wrinkles	Pre-strained PDMS	>100	–	12	[21]
11	3D wrinkles	Pre-strained PDMS	0.5	EBL	30	[26]
12	2D springs	PDMS	0.1	NW lithography	30	This work

into the tube for 10 min to grow graphene, followed by a slow cooling process to room temperature without changing the gas flow.

Mask transferring and GNR etching

To load SiNWs onto the graphene substrate, a PMMA solution (M_w = 950 K, 4 wt%, AR-P 679.04, all-resist) was spin-coated onto the source substrate where SiNWs are grown, the spinning speed was 3000 r/m and the thickness of PMMA film was about 200–300 nm. The SiNW substrate with PMMA film was then immersed in 4% HF solution for 30–60s to separate the SiNW-loaded PMMA film from the source substrate, and then cleaned by deionized water several times. Then, the PMMA film was flipped and placed on the target substrate with graphene on top, forming a SiNW/PMMA/graphene stack that was annealed subsequently at 150 °C for 2–3 min to enhance the adherence of the whole structure. After that, the transferred SiNWs served as nanoscale shadow masks during an oxygen plasma reactive ion etching, with power density, O_2 flow rate, and chamber pressure of 30 W, 9 SCCM, and 2.9 Pa, respectively. This thus etched off the exposed PMMA layer and GNRs, leaving only the segments protected by the SiNW masks. At the end, the PMMA and SiNWs were immediately removed by using hot acetone (60 °C).

FET device fabrication and measurement

The source and drain electrodes (Ti/Au, 5 nm/30 nm) were deposited on top of the graphene stacks through a shadow mask by electron beam evaporation. The electrical measurements were conducted using a semiconductor parameter analyzer (Keithley 4200) in a closed cycle cryogenic probe station under vacuum ($<10^{-5}$ Torr) at room temperature.

Characterizations and simulation

The morphology of the SiNWs was characterized by using scanning electron microscope (SEM, Zeiss Sigma). The thickness of the remained GNRs was measured by Raman Spectra (Horiba Jobin Yvon Lab RAM HR-800 Raman spectrometer with a 514-nm argon ion laser). Surface morphology and the channel width of the GNRs were characterized by AFM (Cypher, Asylum Research Inc.). The mechanical deformation of the stretched GNRs was simulated by using finite element suite, COMSOL Multiphysics, where the Young's modulus, Poisson-ratio and density of the GNRs are 1.05 TPa, 0.186, 0.77 mg/m^2, respectively.

DATA AVAILABILITY

All relevant data are available from the corresponding authors on request.

AUTHOR CONTRIBUTIONS

C.L. and L.Y. conceived and designed the experiments; B.Y. and C.L. prepared the monolayer or few-layer graphene by CVD or exfoliation methods; C.L., T.D., and L.Y. carried out the growth, transferring of in-plane SiNWs, GNR etching, device fabrications, and characterizations; C.L., L.G., and L.Y. wrote the paper and prepared the figures; H.M. and C.L. performed the s.e.m., Raman and AFM characterizations; S. Z., J.W., and C.L. carried out the simulation and strain analysis. All the authors participated in discussing and reviewing the paper.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-019-0105-7).

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