





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## A novel active cell balancing topology for serially connected Li-ion cells in the battery pack for electric vehicle applications

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In a Battery Management System (BMS), cell balancing plays an essential role in mitigating inconsistencies of state of charge (SoCs) in lithium-ion (Li-ion) cells in a battery stack. If the cells are not properly balanced, the weakest Li-ion cell will always be the one limiting the usable capacity of battery pack. Different cell balancing strategies have been proposed to balance the non-uniform SoC of cells in serially connected string. However, balancing efficiency and slow SoC convergence remain key issues in cell balancing methods. Aiming to alleviate these challenges, in this paper, a hybrid duty cycle balancing (H-DCB) technique is proposed, which combines the duty cycle balancing (DCB) and cell-to-pack (CTP) balancing methods. The integration of an H-bridge circuit is introduced to bypass the selected cells and enhance the controlling as well as monitoring of individual cell. Subsequently, a DC–DC converter is utilized to perform CTP balancing in the H-DCB topology, efficiently transferring energy from the selected cell to/from the battery pack, resulting in a reduction in balancing time. To verify the effectiveness of the proposed method, the battery pack of 96 series-connected cells evenly distributed in ten modules is designed in MATLAB/Simulink software for both charging and discharging operation, and the results show that the proposed H-DCB method has a faster equalization speed 6.0 h as compared to the conventional DCB method 9.2 h during charging phase. Additionally, a pack of four Li-ion cells connected in series is used in the experiment setup for the validation of the proposed H-DCB method during discharging operation. The results of the hardware experiment indicate that the SoC convergence is achieved at ~ 400 s.

**Keywords** Active cell balancing, Cell bypass, Energy redistribution balancing (ERB), Duty cycle balancing, Lithium-ion (Li-ion) cells, State-of-charge (SoC)

### List of symbols

$I(t)$	Charging and discharging current
$I_{batt}$	Load current
$I_j^M$	Intermodular balancing current
$I_i^b$	Balancing current from cell 'i'
$I_{bal}$	Balancing current
$\eta$	Energy transferring efficiency
$N$	Number of cells
$Q_{max}$	Maximum capacity
$R_s$	Cell internal resistance

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$SoC_o$	Initial SoC
$V_t$	Cell terminal voltage
$V_{oc}$	Open circuit voltage
$V_1$ & $V_2$	Primary and secondary voltage of DC–DC converter
$Z$	Number of modules

### Abbreviations

AI	Artificial intelligence
ACTC	Adjacent cell to cell
BESS	Battery energy storage system
BMS	Battery management system
CTP	Cell to pack
CTPTC	Cell to pack to cell
DCTC	Direct cell to cell
DCB	Duty cycle balancing
EV	Electric vehicle
ERB	Energy redistribution balancing
H-DCB	Hybrid duty cycle balancing
ICE	Internal combustion engine
Li-ion	Lithium-ion
M	Module
PI	Proportional integral
PHEV	Plug-in hybrid vehicle
SoC	State-of-charge

Lithium-ion (Li-ion) batteries offer several key advantages, including high energy and power density, a low self-leakage rate (battery loses its charge over time when not in use), the absence of a memory effect, a long operational life cycle, and minimal environmental impact<sup>1</sup>. Therefore, found extensive applications in EVs and electronic gadgets (mobile and laptops). In battery packs, cells are interconnected in parallel and series configurations to attain the necessary voltage and power ratings<sup>2</sup>. Variations in cell voltage can be observed among serially connected cells that are supposed to be identical due to discrepancies in the manufacturing process<sup>3</sup>. As the battery pack is used more frequently, these initial variations often become more pronounced due to internal temperature gradients, which causes uneven cell aging. Inconsistencies in self-leakage rate, internal resistance, storage capacity, and other parameters can emerge among the cells<sup>4</sup>. With multiple charge and discharge cycles, these disparities gradually intensify, potentially leading to overcharging or discharging of individual cells. This can result in reduced usable capacity, shortened battery lifespan, and, in more severe cases, safety concerns such as explosions or spontaneous combustion<sup>5</sup>. When cells are connected in series in a battery pack, the cell with the lowest capacity limits the total capacity that can be used, unless a balancing circuit is used. Therefore, it is of utmost importance to investigate cell balancing methods that can mitigate these inconsistencies, enhance battery capacity utilization, prolong battery lifespan, and guarantee the effective and safe functioning of batteries<sup>6</sup>. Cell balancing can be achieved through either passive (dissipative) or active (non-dissipative) balancing methods<sup>7</sup>.

Passive balancing equalises cell SoC by redirecting excess charge from the cells with the highest charge (highest SoC) to their corresponding shunt resistors, which typically dissipate the extra energy as heat. In practice, passive or dissipative balancing schemes offer a lower balancing capability than non-dissipative or active balancing methods. This is primarily because passive methods dissipate energy, which can be both wasteful and difficult to manage, particularly in applications with limited space<sup>7</sup>. For battery packs that use passive balancing, only the minimum cell capacity can be reclaimed during discharge (assuming the cell cannot be bypassed); once the cut-off voltage limit of the cell with the lowest capacity (lowest SoC cell) is reached, the discharge operation must be stopped<sup>8</sup>. Conversely, active balancing methods do not involve energy dissipation but rather focus on controlling the charging and discharging rates of individual cells to maintain a consistent SoC for all cells throughout their operation. With advancements in power electronics technology and increasing emphasis on energy conservation, active balancing methods have gained significant attention in both domestic and international research communities<sup>9</sup>. The following literature presents a classification of active balancing methods based on different energy transfer pathways.

Most non-dissipative balancing schemes discussed in the literature<sup>10,11</sup> employ energy redistribution balancing (ERB), a method in which all cells are interconnected in series, ensuring that all cells carry the main pack current continuously. In the ERB method, balancing among cells is done by transferring the energy between cells through different balancing circuits. ERB circuits are typically categorized into four groups based on their architecture<sup>10</sup>: direct cell-to-cell (DCTC), adjacent cell-to-cell (ACTC), cell-to-pack (CTP), and cell-to-pack-to-cell (CTPTC). In the ACTC architecture, balancing circuits alike the switched capacitor<sup>12</sup>, bidirectional buck-boost converter<sup>13,14</sup>, and Ćuk converter<sup>15,16</sup> are employed. The ACTC design is favoured for their simplicity, modular structure, and cost-effectiveness. However, these methods have constraints as charge transfer is limited to adjacent cells, potentially causing extended balancing periods and increased energy and power losses, especially in packs with a relatively high cell count. Conversely, the DCTC architecture enables energy transfer between any two cells, irrespective of their position, through the use of suitable switches and a storage element. Nevertheless, this method is constrained by the limitation that only two cells can be balanced simultaneously. This limitation leads to prolonged equalization time, especially when addressing a considerable number of imbalanced (different SoC)

charged cells. Circuits such as the flying capacitor<sup>17</sup>, quasi-resonant converter, and shared inductor<sup>18</sup> align with DCTC architecture. In the CTP design, energy transfer is facilitated between an individual cell and the battery pack, offering greater flexibility in the balancing process. Redistribution of charge is accomplished through distributed circuits, such as multi-winding transformers, flyback converters, and shared storage elements<sup>19,20</sup>. However, CTP circuit designs are associated with an increase in size and cost in comparison to the previously mentioned circuit designs.

Present equalization methods exhibit limitations in effectively transferring energy between cells. To overcome this challenge and achieve precise regulation of individual cells, the concept of ‘power electronics enhanced battery packs’ has been introduced for diverse applications<sup>21,22</sup>. These battery packs integrate power electronic switches capable of handling the entire pack current, allowing for cell bypass during operation in the event of cell failure. This feature enhances the overall reliability of the battery system without significantly escalating the overall cost, distinguishing it from ERB systems where all cells remain consistently in the main current path<sup>23</sup>. Active cell balancing is facilitated by the capability to bypass cells during operation by modifying the duty cycle of each cell according to their relative SoC<sup>24</sup>. Different power electronics-enhanced battery packs are investigated in<sup>25</sup>. Cells are interconnected in series using an H-bridge circuit (using two MOSFETs) positioned around each cell. This configuration enables individual cells to function either in series (with a cell current as same as the string current) or to be bypassed (resulting in zero cell current). Figure 1 depicts a traditional equalization topology circuit of DCB.

The objective of this research is to tackle the challenges associated with employing hundreds of cells connected in series within an EV battery pack. The primary challenges involve a relatively slow balancing process and low balancing efficiency. To address these issues, a novel SoC balancing approach is introduced in this study. This innovative method combines DCB and CTP balancing techniques using a DC–DC converter, and it is referred to as “hybrid duty cycle balancing” (H-DCB). The goal is to maintain the advantageous characteristics of both the topology presented in previous works<sup>5</sup> and<sup>8</sup>, while effectively addressing their limitations. In comparison to the topology described in<sup>5</sup> and<sup>8</sup>, in this paper the proposed balancing strategy, H-DCB, is designed to significantly reduce the time required to achieve SoC balancing among the cells in the battery pack.

### Main contribution

In this paper, a novel SoC balancing approach is proposed, which combines DCB and CTP balancing techniques using a DC–DC converter to reduce the time required for SoC balancing. In this study, various balancing topologies are compared to demonstrate the effectiveness of the proposed H-DCB strategy. When contrasted with the ACTC balancing topology, the proposed H-DCB strategy is no longer dependent on the physical location of cells, allowing for direct balancing between any pair of cells. In comparison to the DCTC balancing topology, it can simultaneously balance multiple pairs of cells. In contrast to the traditional DCB topology, it can achieve balancing even during periods of idle state (not actively charging/discharging) and significantly reduce the balancing time. This contrasts with ERB (ACTC, DCTC, CTP, and CTPTC) systems, the capability to bypass cells during operation facilitates active cell balancing by dynamically adjusting the duty cycle of each cell according to their relative SoC<sup>24,26</sup>.

Table 1 provides a comparative analysis of the proposed topology with existing research in terms of the control complexity, applications, controlling and monitoring of each cell, balancing current determination in each cell ( $I_i^b$ ), SoC balancing method, and the main drawbacks. Also, in Table 1 the balancing current is computed to assess SoC using the coulomb counting (CC) method and to evaluate balancing losses in each cell. The process of determining the balancing current in the proposed balancing topology is explained in “Current determination” section.

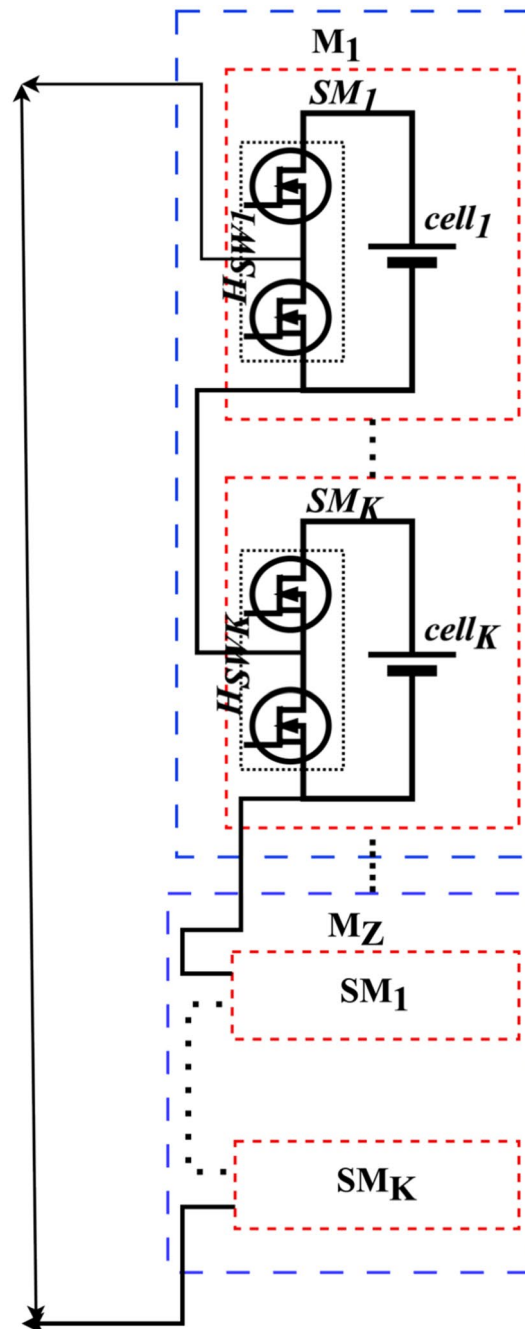
This study aims to offer a simple and precise SoC balancing circuit topology to reduce the time required for balancing and enhancing the overall system efficiency. The methodology for the proposed topology including the circuit diagram and working operation is outlined in Section II. Section III elaborates on the control strategy of the proposed H-DCB topology. The simulation results of the proposed H-DCB strategy along with a comparison of balancing performance with traditional DCB are explained in section IV. The experimental setup is detailed in Section V and the last section serves the conclusion and future work for this paper.

### Methodology

The proposed H-DCB topology offers an advanced strategy for active cell balancing. The focus in this balancing process is to obtain the value of SoC using the current integration (coulomb counting) method, which relies on the current determination of each cell in the battery pack. This section includes the circuit diagram description, operating principle, and current determination of each cell in the proposed topology.

### Description and circuit diagram

The proposed layout of a battery bank with 96s1p (96 cells in series) is shown in Fig. 2. Thus, the battery has a nominal voltage of 350 V and a capacity of 20 Ah. The battery pack has a similar configuration as in the Chevrolet Bolt EV with 10 modules which has a total of 288 cells connected in 96s3p (3 parallel strings each having 96 cells in series). The cells connected in parallel are assumed to be identical and do not differ in their characteristics. Therefore, this circuit might be comparable to a battery bank with a connection of 96s1p (96 cells in series). In this paper, A battery pack of 96s1p is divided into 10 modules (M) connected in series, with 8 M each having 10 cell groups and 2 M each having 8 cell groups. M is divided into k sub-modules (SM) that are connected in series, each SM consists of integration of an H-bridge around cell, and each SM is connected to a DC–DC converter that transfers energy to/from a selected cell to/from the entire respective module M.



**Figure 1.** DCB equalization topology circuit.

Figure 3 depicts the status of an SM-related switch ( $H_{SWZ}$ ) as ON (1 or  $-1$ ) or OFF (0), as well as its effects on voltages across the SM, which are equivalent to cell voltage  $+V_c$  or 0 accordingly. As a result, the voltage across M is summed according to the number of activated cells (for example, M includes 10 cells, nine of them are activated while the remaining one is bypassed). As a result, the voltage across the module ( $V_M$ ) equals the total of the voltages of the activated cells. A DC–DC converter is also connected in parallel to each M for intermodular balancing.

### Operating principle of proposed topology

During the charging and discharging operation, cells are interconnected in series through an H-bridge circuit, allowing any specific cell to be either in series (current flowing through an individual cell is equal to the overall pack current within the string) or bypassed (no or zero current). Individual cells are independently regulated by their connection to an H-bridge. The capability to bypass cells during operation facilitates active cell balancing by adjusting the duty cycle of each cell by the SoC balancing strategy is outlined in the section below III. The core concept of the proposed H-DCB method involves using a DC–DC converter to discharge the bypassed cell

Balancing strategy	Cell balancing schemes	Controlling and regulating individual cell	Limitation	Applications/cost	Balancing losses
Chatziniolaou & Rogers <sup>8</sup>	Balancing scheme based on duty cycle for both DC packs (DCB-DC) and AC packs (DCB-AC)	Yes	The cell with the lowest capacity in DC packs (DCB-DC) limits the effective pack capacity. Losses resulting from series resistance at low-frequency current ripple in AC packs (DCB-AC)	Medium and High power applications/ High cost	Balancing losses are zero as the selected cell gets bypassed from the current path $I_i^b = \begin{cases} 0 & \text{Selected cell} \\ I(t) \pm I_j^M & \text{Other cells} \end{cases} \quad (1)$
Cao et al. <sup>5</sup>	SoC-based equalization (CTC)	Yes	Equalization time is prolonged as balancing can only be executed between two cells at a time	Medium and High power applications/ Medium cost	Balancing losses are high as the equalization circuit consists of multi winding transformer (flyback converter) $I_i^b = \begin{cases} -I_{bal} + I(t) \pm I_j^M & \text{high charged cell} \\ hI_{bal} + I(t) \pm I_j^M & \text{low charged cell} \\ I(t) \pm I_j^M & \text{other cells} \end{cases} \quad (2)$
Ci et al. <sup>27</sup>	Voltage-based balancing reconfiguration circuit	No	A different configuration circuit is required for charging and discharging states	High power applications/Low cost	Balancing losses are zero as the selected cell gets bypassed from the current path $I_i^b = \begin{cases} 0 & \text{selected cell} \\ I(t) \pm I_j^M & \text{other cells} \end{cases} \quad (3)$
Imtiaz & Khan <sup>28</sup>	Voltage-based balancing (CTP)	Yes	Reduced lifecycle of battery pack due to repeated charging and discharging	HEV applications/ Medium cost	Due to repetitive charging and discharging of selected cells, balancing losses are significant $I_i^b = \begin{cases} -I_{bal} + \frac{\eta I_{bal}}{k} + I(t) \pm I_j^M & \text{selected cell} \\ \frac{\eta I_{bal}}{k} + I(t) \pm I_j^M & \text{other cells} \end{cases} \quad (4)$
Proposed strategy	Hybrid duty cycle balancing (H-DCB)	Yes	This proposed circuit can bypass one cell at a time	EV Battery pack applications/Medium cost	Balancing losses are less than CTP balancing as it prevents repeated charging and discharging by bypassing the selected cell $I_i^b = \begin{cases} -I_{bal} & \text{selected cell} \\ \frac{\eta I_{bal}}{k-1} + I(t) \pm I_j^M & \text{other cells} \end{cases} \quad (5)$

**Table 1.** Evaluating the proposed topology in comparison to various existing studies in the literature.

during charging and charge the bypassed cell during discharging to reduce the balancing time of the system. For DCB to take place, the system needs to be configured with some “redundant cells” to ensure the attainment of the necessary output voltage even when certain cells are redirected or bypassed. DCB can also be implemented in battery pack topologies that facilitate, converting DC voltage into AC voltage as seen in packs relying on the modular multilevel converter (MMC)<sup>29,30</sup>. Accordingly, the SoC balancing strategy is designed to bypass a high-charged cell without using redundant cells. However, the primary limitation of conventional DCB topologies is the inability to harness the potential of bypassed cells. In contrast, the proposed H-DCB topology has the advantage of discharging highly charged cells and charging low charged cell in the series connected string, thereby reducing balancing time. Secondly, the failed cell can be isolated for replacement or maintenance without disrupting the battery energy storage system (BESS) operation. Thirdly, the balancing can also be achieved in an idle state (when the vehicle is not in use or not actively charging/discharging) by using CTP architecture. Additionally, it becomes evident from Eqs. (4 and 5) that the balancing method introduced in this paper avoids the repetitive charging and discharging of cells (achieved by disconnecting the high SoC cell from the current path during CTP operation, preventing it from being charged).

### Current determination

In the proposed topology, during charging mode the strongest (highest SoC) cell is identified and bypassed using an H-bridge connected in parallel to the selected cell and supplying energy to the pack via the DC–DC converter (CTP mode). The reason for choosing this circuit is that it requires only one additional balancing current sensor other than the charging/discharging current sensor to calculate the current of each cell in a module. Figure 4 shows that only one extra current sensor is needed to determine the current of each cell in the proposed balancing circuit.

The balancing current sensor is tasked with measuring the current of the selected cell designated for releasing or absorbing energy during the balancing operation through a switch matrix. Given that only one cell is bypassed and connected to the DC–DC converter at any given moment, the resultant current of the selected (bypassed) cell and the other cells can be calculated, as shown in Eq. (6).

$$I_i^b = \begin{cases} -I_{bal} & \text{selected cell} \\ \frac{\eta I_{bal}}{k-1} + I(t) \pm I_j^M & \text{other cells} \end{cases} \quad (6)$$

where  $I(t)$  = Charging/discharging current,  $I_i^b$  = balancing current from the cell ( $1 \leq i \leq k$ ),  $I_{bal}$  = balancing current,  $I_j^M$  = balancing current from the module ( $1 \leq j \leq z$ ),  $k$  = number of sub-modules,  $z$  = number of modules.

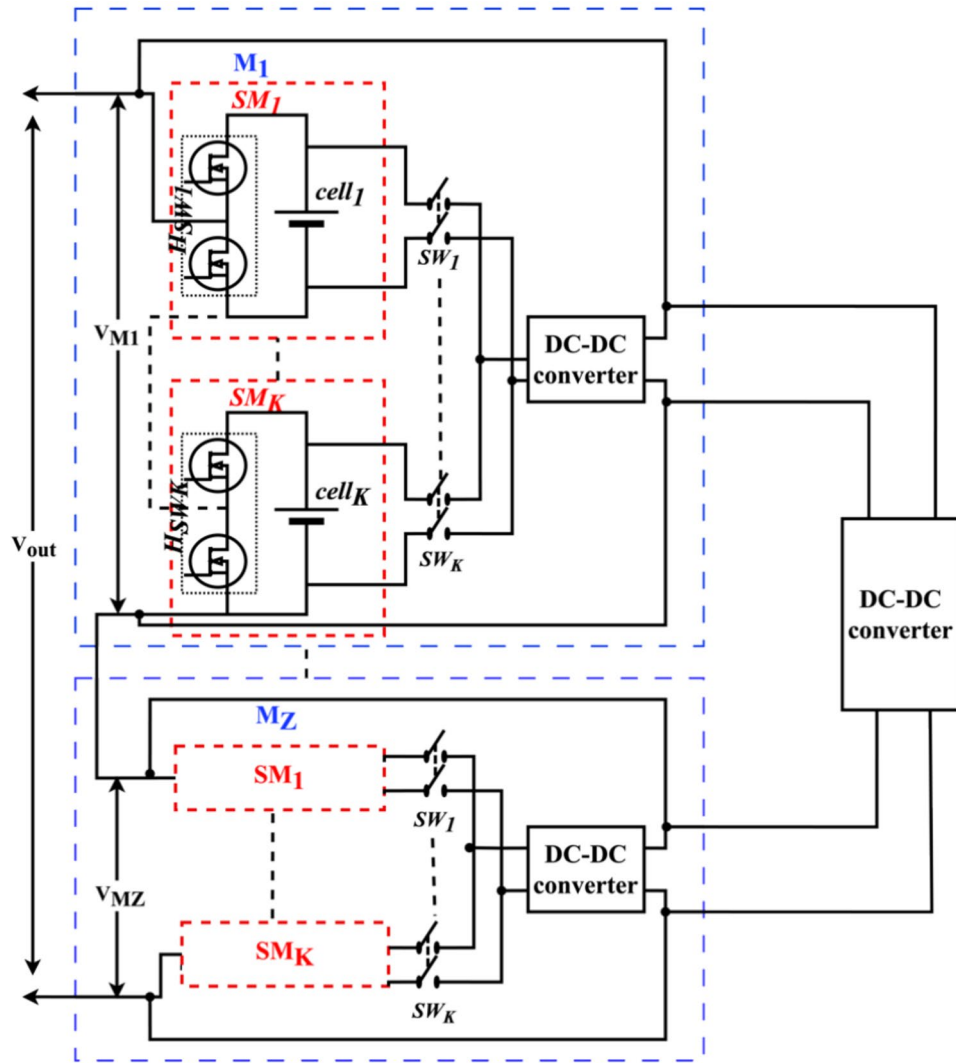


Figure 2. Circuit diagram of the proposed H-DCB topology.

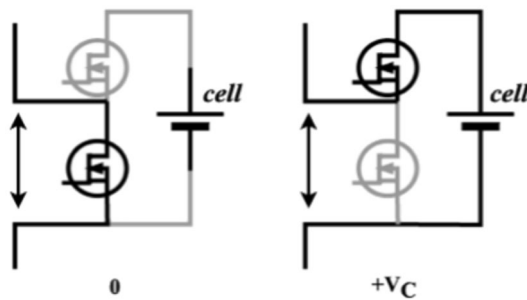
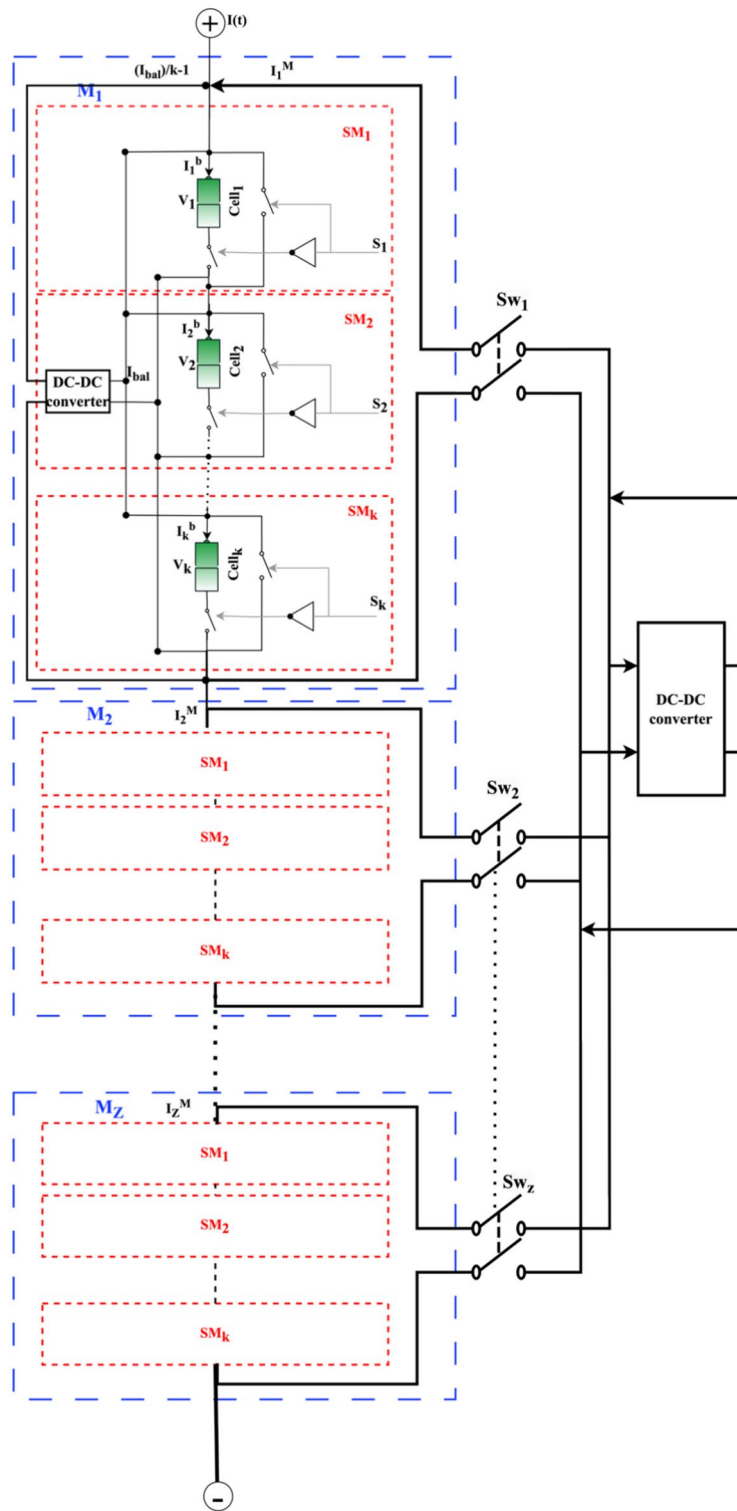


Figure 3. Status of H-bridge.

### Battery cell Soc determination

For determining SoC there is already much detailed literature<sup>31</sup> available, the SoC determination strategies such as kalman or particle filter, open circuit voltage method (OCV), current integration method, extended kalman filter (EKF), and unscented kalman filter (UKF) are the most common SoC determining methods<sup>31</sup>. In this study, the CC method is used to calculate the SoC as it only needs the information of the current and initial SoC of the battery cell and requires very low computational power. For estimating SoC, a Thevenin equivalent circuit

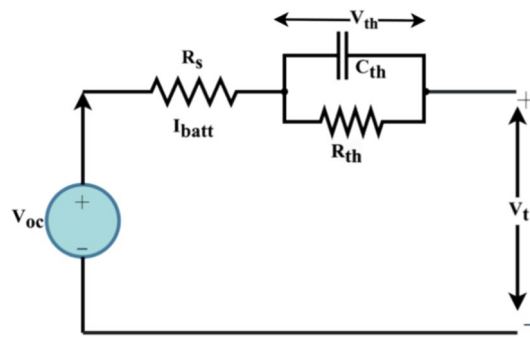


**Figure 4.** Current determination.

model is adopted for describing the battery cell dynamic characteristics, performed on the MATLAB/Simulink platform is shown in Fig. 5.

### Battery modelling

Several battery models such as the RC model,  $R_{int}$  model, linear regression model, dual polarisation model and fractional model have been proposed by various studies, as seen in<sup>31</sup>. The 1-RC models are valuable for understanding the transient response and time-dependent behavior as well as they are easy to design equivalent battery



**Figure 5.** Equivalent circuit for Li-ion battery.

characteristics. The internal impedance of the battery influences the balancing current and terminal voltage. As a result, it should be considered during the system's design process. Figure 5 presents the 1-RC model with an RC network in series, obtained from the  $R_{int}$  model<sup>31</sup>, offering a description of the dynamic characteristics of the battery. The battery's electrical behaviour is shown in Eq. (7).

$$\begin{cases} V_t = V_{OC} - V_{th} - I_{batt}R_s \\ \dot{V}_{th} = \frac{-V_{th}}{R_{th}C_{th}} + \frac{I_{batt}}{C_{th}} \end{cases} \quad (7)$$

where  $I_{batt}$  = load current (positive when discharging and negative when charging),  $V_t$  = terminal voltage,  $V_{OC}$  = open circuit voltage,  $C_{th}$  = equivalent capacitance,  $R_s$  = internal resistance,  $V_{th}$  = voltage across  $C_{th}$ ,  $R_{th}$  = polarization resistance.

The crucial factors of a battery cell include battery capacity,  $V_{OC}$ ,  $R_s$ , equivalent capacitance ( $C_{th}$ ), and polarization resistance ( $R_{th}$ ). These variables depend on the SoC, temperature, and current of the battery<sup>32</sup>. To perform simulations, it is necessary to create or pre-calibrate tables that depict the relationships between these parameters. The input values for these tables, namely temperature and SoC, can be obtained through established methods. SoC is estimated using the standard current integration method, and the temperature is assumed to be 25 °C.

This study employed a high-energy Li-ion battery with a nominal capacity of 20 Ah and a voltage of 3.6 V. The model parameters for the equivalent circuit component are determined by incremental current test<sup>33,34</sup> as illustrated in Fig. 6, and lookup tables are established in MATLAB/Simulink for battery modelling accordingly. To save test time, a reduced capacity of 1 Ah was utilized during the test. A maximum cell voltage of 4.0 V is set to prevent over-charge of the Li-ion battery. The battery cell underwent continuous charge with 200 s, 2 A current pulses alternating with 200 s breaks until the terminal voltage reached the maximum charge voltage of 4.0 V. The current pulses, measured voltage response, and calculated SoC using the CC method are depicted in Fig. 7. The offline parameter identification approach used for the validation of the battery cell model is presented below.

### Offline model parameter identification

The parameters of the battery model can be determined through two methods: online identification and offline identification<sup>32</sup>. The diagram shown in Fig. 6 demonstrates the offline identification approach employed in this study. This approach involves conducting an incremental current test on the Li-ion battery until it reaches the charge cut-off voltage. Subsequently, the model parameters can be computed as follows:

- Variable capacitor  
The variable capacitor  $C_o$  can be calculated as:

$$C_o(\text{SoC}) = \frac{\Delta Q}{\Delta V_{OC}}, \quad (8)$$

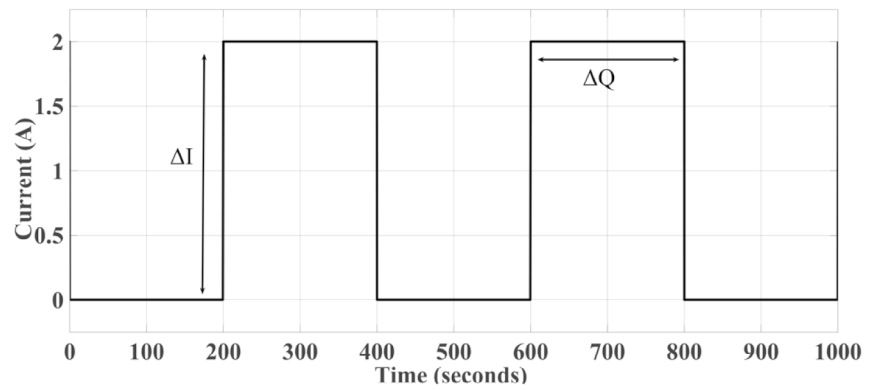
where  $\Delta Q$  = Incremental discharge capacity in one discharging step which can be calculated by the Ampere-hour counting method.  $\Delta V_{OC}$  = Voltage changes between  $V_{OC}$  and SoC.

- Ohmic resistance  
During the discharge of the Li-ion battery, a noticeable abrupt decline in the measured terminal voltage occurs. The terminal voltage difference  $\Delta V_t$  at the beginning of the discharging moment is divided by the current difference  $\Delta I$  to determine  $R_s$ <sup>35</sup>. This can be expressed as follows:

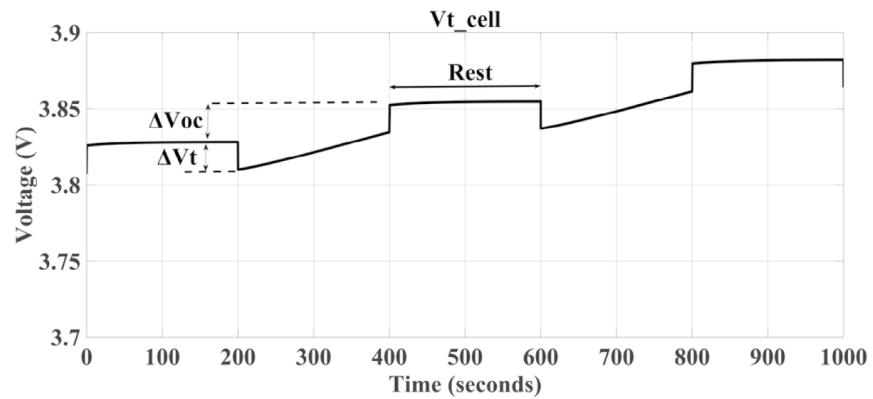
$$R_s(\text{SoC}) = \frac{\Delta V_t}{\Delta I} \quad (9)$$

- RC circuits  
Following the zero-input response, the remaining process depicted in Fig. 7b can be characterized by the following equation:

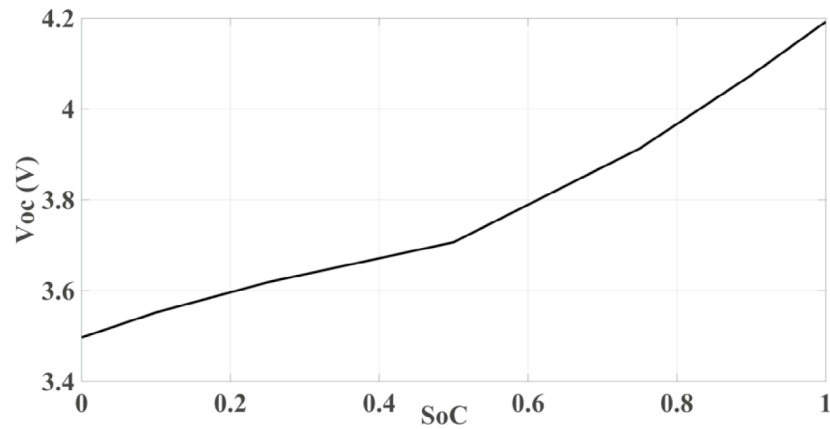




(a)



(b)



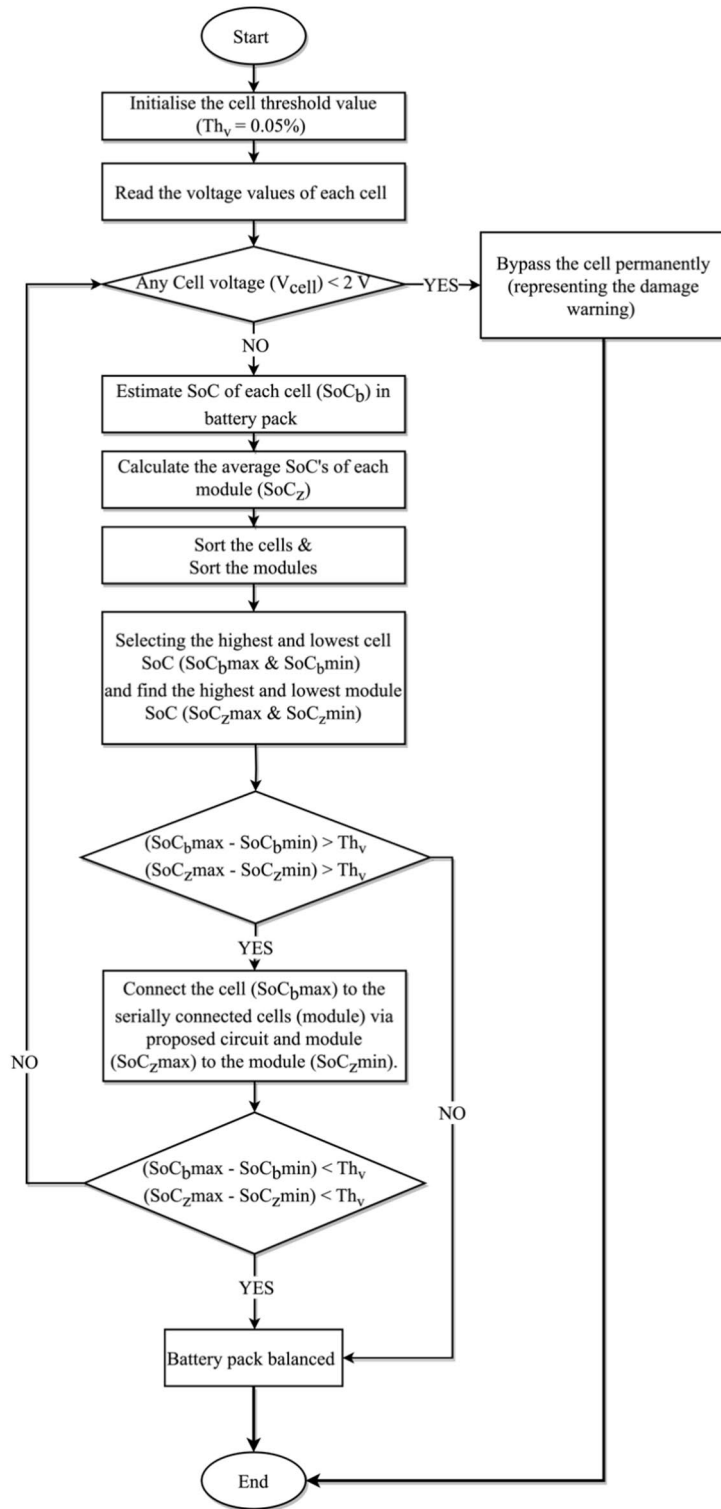
(c)

**Figure 6.** Representation of the offline parameter identification process. (a) Current pulses (b) Measured voltage response (c)  $V_{OC}$  versus SoC graph.

$$V_t = V_{OC} - IR_{th}e^{-\frac{t}{R_{th}C_{th}}} \tag{10}$$

In this study, the identification of RC circuit parameters is carried out using MATLAB/Simulink. The exponential fitting function employed is outlined as follows:

$$y = y_0 + Ae^{-\lambda t} \tag{11}$$



**Figure 7.** Control strategy for the proposed method.

where  $A_1$  and  $\lambda_1$  are the coefficients obtained through the least square method. Comparing Eq. (10) with Eq. (11), the parameters can be calculated by:

$$\begin{cases} R_{th}(SoC) = A_1/(-I) \\ C_{th}(SoC) = \frac{1}{\lambda_1 R_{th}} \end{cases} \quad (12)$$

Consequently, a set of parameters can be computed at corresponding SoC points. Polynomial interpolation is employed to extrapolate the model parameters at untested SoC points<sup>35</sup>.

### SoC estimation method

SoC balancing is typically implemented using one of two approaches: cell SoC or cell terminal voltage. The precision of SoC estimation is critical in cell balancing. As a result, numerous approaches for obtaining an accurate SoC estimation have been presented in<sup>36,37</sup>. The CC method is based on the principle of integrating current over time, and it tends to provide a linear SoC estimation. It often requires basic hardware such as current sensors and a microcontroller, making it a cost-effective and straightforward solution. Based on Eq. (13), the CC approach is employed in this paper to determine cell SoC.

$$SoC(t) = SoC_o + \frac{1}{Q_{max}} \int_0^t i(t) dt, \quad (13)$$

where  $SoC_o$  = initial SoC,  $SoC(t)$  = SoC at a time 't',  $Q_{max}$  = maximum capacity of a cell,  $i(t)$  = current going in and out of a cell.

### Balancing control strategy

The balancing algorithm of the proposed topology for the battery pack (consists of  $N$  number of serially connected cells) is divided into  $Z$  modules  $M_1, M_2 \dots M_z$ . Each module may contain an equal number of  $k$  cells  $b_1, b_2 \dots b_k$ . Firstly, the controller reads the voltages of all cells. If all of them are in the allowable range ( $V_{cell} > 2 V$ ), the SoC of each cell and module is determined, then cells are sorted and the cells with the minimum and maximum SoC ( $SoC_{b,min}$  and  $SoC_{b,max}$ ) values are determined. If there is more than one module in the battery pack, the modules are sorted as well into the highest and lowest average SoC ( $SoC_z,max$  and  $SoC_z,min$ ). After checking the overall battery pack for faults and enabling the switch matrix according to the desired direction, the strongest module ( $SoC_z,max$ ) energy is transferred to the weakest module ( $SoC_z,min$ ) in the pack until the threshold ( $SoC_z,max - SoC_z,min < 0.05\%$ ) is reached. A DC–DC converter is connected to the module with  $SoC_z,max$  which takes up the energy from each cell inside the module, to charge the module with  $SoC_z,min$ . In parallel to the intermodular equalization, the cell with  $SoC_{b,max}$  is selected in each module and gets bypassed using an H-bridge circuit, as well as this bypass cell gets discharged (CTP) via a DC–DC converter to a whole bunch of cells inside the modules until all cells are balanced i.e., ( $SoC_{b,max} - SoC_{b,min} < 0.05\%$ ). Thus, achieving both intramodular (balancing of cells inside modules) and intermodular (balancing among modules) uniformity. The same process can be followed during the discharging phase by just bypassing the lowest SoC cell instead of the highest SoC cell and getting it charged by the other cells in the module. The balancing algorithm flowchart is depicted in Fig. 7.

#### Simulation results for the proposed topology

To validate the performance of the proposed SoC balancing technique, a simulation model has been developed in the MATLAB/Simulink program (R2021b). The battery model was developed using<sup>31</sup> and explained in Sect. 2.4.1. The CC method for estimating cell SoC is described in Sect. 2.4.3. Tables 2 and 3 depict the battery pack and cell parameters used in the simulation. The Li-ion cells are used in this paper, with the configuration of nominal capacity: 20 Ah and voltage: 3.65 V, and the rated energy capacity of the battery pack is equivalent to 7 kW (calculated as  $96 \times 20 \times 3.65$ ). The proposed SoC balancing strategy is validated through a case study<sup>38</sup> with an architecture similar to the one of the Chevrolet Bolt EV involving 288 cells with the configuration of 3 parallel strings each containing 96 cells in series (96s3p). It is important to note that in the case study, the rated energy capacity is equivalent to 60 kWh (calculated as  $288 \times 57 \times 3.65$ ). As the three parallelly connected cells are assumed to be identical and have the same characteristics, the pack with 96s1p is comparable to the pack having 96s3p. Therefore, this simulation model considers only 1 string of 96 serially connected cells and is simulated in MATLAB/Simulink.

Parameters	Value
Battery nominal voltage	350 V
Battery nominal capacity	20 Ah
Nominal energy capacity	60 kWh
Battery type	Li-ion

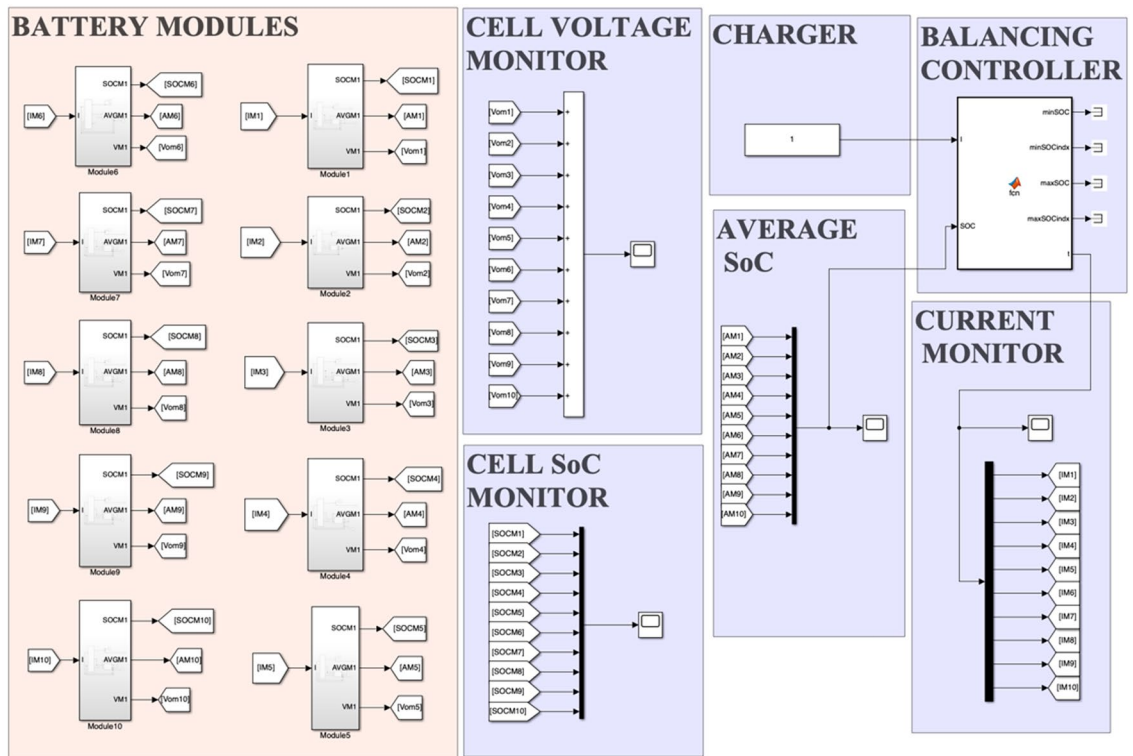
**Table 2.** Battery parameters used in simulation.

Rated cell voltage	3.65 V
Battery cell capacity	20 Ah
No. of module	10
Total no. of cells	288 (96s3p)

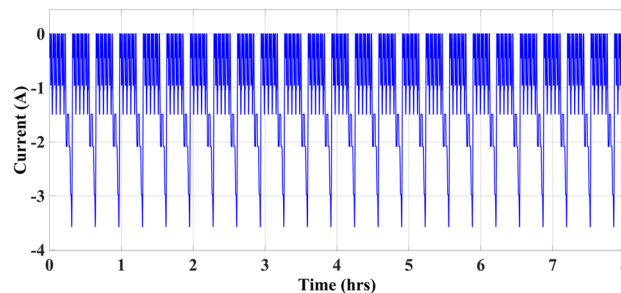
**Table 3.** Li-ion cell parameters.

A simulation result for this paper compares the H-DCB topology proposed in section II with a conventional DCB. In the proposed H-DCB architecture, each cell is separately controlled using only two power switches (H-bridge circuit) to bypass the selected cell or highest/lowest charged cell completely from the current path depending on the control strategy. The CTP method is employed sequentially to transfer charge from a selected (bypassed) cell to the entire battery pack or module using galvanic-isolated DC-DC converters. Thus, shortening the SoC balancing time. Whereas, in the conventional DCB method, the bypassed cell does not transfer any charge to and from the pack or module. The main disadvantage of DCB topology is that it can only equalize the Li-ion cells in the battery pack during the charging or discharging state whereas, in the H-DCB method it can equalize the Li-ion cells in the battery pack during the idle state (neither charging nor discharging) using CTP circuitry. The simulation model for the proposed H-DCB strategy is developed to replicate a Li-ion battery pack consisting of ten modules (8 modules, each consisting of 10 cells and 2 modules, each consisting of 8 cells) along with a cell balancing system, as depicted in Fig. 8. The series connected Li-ion cells in battery pack is charged by 1.5 A current during charging mode and a current load profile from New European Drive Cycle (NEDC)<sup>39</sup> as shown in Fig. 9 is used during discharging mode.

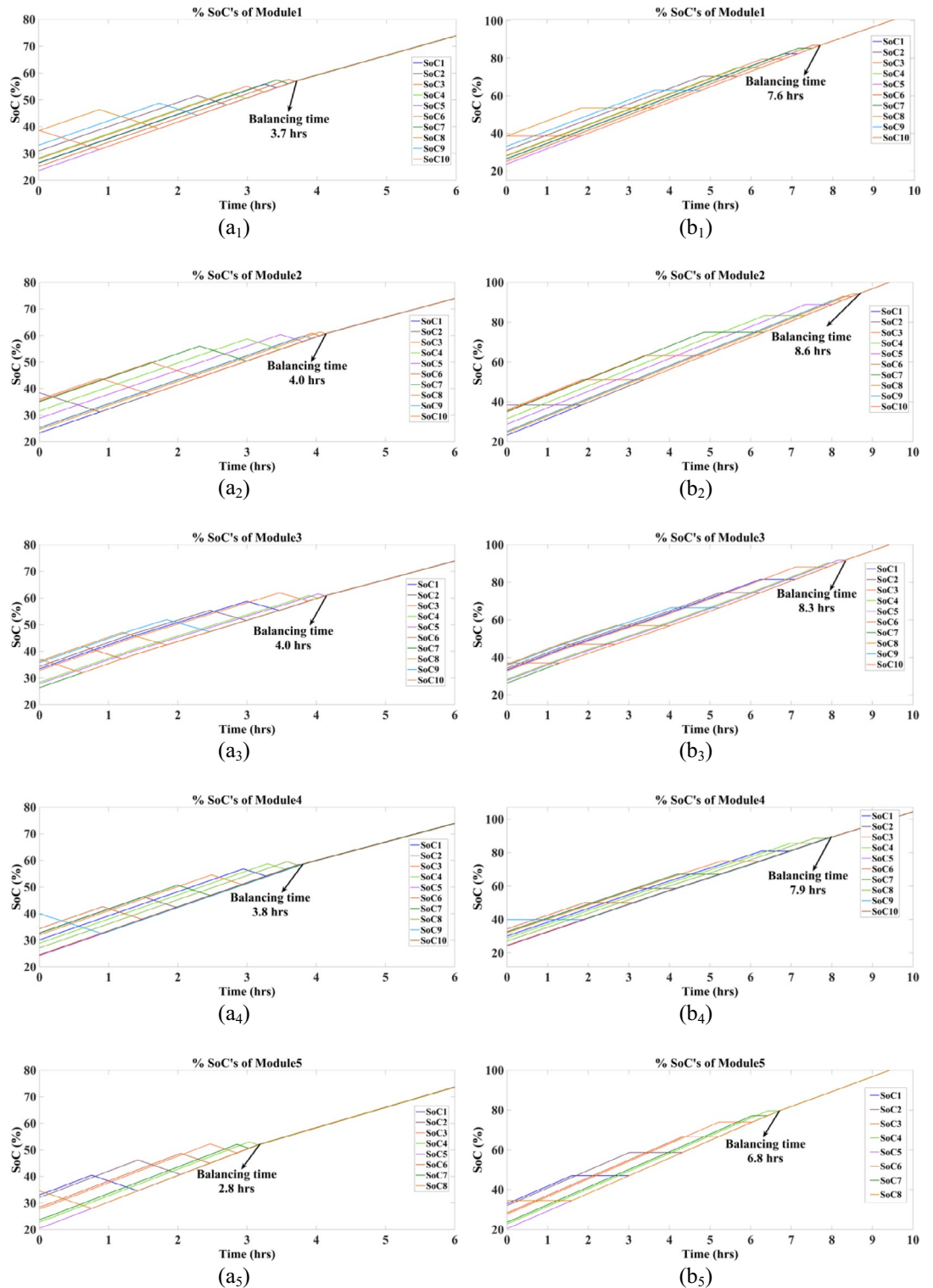
The cells connected in series vary in initial SoCs, the cell's initial SoC to be randomly generated in the interval (20% to 40%) during charging mode as shown in Fig. 10a and b and during discharging mode, initial SoCs are taken in the interval of (70% to 90%) as shown in Fig. 14a and b. The two topologies (H-DCB and usual DCB) use the same initial SoCs, including battery parameters (balancing, charging, and discharging current) for a fair comparison of balancing time. The SoC-based algorithm keeps the SoC of each cell within a tolerance band of 0.05%. For protective measures, the balancing operation stops when the cells exceed the voltage of 4.2 V or (100%



**Figure 8.** Simulation layout for H-DCB cell balancing strategy.



**Figure 9.** NEDC load current profile.



**Figure 10.** SoCs of first 5 modules (a) Proposed H-DCB topology (b) Conventional DCB topology.

SoC) and discharge below the voltage of 2 V. The balancing algorithm compensates for the SoC differences by bypassing and discharging the highest (selected) SoC cell to the other cells within the module during charging phase and charging the lowest (selected) SoC cell from the other cells within the module during discharging phase. As a result, the SoC balancing among cells is achieved by the proposed H-DCB topology in a shorter time

as compared to conventional DCB topology for both the charging and discharging phases. Since the bypassed or selected cell is not participating in energy transfer to/from the other cells within the module inside the battery pack in the usual DCB topology, it is noticeable that the balancing time during the charging/discharging phase is almost double the proposed H-DCB topology as shown in Fig. 13a and b. Figure 10a and b show the comparison of 5 modules for H-DCB and DCB topology, respectively. From the Fig. 10a<sub>1</sub> and b<sub>1</sub>, it can be seen that the first module M<sub>1</sub> (consisting of 10 cells) converged at 3.7 h using the H-DCB method while the DCB almost takes more than double the time 7.6 h to get balanced having same initial SoCs and charging current.

Similarly, for M<sub>2</sub>, H-DCB balanced the cells at 4.0 h on the other hand DCB equalized the unbalanced cells at 8.6 h as shown in Fig. 10a<sub>2</sub> and b<sub>2</sub> respectively. Additionally, for M<sub>3</sub> and M<sub>4</sub> by utilizing the H-DCB method the SoC balance is achieved at 4.0 h and 3.8 h respectively shown in Fig. 10a<sub>3</sub> and a<sub>4</sub>. While by using the DCB method the SoC convergence is achieved at 8.3 h and 7.9 h shown in Fig. 10b<sub>3</sub> and b<sub>4</sub>. Similarly, for module M<sub>5</sub>, M<sub>6</sub> ... M<sub>10</sub> are converged at 2.8 h, 4.3 h, 2.8 h, 4.1 h, 4.3 h, and 4.2 h using H-DCB topology respectively. While in DCB mode, modules M<sub>5</sub>, M<sub>6</sub> ... M<sub>10</sub> converged at 6.8 h, 9.2 h, 6.2 h, 8.3 h, 8.4 h, and 7.9 h respectively as shown in Table 4.

The simulation results of H-DCB and DCB topology of SoC balancing for the first four modules are shown in Fig. 14a and b. From the Fig. 14a<sub>1</sub> and b<sub>1</sub>, it can be seen that the first module M<sub>1</sub> (consisting of 10 cells) converged at 6.7 h using the H-DCB method while the DCB almost takes more than double the time 12.0 h to get balanced having same initial SoCs and discharging current. Similarly, for M<sub>2</sub>, H-DCB balanced the cells at 4.6 h on the other hand DCB equalized the unbalanced cells at 9.7 h as shown in Fig. 14a<sub>2</sub> and b<sub>2</sub> respectively. Additionally, for M<sub>3</sub> and M<sub>4</sub> by utilizing the H-DCB method the SoC balance is achieved at 6.6 h and 7.1 h respectively shown in Fig. 14a<sub>3</sub> and a<sub>4</sub>. While by using the DCB method the SoC convergence is achieved at 11.7 h and 12.0 h shown in Fig. 14b<sub>3</sub> and b<sub>4</sub>. For the discharging phase, the SoC balancing convergence point for the cells/modules successfully reached in approximately 7.2 h as depicted in Fig. 15a while using DCB topology an increment in SoC convergence length of 4.8 h is observed as shown in Fig. 15b. Notably, the proposed method achieves SoC balancing in almost half the time compared to the conventional DCB method, in both charging and discharging modes. Thus, this study concludes that the proposed H-DCB method quickly achieves SoC balancing during both charging and discharging modes. This approach reduces energy loss in the charge transfer process, extends the battery life, and enhances energy utilization. The balancing time for both H-DCB and the conventional DCB is displayed in Table 5.

Consequently, in comparison to the conventional DCB equalization topology, the balancing time of the proposed topology in this paper is halved. Table 4 displays the module balancing time and SoC value at the convergence point for the H-DCB and DCB approaches. The modules are balanced using a DC-DC converter, and the pack current and current in each module are shown in Fig. 11a and b.

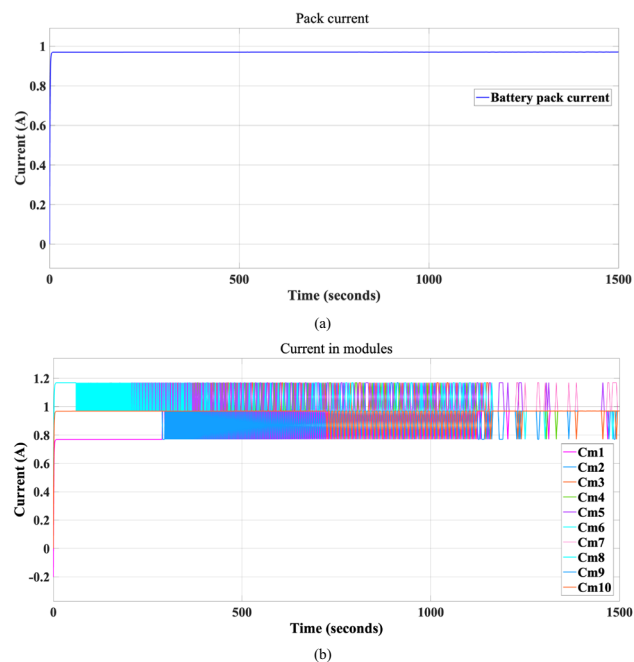
The module with the highest average SoC in the battery pack gets drained by 0.2 A current to the module with the lowest average SoC in the battery pack. The average SoC's of modules converge at 5.5 h, as shown in Fig. 12.

Module	H-DCB topology		DCB topology	
	Balancing time	SoC (%) at balancing time	Balancing time	SoC (%) at balancing time
M <sub>1</sub>	3.7 h	59%	7.6 h	88%
M <sub>2</sub>	4.0 h	60%	8.6 h	93%
M <sub>3</sub>	4.0 h	59%	8.3 h	91%
M <sub>4</sub>	3.8 h	57%	7.9 h	88%
M <sub>5</sub>	2.8 h	52%	6.8 h	79%
M <sub>6</sub>	4.3 h	62%	9.2 h	97%
M <sub>7</sub>	2.8 h	49%	6.2 h	74%
M <sub>8</sub>	4.1 h	58%	8.3 h	91%
M <sub>9</sub>	4.3 h	58%	8.4 h	93%
M <sub>10</sub>	4.2 h	60%	7.9 h	87%

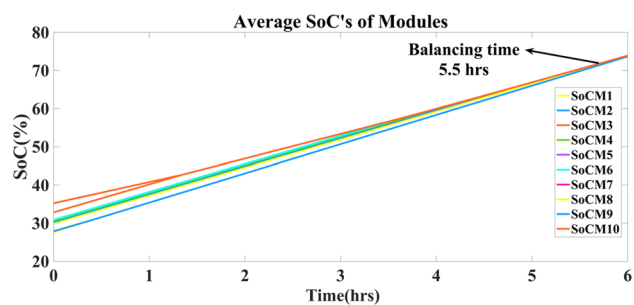
**Table 4.** Contrasting the proposed topology with the conventional configuration.

Module	H-DCB topology		DCB topology	
	Balancing time	SoC (%) at balancing time	Balancing time	SoC (%) at balancing time
M <sub>1</sub>	6.7 h	55%	12.0 h	22%
M <sub>2</sub>	4.6 h	62%	9.7 h	38%
M <sub>3</sub>	6.6 h	52%	11.7 h	21%
M <sub>4</sub>	7.1 h	50%	12.0 h	20%
SoC's of 96 cells	7.2 h	48%	12.0 h	20%

**Table 5.** Contrasting the proposed topology with the conventional configuration during discharging mode.



**Figure 11.** (a) Pack current (b) Current in each module.



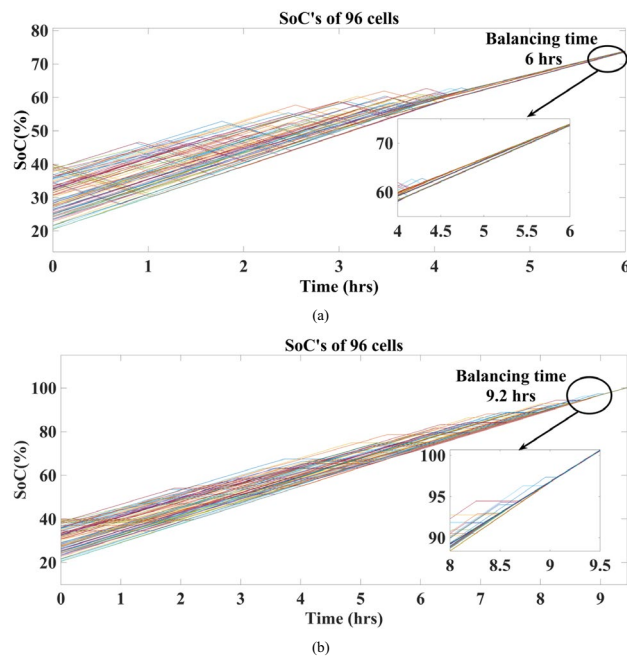
**Figure 12.** Average of module SoCs.

The proposed equalization approach H-DCB can quickly achieve SoC equalization in 6.0 h for 96 cells connected in series during the charging phase shown in Fig. 13a and on the other hand, for the same number of cells DCB takes 9.2 h to achieve SoC equalization shown in Fig. 13b.

### Experimental setup

This section indicates the proposed H-DCB balancing approach in an experimental platform; an overview of the experimental setup consists of a battery in which four NCR18650B cells are grouped in series using an H-bridge circuit (two MOSFETs) to bypass the lowest SoC cell from the main current path and also an additional switch in parallel structure to each cell to connect the lowest SoC cell to the isolated DC–DC converter (Figs. 14 and 15). Figure 16 depicts the experimental prototype circuit for the four serially connected cells in a battery pack during discharging mode.

The work on the experiment is still ongoing. Therefore, this paper presents a general overview of the experimental setup along with some preliminary findings. The hardware set-up includes four Li-ion battery cells



**Figure 13.** SoCs of 96 cells during charging operation (a) H-DCB topology. (b) DCB topology.

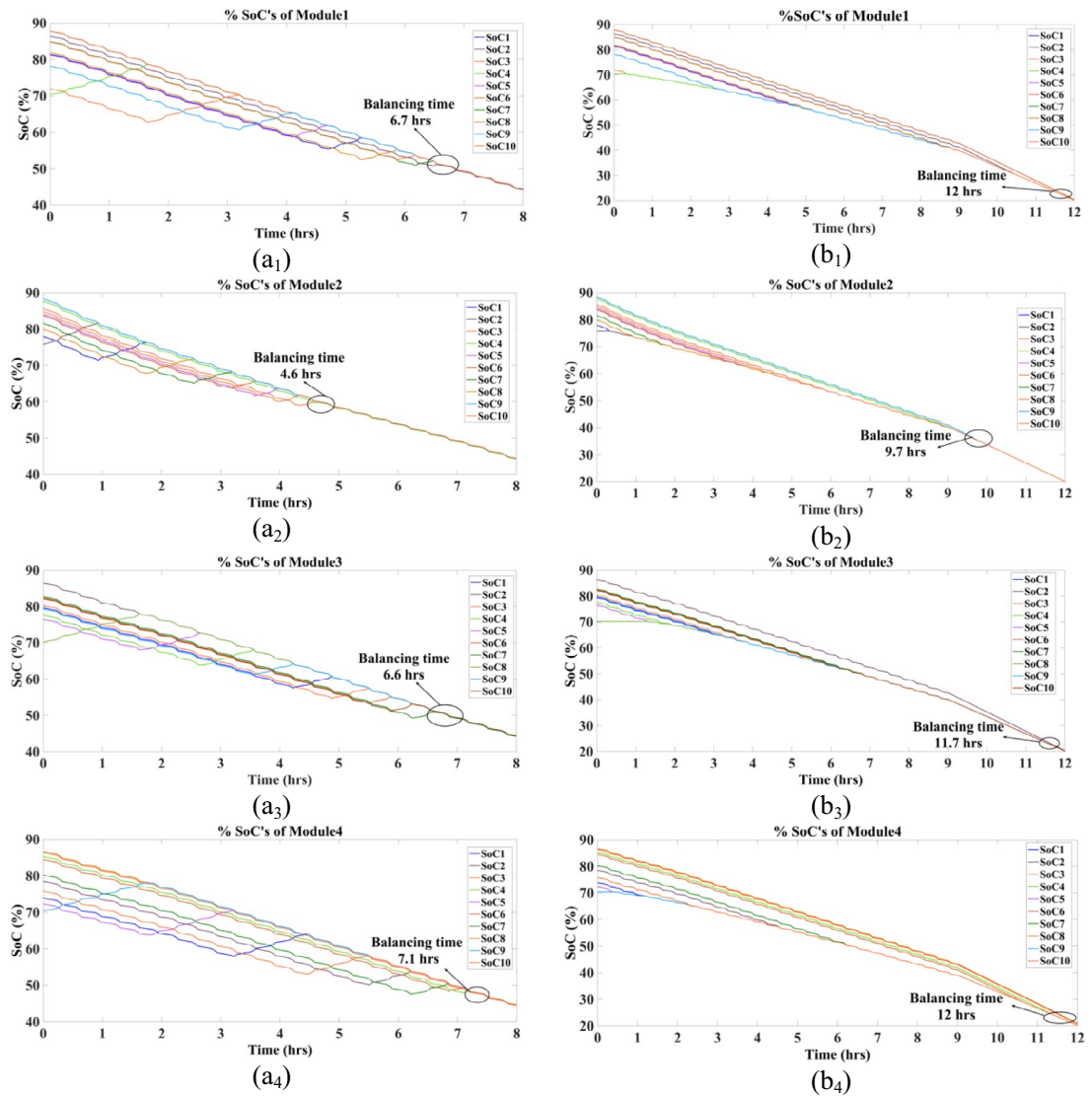
(Panasonic NCR18650) configuration; 3.35 Ah nominal and 3.6 V nominal voltage. Cells are interconnected in series using an H-bridge circuit (using two MOSFETs) positioned around each cell as shown in Fig. 16. Note: The final experimental setup will comprise 16 cells arranged in 4 modules in series.

A TMS320F28379D is chosen as the Microcontroller Unit (MCU) and MATLAB/Simulink software is used to program MCU. The INA117p are used for voltage measurement, and two TMCS1108 are used for current detection (one current sensor is used to calculate the current of the lowest SoC cell that is bypassed or selected to transfer energy to charge the other cells in series for balancing operation through a DC–DC converter, another current measurement is used to detect the current in each serially connected cell). The initial SoCs of the four cells are 33.8%, 34.0%, 35.0% and 36.0%, respectively. In Fig. 16, 12-bit ADCs are employed to measure current and cell voltages at each time step to implement converter control and the SoC balancing algorithm. Additionally, a shift register (serial-in, parallel-out) is utilized to address the limitation in the no. of digital signal pins.

The results in Fig. 17 shows that the battery pack can converge to a balanced state utilizing the H-DCB circuit. After analysing the cell SoCs, the balancing algorithm discovered that cell<sub>1</sub> had the highest SoC (36.0%), while cell<sub>4</sub> had the lowest SoC (33.8%). As a result, the lowest SoC cell<sub>1</sub>, which has been bypassed and charged via a DC–DC converter, receives its energy from the pack (module). The balancing process continued until all the cells in the string had the same SoC of 33.2% with a small difference in SoC (0.02%) is achieved. From Fig. 17, it can be seen that all SoCs are converged at 6.6 min. Table 6 shows the nominal specification for the Li-ion cells.

During the discharging operation, the voltage of each cell lies between 4 to 4.2 V as shown in Fig. 18a, and the charging/discharging current for each cell is depicted in Fig. 18b. Additionally, the switching of each cell is depicted in Fig. 19, where the lowest SoC cell assigned as signal 0 and for remaining cells the signal is assigned as 1 until it reaches to highest SoC cell.





**Figure 14.** SoCs of each module (a) Proposed H-DCB topology. (b) Conventional DCB topology.

## Conclusion

This paper proposed a novel H-DCB technique in BMS that is implemented to achieve SoC balancing among serially connected cells in the battery pack. The integration of each cell with the proposed H-DCB circuit resulted in a reduction in balancing time and losses. Cell equalization was accomplished by employing an H-bridge circuit and a DC–DC converter to/from transfer energy from the highest/lowest SoC cell to/from the pack, bypassing it during charging and discharging mode. Integrating DCB with the CTP balancing method has substantially reduced the time required to reach the SoC balancing convergence point among cells/modules, as opposed to relying solely on the DCB circuit. The novel approach has been validated using simulation modelling in MATLAB/Simulink. The simulation results have illustrated the effectiveness of the proposed balancing strategy, with the SoC balancing convergence point for the cells/modules successfully reached in approximately 6.0 h. When the DCB has worked without a CTP strategy an increment in SoC convergence length of 3.2 h has been observed. While the cells have not yet reached the SoC balancing convergence point, the modules attained balancing after 5.5 h. The effectiveness of the proposed strategy is also validated by hardware setup. It can be observed through the experimental results that four serially connected cells having 2.2% difference between the highest and lowest initial SoCs, the SoC balancing convergence point is achieved after 400 s. The suggested balancing circuit, therefore, extends the life of the battery pack and prevents the highest SoC cell from being repeatedly charged and discharged as in the CTP balancing architecture. Additionally, damaged cells can be removed permanently

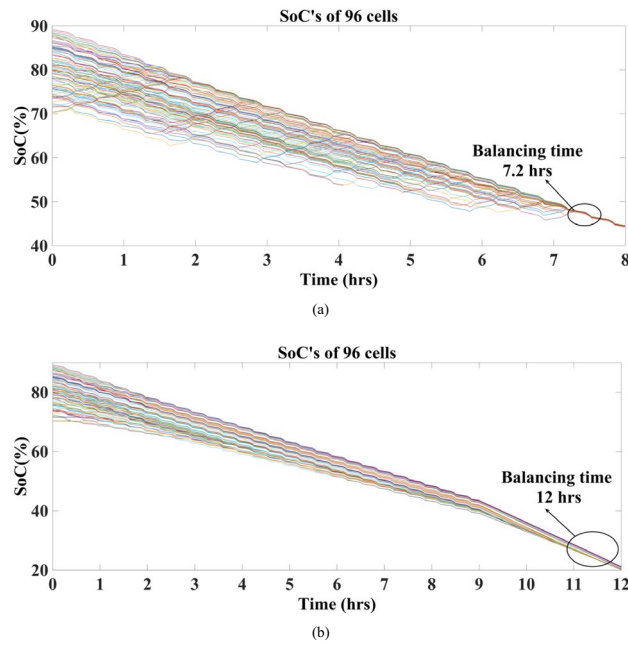


Figure 15. SoCs of 96 cells during discharging operation (a) H-DCB topology (b) DCB topology.

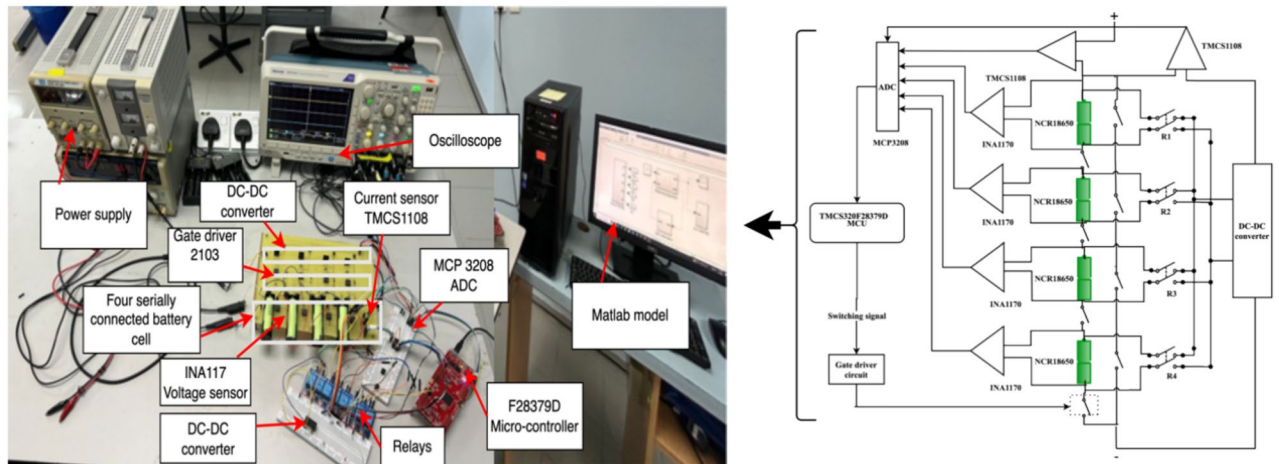


Figure 16. Experimental circuit design.

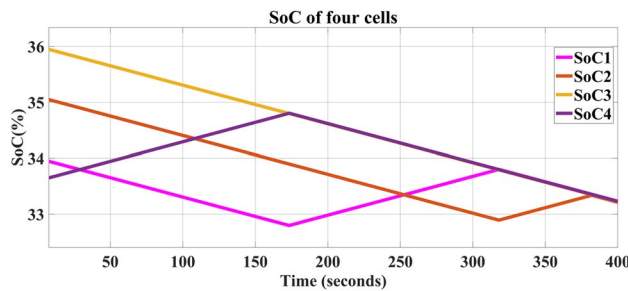
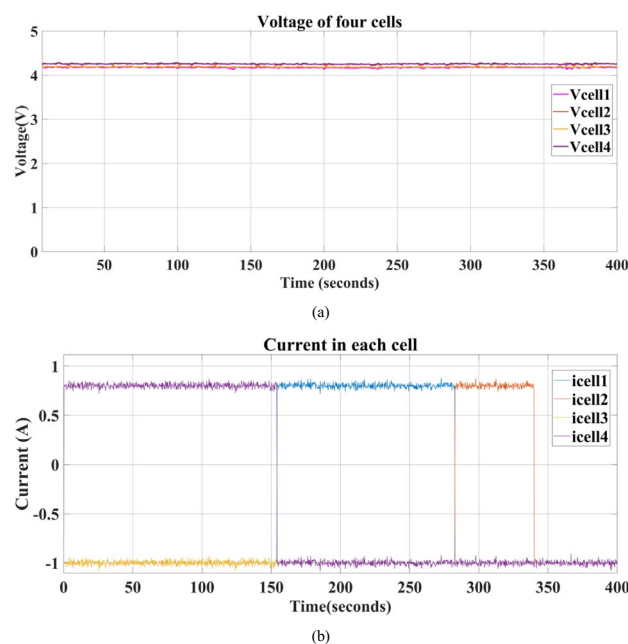


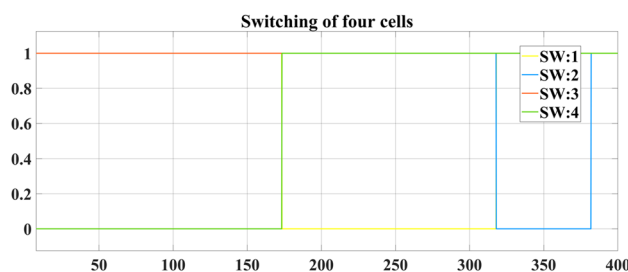
Figure 17. Experiment results of proposed SoC balancing method.

Model	Nominal capacity	Nominal voltage	Charging current	Internal resistance
18650b	3350 mAh	3.6 V	1625 mA	0.07–0.09

**Table 6.** Characteristics of 18,650 Li-ion cell.



**Figure 18.** (a) The voltage of each cell (b) charging/discharging current of each cell.



**Figure 19.** Switching of each cell.

without affecting the operation of the entire balancing circuit. Furthermore, the proposed H-DCB circuit can be used to address SoC balancing among cells.

The goal of future work will be to improve the suggested topology and reduce control complexity by adding different balancing circuits (CTC, PTC, and CTPTC) to utilize the bypassed cell in the DCB circuit as well as the inclusion of redundant cells should be considered to meet the voltage requirement of EVs. Also, more work is needed to improve the SoC estimation's accuracy. In addition, state-of-health (SoH), capacity fading, temperature, and change in internal resistance should be included as additional parameters in the existing balancing controller.

### Data availability

Data is provided within the manuscript.

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N.K.: Conceptualisation, Formal analysis, Methodology, Investigation, Writing—original draft, Visualisation; C.A.O.: Conceptualisation, Writing—review & editing, Resources, Project administration, Supervision; S.: Methodology, Investigation; A. A.: Review & editing, Resources; M. K.B.M.D: Review paper & editing; M.A.: Methodology & Investigation; A.B.A.: Review & editing; M.I.K.: Review.

## Competing interests

The authors declare no competing interests.

## Additional information

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