scientific reports

Check for updates

OPEN

Hysteretic temperature dependence of resistance controlled by gate voltage in $LaAlO_3/SrTiO_3$ heterointerface electron system

Yongsu Kwak[1,2], Woojoo Han[1,3], Joon Sung Lee[4], Jonghyun Song[2,5]✉ & Jinhee Kim[1]✉

For two-dimensional electron gas device applications, it is important to understand how electrical-transport properties are controlled by gate voltage. Here, we report gate voltage-controllable hysteresis in the resistance–temperature characteristics of two-dimensional electron gas at $LaAlO_3$/$SrTiO_3$ heterointerface. Electron channels made of the $LaAlO_3/SrTiO_3$ heterointerface showed hysteretic resistance–temperature behavior: the measured resistance was significantly higher during upward temperature sweeps in thermal cycling tests. Such hysteretic behavior was observed only after application of positive back-gate voltages below 50 K in the thermal cycle, and the magnitude of hysteresis increased with the applied back-gate voltage. To explain this gate-controlled resistance hysteresis, we propose a mechanism based on electron trapping at impurity sites, in conjunction with the strong temperature-dependent dielectric constant of the $SrTiO_3$ substrate. Our model explains well the observed gate-controlled hysteresis of the resistance–temperature characteristics, and the mechanism should be also applicable to other $SrTiO_3$-based oxide systems, paving the way to applications of oxide heterostructures to electronic devices.

Since the discovery of a two-dimensional electron gas (2DEG) at the all-oxide $LaAlO_3$ (LAO)/$SrTiO_3$ (STO) heterointerface and the ensuing exploration for its various novel properties such as superconductivity[1], ferromagnetism[2,3] and strong spin–orbit coupling[4], there has been a flurry of study to uncover the origin of such peculiar characteristics and their correlations. The efforts have been paid for by inventions of new devices; the LAO/STO heterostructure is as a strong candidate for novel application in electronics because the discovered properties are gate-tunable. For example, superconductor-to-insulator transition, phase diagram similar to those of high-temperature superconductors[5] and Lifshitz transition[6] have been observed via back-gate biasing across the gate insulator single crystal STO that has a high dielectric constant. The gate-controllability of physical properties via STO substrate was also shown in other STO-based 2DEG systems such as γ-Al_2O_3/STO[7], LAO/$La_{1-x}Sr_xMnO_3$/STO[8], $CaZrO_3$/STO[9]. In addition, the two-dimensional property of electrical channels in those systems allows the devices to be significantly reduced in thickness, which is another advantage of these 2DEG systems[10].

The band insulator STO used as the substrate of LAO/STO heterostructure is one of the key elements for the formation of a 2DEG. According to the polar catastrophe scenario, whether the interface has *n*-type or *p*-type carriers after electronic reconstruction is determined by the termination of the STO substrate surface[11]. Experimentally, 2DEGs (two-dimensional hole gases, 2DHGs) showing *n*-type (*p*-type) properties were found at the interface between LAO and TiO_2 (SrO) terminated STO[12,13]. Additionally, oxygen vacancies, strain, and the structural phase transition of STO have been reported to affect the properties of the 2DEG[14–19]. A notable peculiarity in properties of STO is that the bulk STO undergoes a structural phase transition from cubic to tetragonal at 105 K. Kalisky et al. observed that the domain structure, attributed to the direction of TiO_6

[1]Korea Research Institute of Standards and Science, Daejeon 34113, South Korea. [2]Department of Physics, Chungnam National University, Daejeon 34134, South Korea. [3]Department of Nanoscience, University of Science and Technology, Daejeon 34113, South Korea. [4]Display and Semiconductor Physics, Korea University Sejong Campus, Sejong 30019, South Korea. [5]Institute of Quantum Systems (IQS), Chungnam National University, Daejeon 34134, South Korea. ✉email: songjonghyun@cnu.ac.kr; jinhee@kriss.re.kr

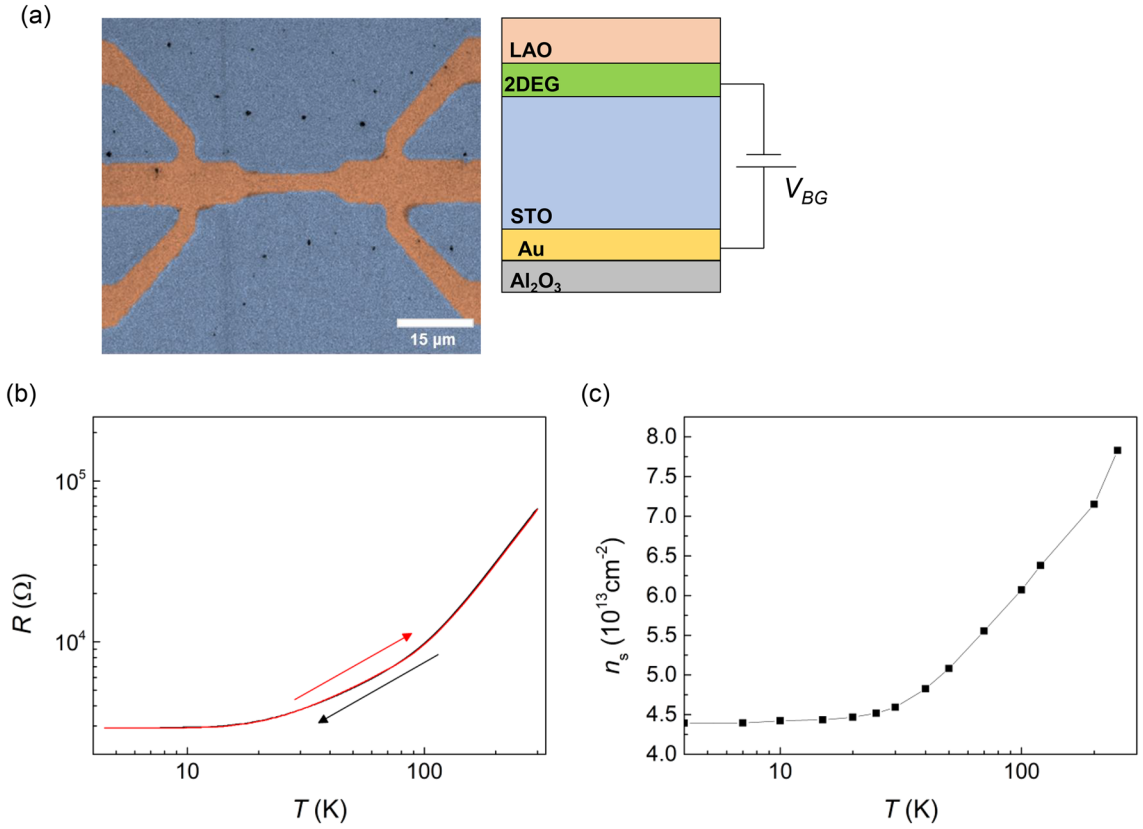

Figure 1. (**a**) SEM image of the Hall bar-patterned device. Inset shows schematic device cross section with a metallic back-gate electrode. In gating experiments, V_{BG} was applied between Au and 2DEG electrodes. (**b**) Temperature dependence of resistance for cool-down and warm-up processes with no V_{BG} applied. (**c**) Temperature-dependent carrier density for the cool-down process with $V_{BG}=0$ V.

octahedral rotation via the phase transition, caused an inhomogeneous electrical transport showing locally enhanced conductivity near the domain boundaries[17]. Because the domain boundaries were formed randomly after each cubic-to-tetragonal phase transition, electrical transport was sensitive to thermal cycling above the structural phase transition temperature[2,17].

The domain boundary effect was especially pronounced in patterned devices with dimensions comparable with or smaller than the typical domain size. Anisotropic electrical resistance was observed in the patterned devices with domain walls inside, and there was a hysteresis in the temperature *versus* resistance loop measured during the cool-down and warm-up processes[18]. The hysteresis of electrical resistance was reported to be maximized in nanoscaled devices[19]. However, considering the fact that the domain structure will remain the same when the temperature is cycled within the temperature range below the phase transition point ($T\sim105$ K)[17], the domain wall mechanism suggested in the previous studies does not fully explain the observed hysteric behavior in resistance.

Here, we investigate the hysteretic behavior in the temperature-dependent resistance ($R(T)$) of a microscale Hall bar-patterned LAO/STO device. It is found that application of gate voltages causes hysteresis in the $R(T)$ loop, and the magnitude of hysteresis increases with the applied positive gate voltage. To explain the observed $R(T)$ loop, we introduce a model that relates the $R(T)$ hysteresis to the temperature-dependent dielectric constant of STO, and to electron trapping within the STO substrate.

Results and discussion

Figure 1a shows a top-view SEM image and a cross-sectional schematic of the device. The hall bar-patterned device was fabricated by using photolithography and Ar-ion milling on a LAO/STO sample grown by pulsed laser deposition. After the fabrication, the back-gate electrode was prepared by directly attaching a gold film deposited on an Al_2O_3 single crystal plate to the bottom surface of the STO substrate using a silver paste. Therefore, as shown in Fig. 1a, the Au electrode was sandwiched between the bottom of the STO substrate and Al_2O_3 single crystal, and was used to apply back-gate voltage (V_{BG}) to investigate the gate dependence of resistance. The Al_2O_3 plate was used for electrical insulation.

Figure 1b shows the inherent temperature dependence of resistance with no back-gate voltage applied. The resistance shows metallically decreasing behavior with lowering temperature, and there is no hysteresis in $R(T)$ between the cool-down and the warm-up processes. This ensures that our experimental instruments, such as the temperature control system and the gate voltage source, do not cause any problem that may result in false hysteresis or anomalies in $R(T)$. Figure 1c shows temperature dependence of the carrier density for $V_{BG}=0$ V.

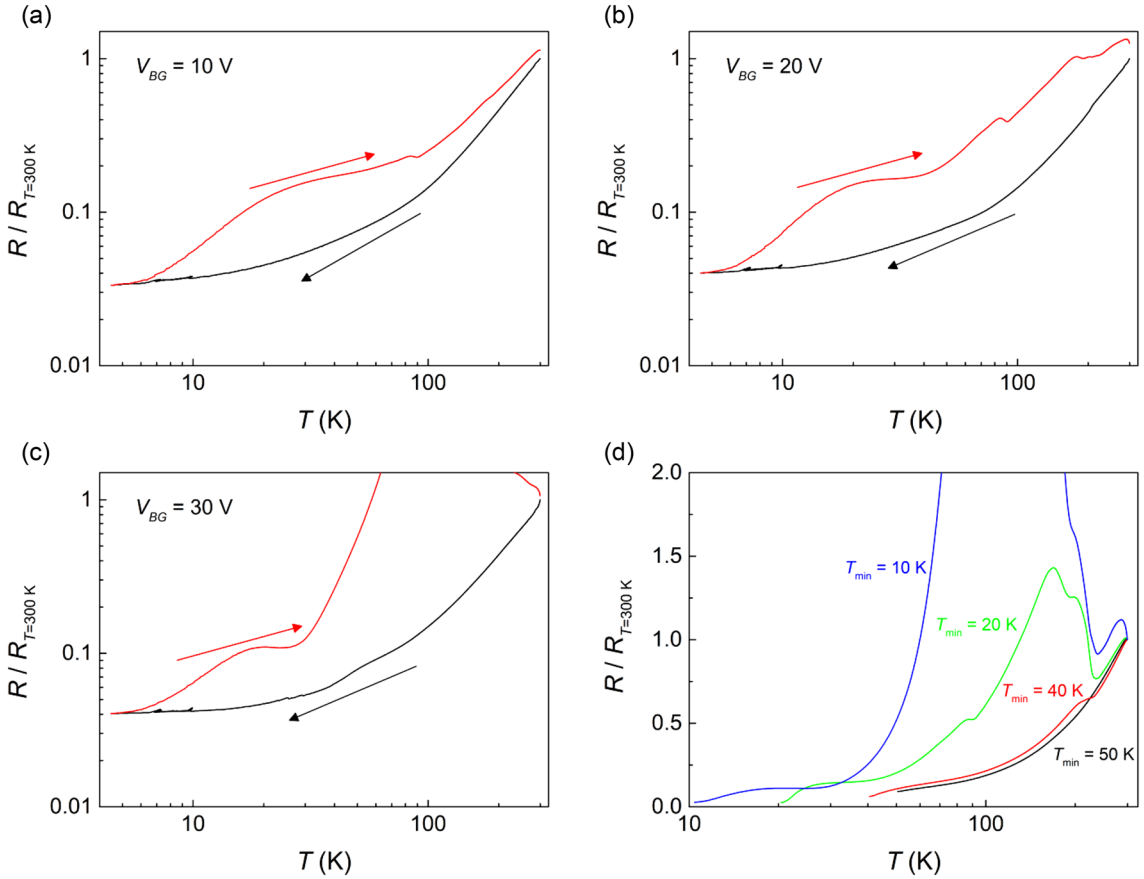

Figure 2. Temperature dependence of the normalized resistance ($R(T)/R_{T=300\,K}$) for cool-down and warm-up processes with (**a**) $V_{BG}=10$ V, (**b**) $V_{BG}=20$ V, (**c**) $V_{BG}=30$ V. Black and red curves show $R(T)/R_{T=300\,K}$ for cool down and warm-up processes, respectively. (**d**) $R(T)/R_{T=300\,K}$ for several warm-up process at $V_{BG}=30$ V with various T_{min}, where T_{min} is the target base temperature for the preceding cool-down sequence from room temperature.

The carrier density is changed from 8×10^{13} cm^{-2} to 4.5×10^{13} cm^{-2} with lowering temperature. At $T=4$ K, the carrier density is higher than 1×10^{13} cm^{-2}, a value known as the Lifshitz transition point[6].

To investigate if a resistance hysteresis occurs when V_{BG} is applied, $R(T)$ for both cool-down and warm-up processes were measured. Figure 2a–c show the temperature dependence of the normalized resistance ($R(T)/R_{T=300\,K}$) measured under different applied V_{BG}. During the cool-down processes, $R(T)/R_{T=300\,K}$ shows metallic property for all V_{BG}, similar to that for $V_{BG}=0$ V. On the other hand, during the warm-up processes, anomalous $R(T)/R_{T=300\,K}$ showing hysteric behavior are observed. In the lowest temperature range, that is, while the temperature is warmed from 4 to 6 K, $R(T)/R_{T=300\,K}$ are similar to those obtained during the cool-down. However, the $R(T)/R_{T=300\,K}$ curves start to deviate from the respective cool-down curves above 6 K, and the deviation intensifies with increasing temperature: the values of resistance are higher than those measured during the cool-down. Furthermore, the $R(T)/R_{T=300\,K}$ for the warm-up processes show some common features which can be summarized as follows. First, when the applied V_{BG} is higher, the difference in the normalized resistance between the cool-down and warm-up processes becomes larger. Second, smooth decreases of the slope of $R(T)/R_{T=300\,K}$ curve are observed from $T=20$ K during the warm-up, and sudden decreases immediately followed by recoveries in resistance are observed at a higher temperature around $T=80$ K. Third, even though there is a hysteresis in $R(T)/R_{T=300\,K}$, the values of resistance near room temperature approach a single value ($\sim10^5\ \Omega$) irrespective of the process history.

Figure 2d shows the dependence of $R(T)/R_{T=300\,K}$ on the minimum temperature (T_{min}) measured for several warm-up processes with a common $V_{BG}=30$ V, where T_{min} is the target base temperature to which the device is cooled down from room temperature. To obtain the data in Fig. 2d, the temperature was lowered to T_{min}, then $R(T)$ was measured while increasing the sample temperature from T_{min} to room temperature. The same experimental procedure was repeated for several different T_{min}. As shown in Fig. 2d, $R(T)/R_{T=300\,K}$ with $T_{min}=50$ K is qualitatively similar to that obtained with $V_{BG}=0$ V (Fig. 1b). On the other hand, when T_{min} is below ~ 40 K, strongly increased $R(T)/R_{T=300\,K}$ is observed for warm-up sequences, and the magnitude of hysteresis increases with decreasing T_{min}.

Experimental results similar to that shown in Fig. 2 have been reported not only for LAO/STO[19] but also for $SrNbO_3$/STO[20], while we also have observed a similar $R(T)$ hysteresis from STO/LAO/STO trilayer (see Fig. S1

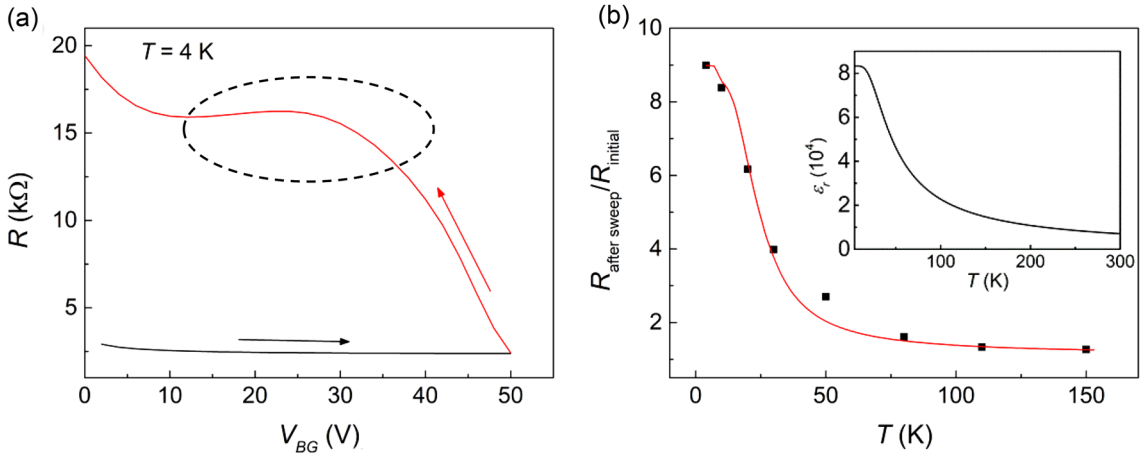

Figure 3. (**a**) V_{BG} dependence of the resistance at 4 K. Black (red) line shows the gate voltage-dependent resistance with increasing (decreasing) V_{BG} from 0 V (50 V) to 50 V (0 V). (**b**) Black squares represent the ratio of resistance after gate sweeping at $V_{BG}=50$ V ($R_{\text{after sweep}}$) to resistance without any gate voltage (R_{initial}). The red line is a curve fitted based on the revised empirical formula. The temperature-dependent dielectric constant in the inset (obtained from Barrett's formula)[30] and $V_{BG}=50$ V were used for the curve fitting. We obtained the following parameters for a 95% confidence interval: $\alpha=200\pm35$ V, $\beta=0.9\pm0.18$, $n_0=(1.3\pm0.17)\times10^{14}$ cm^{-2}.

in supplementary). These previous studies argue that the observed resistance hysteresis is originated from the domain walls created by the cubic-to-tetragonal structural phase transition of STO at $T=105$ K. Furthermore, it is also claimed that the formation of domain wall network at low temperatures causes the 2DEG to change from metal to insulator with increasing temperature, only for the devices with nanoscale channel width[19]. If the domain wall structure is an important factor of the $R(T)$ hysteresis, it should be observed randomly[18] and also should be sensitive to thermal cycling, when the electron channel of the LAO/STO device is laterally confined within the typical domain size. However, the hysteresis in $R(T)$ was always observed whenever we applied positive V_{BG} on the device and lowered the sample temperature below 50 K. Considering these observations, especially the influence of V_{BG} on the hysteresis, we propose that the dielectric characteristic of STO, rather than domain walls, is the main origin of the hysteretic behavior of $R(T)$. This idea is also supported by the fact that T_{min} being less than 50 K is essential for the hysteresis to occur, as shown in Fig. 2d. If the domain wall were the main cause of the resistance hysteresis, we should have observed a small or little dependence of hysteresis on T_{min}, owing to the fact that the structural phase transition of STO occurs at $T=105$ K.

To figure out the detailed effect of V_{BG} at the lowest temperature, which is the turning point of the thermal cycling processes in Fig. 2a–c, we measured the sample resistance while sweeping V_{BG} in forward and backward directions at $T=4$ K. Here, the forward sweep (backward sweep) was carried out by changing V_{BG} from 0 V (50 V) to 50 V (0 V). Figure 3a shows the V_{BG} dependence of resistance, which is strongly hysteretic: the measured resistance was much larger for the backward sweep than for the forward sweep. As is indicated by a dotted circle in Fig. 3a for the backward sweep of V_{BG}, the increasing trend of resistance with decreasing V_{BG} subsides and $R(V_{BG})$ forms a depression between $V_{BG}=30$ V and 10 V. We should note that this retracing curve of $R(V_{BG})$ is similar to the shape of $R(T)/R_{T=300\text{ K}}$ observed near $T=20$ K during the warm-up process in Fig. 2. This suggests that the observed hysteresis of $R(T)/R_{T=300\text{ K}}$ in Fig. 2 is closely related to the hysteretic behavior of resistance shown in Fig. 3a, which took place just by sweeping V_{BG} to and back from a positive value.

To investigate the relationship between the hysteresis in the $R(T)$ and $R(V_{BG})$ in Figs. 2 and 3, we used a planar capacitor model[21] where the electron density injected by applying V_{BG} is described as $\varepsilon_0\varepsilon_r V_{BG}/ed$, where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of STO, e is the electron charge, and d is the thickness of the STO substrate. Considering that the dielectric constant ε_r of STO increases drastically at low temperatures, it can be seen that sweeping down the temperature under a fixed V_{BG} plays a role that is similar to a V_{BG} sweep with regard to the injected electron density. Thus, it can be deduced that the hysteretic $R(T)$ phenomenologically arises from the same origin with that for the hysteretic $R(V_{BG})$ at a fixed temperature. Therefore, it is necessary to figure out the origin of hysteresis in the $R(V_{BG})$ to understand the hysteresis of $R(T)$.

It has been reported by Yin et al. that the gate-dependent resistance of LAO/STO shows a similar hysteretic behavior, which has been attributed to electron trapping that results in a difference in the electron density of 2DEG between the forward and backward V_{BG} sweeps[22]. When V_{BG} is swept, the amount of total injected electrons during the forward sweep should be same with the amount of removed electrons during the backward sweep. During the forward sweep, electrons are injected into the 2DEG channel and the impurity sites as well. In the backward sweep, on the other hand, electrons are removed only from the 2DEG because the electrons trapped at the impurity sites are energetically more stable. As a result, the electron density of 2DEG after a V_{BG} sweep is decreased as much as the trapped electron density (n_{tr}). In that report, the trapped electron density is described by an empirical formula, $n_{tr}=n_0\{1-\exp(-V_{BG}/\alpha)\}$, where n_0 is the maximum electron density that can be trapped at the impurity sites, and α is a fitting parameter for each sample. However, it is not possible to correlate the hysteresis in $R(T)$ to the trapped electrons using that empirical formula, because the influence of the dielectric

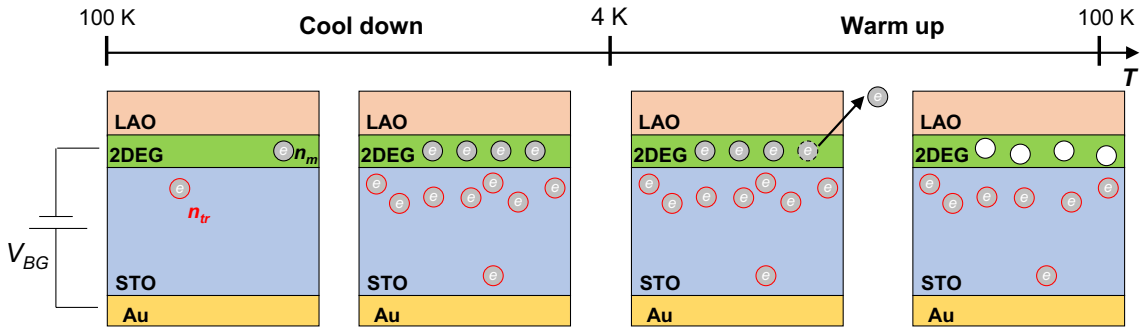

Figure 4. Schematic of our model for the $R(T)$ hysteresis. During the cool-down process, the temperature-dependent dielectric constant of STO makes n_{tr} and n_m to be increased even though a fixed positive V_{BG} is applied throughout. For the warm-up process, the electrons that have been injected into the 2DEG, as well as preexisting electrons, are removed prior to the electrons injected and trapped at impurity sites, owing to the said temperature dependence of dielectric constant.

constant of STO substrate is not factored in. Since the injected electron density in the planar capacitor model is proportional to the electric displacement, which is dependent not only on V_{BG} but also on the temperature via $\varepsilon_r(T)$, we modified the above formula into $n_{tr} = n_0\{1 - \exp(-\varepsilon_r(T)V_{BG}/\varepsilon_r(0)\alpha)\}$, which becomes practically identical to the original formula when the temperature is fixed 0 K. The use of $\varepsilon_r(0)$ instead of $\varepsilon_r(T_{min})$ is just for simplicity; any difference between the two values will be compensated by the fitting parameter α.

To confirm the reliability of this revised formula for description of electron trapping at impurity sites, we fit the temperature dependence of the resistance ratio, that is $R_{\text{after sweep}}/R_{\text{initial}}$, where $R_{\text{after sweep}}$ is the resistance measured after a V_{BG} sweep up to 50 V and R_{initial} is that measured before the application of V_{BG}. Considering that the electron density of 2DEG decreases to $(n_{in} - n_{tr})$ after a V_{BG} sweep due to the electron trapping, $R_{\text{after sweep}}/R_{\text{initial}}$ equals $\mu_{in}n_{in}/\{\mu_{\text{after sweep}}(n_{in} - n_{tr})\}$ according to the Drude formula $(R = 1/ne\mu)$, where n_{in}, μ_{in}, and $\mu_{\text{after sweep}}$ are the initial electron density, the initial mobility, and the mobility after the V_{BG} sweep of the 2DEG, respectively. Assuming that $\mu_{\text{after sweep}} = \mu_{\text{in}}\beta$, where β is another fitting parameter and n_{tr} is described by the revised empirical formula, the measured $R_{\text{after sweep}}/R_{\text{initial}}$ is fit by using the parameters: $\alpha = 200$ V, $\beta = 0.9$, and $n_0 = 1.3 \times 10^{14}$ cm^{-2}. Figure 3b shows the temperature dependence of $R_{\text{after sweep}}/R_{\text{initial}}$ along with the fitted curve. The conformity of the fitting result demonstrates that the revised empirical formula correctly reflects the effect of electron trapping at the impurity sites throughout the experimental temperature range. This also indicates that the hysteretic $R(T)$ is owing to the electron trapping caused by application of V_{BG}, along with the strongly temperature-dependent dielectric property of STO[23].

Now we present an explanation for the observed hysteresis in $R(T)$. When a positive gate voltage is applied, electrons are injected not only into the 2DEG but also into the impurity sites, as is explained above. The electron density injected into the impurity sites (n_{tr}) is described by the revised empirical formula with the constraint of $n_m + n_{tr} = \varepsilon_0\varepsilon_r V_{BG}/d$ from the planar capacitor model[21], where n_m is the injected electron density in the 2DEG and thus stays itinerant. When the device is cooled down with an applied gate voltage, increasing dielectric constant of the STO with lowering temperature causes n_m and n_{tr} to be increased (see Fig. 4). This does not change the metallic property of $R(T)$ for the cool-down process. On the other hand, when the device is being warmed up after the cool-down, the injected electrons should be removed due to the decreased dielectric constant of the STO with increasing temperature. However, because the electrons trapped at the impurity sites are energetically stable, the itinerant electrons at the 2DEG are removed prior to the trapped electrons, as in the case of the V_{BG} sweep in Fig. 3a. As a result, there occurs a difference in the electron density of 2DEG between the cool-down and warm-up processes, which produces the observed resistance hysteresis. At higher temperatures ($T \geq 250$ K), the resistance values measured during the warm-up process approach those measured during the cool-down, as a greater part of the trapped electrons can now escape due to the thermal effect[22,24].

The above scenario provides a good explanation of the V_{BG} dependence of the observed resistance hysteresis intensity shown in Fig. 2a–c. It also rationalizes well the T_{min} dependence of resistance hysteresis shown in Fig. 2d, in the light of the dielectric constant of STO that increases with decreasing temperature especially rapidly below 50 K. Since the temperature dependence of the dielectric constant of STO is the key factor of the $R(T)$ hysteresis, similar gate-dependent $R(T)$ hysteresis is expected to occur commonly in STO-based 2DEG devices.

As a final remark, we comment on the differences and improvements of our model from preexisting explanations for the resistance hysteresis in LAO/STO. Some of previous studies pointed out the domain boundary structure as the main cause of the resistance hysteresis[18–20] However, the data shown in Fig. 2 reveals that the $R(T)$ hysteresis starts to develop from as low as 6 K, which is much lower than the structural phase transition temperature 105 K. Our model provides a good rationale of this experimental observation. There have been a number of experimental studies on the V_{BG}-dependent hysteretic resistance at fixed temperatures that attribute the gate hysteresis to electron trapping[22,24–29]. In this work, we introduce the dramatically strong temperature dependence of dielectric constant of the quantum paraelectric STO into the picture of gate hysteresis by electron trapping, and develop a model that successfully reproduces the observed $R(T)$ hysteresis. We further infer that the channel width dependence of $R(T)$ hysteresis reported previously[19] may be explained partly in terms of stronger focusing of the gating field near a narrower channel.

Conclusion

We studied gate voltage-controllable hysteresis in the resistance–temperature characteristics of two-dimensional electron gas at $LaAlO_3/SrTiO_3$ heterointerface. Without an applied gate voltage, the $R(T)$ curves measured during cool-down and warm-up processes were almost the same. However, a hysteresis in $R(T)$ was manifest after applying a gate voltage, and its intensity was increased by increasing the applied gate voltage V_{BG}. The magnitude of the hysteresis also increased with lowering the base temperature of the cool-down process. These observations of resistance hysteresis were explained in terms of electron injection into the 2DEG conduction channel at the LAO/STO heterointerface and electron trapping at the impurity sites of STO substrate. In the presented scenario, the strongly temperature-dependent dielectric constant of STO plays an important role. We believe that our model of gate-dependent $R(T)$ hysteresis can also be applied to interpretation of electrical transport in other STO-based devices, and may lead to better control over the device properties.

Methods

$LaAlO_3$ thin films growth. Before deposition of LAO, TiO_2-terminated STO was annealed to obtain an atomically flat terrace on the STO surface at 950 °C under oxygen partial pressure of 2×10^{-5} Torr for two hours. The LAO thin film of 8 unit-cells was deposited on the TiO_2-terminated STO by using pulsed laser deposition at 750 °C under oxygen partial pressure of 10^{-5} Torr. For the deposition, a KrF excimer laser with an energy of 120 mJ and a repetition rate of 4 Hz was used. After the LAO layer deposition, the sample was maintained in an oxygen partial pressure of 500 mTorr at 750 °C for 30 min and cooled down from 750 °C to room temperature.

Electrical transport measurements. $R(T)$ was measured during cool-down from room temperature to minimum temperature (T_{min}) and the subsequent warm-up. The temperature was changed at a rate of 3 K/min, while applying a back-gate voltage to the electrode coated on the back-side surface of STO. The temperature was controlled by Quantum Design PPMS, and the sample resistance was measured using standard lock-in techniques.

Received: 4 November 2021; Accepted: 7 April 2022
Published online: 19 April 2022

References

1. Reyren, N. *et al.* Superconducting interfaces between insulating oxides. *Science* **317**, 1196–1199 (2007).
2. Ngo, T. D. N. *et al.* Polarity-tunable magnetic tunnel junctions based on ferromagnetism at oxide heterointerfaces. *Nat. Commun.* **6**, 8035 (2015).
3. Ariando, *et al.* Electronic phase separation at the $LaAlO_3/SrTiO_3$ interface. *Nat. Commun.* **2**, 188 (2011).
4. Caviglia, A. D. *et al.* Tunable Rashba spin-orbit interaction at oxide interfaces. *Phys. Rev. Lett.* **104**, 126803 (2010).
5. Richter, C. *et al.* Interface superconductor with gap behaviour like a high-temperature superconductor. *Nature* **502**, 528–531 (2013).
6. Joshua, A., Pecker, S., Ruhman, J., Altman, E. & Ilani, S. A universal critical density underlying the physics of electrons at the $LaAlO_3/SrTiO_3$ interface. *Nat. Commun.* **3**, 1129 (2012).
7. Chen, Y. Z. *et al.* A high-mobility two-dimensional electron gas at the spinel/perovskite interface of γ-$Al_2O_3/SrTiO_3$. *Nat. Commun.* **4**, 1371 (2013).
8. Chen, Y. Z. *et al.* Extreme mobility enhancement of two-dimensional electron gases at oxide interfaces by charge-transfer-induced modulation doping. *Nat. Mater.* **14**, 801–806 (2015).
9. Chen, L. *et al.* Extreme reconfigurable nanoelectronics at the $CaZrO_3/SrTiO_3$ interface. *Adv. Mater.* **30**, 1801794 (2018).
10. Lee, S. R. *et al.* First Observation of ferroelectricity in ~1 nm ultrathin semiconducting $BaTiO_3$ films. *Nano Lett.* **19**, 2243–2250 (2019).
11. Nakagawa, N., Hwang, H. Y. & Muller, D. A. Why some interfaces cannot be sharp. *Nat. Mater.* **5**, 204–209 (2006).
12. Ohtomo, A. & Hwang, H. Y. A high-mobility electron gas at the $LaAlO_3/SrTiO_3$ heterointerface. *Nature* **427**, 423–426 (2004).
13. Lee, H. *et al.* Direct observation of a two-dimensional hole gas at oxide interfaces. *Nat. Mater.* **17**, 231–236 (2018).
14. Brinkman, A. *et al.* Magnetic effects at the interface between non-magnetic oxides. *Nat. Mater.* **6**, 493–496 (2007).
15. Kalabukhov, A. *et al.* Effect of oxygen vacancies in the $SrTiO_3$ substrate on the electrical properties of the $LaAlO_3/SrTiO_3$ interface. *Phys. Rev. B* **75**, 121404 (2007).
16. Bark, C. W. *et al.* Tailoring a two-dimensional electron gas at the LaAlO3/SrTiO3 (001) interface by epitaxial strain. *Proc. Natl. Acad. Sci.* **108**, 4720–4724 (2011).
17. Kalisky, B. *et al.* Locally enhanced conductivity due to the tetragonal domain structure in $LaAlO_3/SrTiO_3$ heterointerfaces. *Nat. Mater.* **12**, 1091–1095 (2013).
18. Goble, N. J. *et al.* Anisotropic electrical resistance in mesoscopic $LaAlO_3/SrTiO_3$ devices with individual domain walls. *Sci. Rep.* **7**, 44361 (2017).
19. Minhas, M. Z., Müller, A., Heyroth, F., Blaschek, H. H. & Schmidt, G. Temperature dependent giant resistance anomaly in $LaAlO_3/SrTiO_3$ nanostructures. *Sci. Rep.* **7**, 5215 (2017).
20. Yan, X., Zhang, H., Shen, B., Hu, F. & Sun, J. Transport abnormity and its modulations via gating effect and light illumination at the $SrNbO_3/SrTiO_3$ interface. *Mater. Res. Express* **7**, 96407 (2020).
21. Novoselov, K. S. *et al.* Electric field effect in atomically thin carbon films. *Science* **306**, 666–669 (2004).
22. Yin, C. *et al.* Electron trapping mechanism in $LaAlO_3/SrTiO_3$ heterostructures. *Phys. Rev. Lett.* **124**, 17702 (2020).
23. Sawaguchi, E., Kikuchi, A. & Kodera, Y. Dielectric constant of strontium titanate at low temperatures. *J. Phys. Soc. Japan* **17**, 1666–1667 (1962).
24. Biscaras, J. *et al.* Limit of the electrostatic doping in two-dimensional electron gases of $LaXO_3$(X = Al, Ti)/$SrTiO_3$. *Sci. Rep.* **4**, 6788 (2014).
25. Bell, C. *et al.* Dominant mobility modulation by the electric field effect at the $LaAlO_3/SrTiO_3$ interface. *Phys. Rev. Lett.* **103**, 226802 (2009).
26. Biscaras, J. *et al.* Two-dimensional superconducting phase in $LaAlO_3/SrTiO_3$ heterostructures induced by high-mobility carrier doping. *Phys. Rev. Lett.* **108**, 247004 (2012).

27. Pallecchi, I. *et al.* Irreversible multi-band effects and lifshitz transitions at the $LaAlO_3/SrTiO_3$ Interface under field effect. *Adv. Electron. Mater.* **7**, 2001120 (2021).
28. Liu, W. *et al.* Magneto-transport study of top- and back-gated $LaAlO_3/SrTiO_3$ heterostructures. *APL Mater.* **3**, 62805 (2015).
29. Lee, J. N., Hou, X., Takahashi, R. & Lippmaa, M. Tuning the carrier density in $SrTiO_3/LaTiO_3/SrTiO_3$ quantum wells. *Appl. Phys. Lett.* **116**, 171601 (2020).
30. Barrett, J. H. Dielectric constant in perovskite type crystals. *Phys. Rev.* **86**, 118–120 (1952).

Acknowledgements

This work was supported by Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (P0008458, The HRD Program for Industrial Innovation), Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2020R1A6A1A03047771), the Max Planck POSTECH/Korea Research Initiative, Study for Nano Scale Optomaterials and Complex Phase Materials (2016K1A4A4A01922028), though NRF funded by MSIP of Korea, NRF grant funded by MSIP (2020R1A2C1011000).

Author contributions

Y.K. and W.H. performed sample growth, measurement. Y.K. wrote the manuscript. J.S.L., J.S. and J.K. contributed to interpretation of the results. J.S. and J.K. supervised the findings of this work. All authors discussed the results and reviewed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary Information The online version contains supplementary material available at https://doi.org/10.1038/s41598-022-10425-3.

Correspondence and requests for materials should be addressed to J.S. or J.K.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.