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Large-area plastic nanogap electronics enabled by adhesion lithography

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Large-area manufacturing of flexible nanoscale electronics has long been sought by the printed electronics industry. However, the lack of a robust, reliable, high throughput and low-cost technique that is capable of delivering high-performance functional devices has hitherto hindered commercial exploitation. Herein we report on the extensive range of capabilities presented by adhesion lithography (a-Lith), an innovative patterning technique for the fabrication of coplanar nanogap electrodes with arbitrarily large aspect ratio. We use this technique to fabricate a plethora of nanoscale electronic devices based on symmetric and asymmetric coplanar electrodes separated by a nanogap < 15 nm. We show that functional devices including self-aligned-gate transistors, radio frequency diodes and rectifying circuits, multi-colour organic light-emitting nanodiodes and multilevel non-volatile memory devices, can be fabricated in a facile manner with minimum process complexity on a range of substrates. The compatibility of the formed nanogap electrodes with a wide range of solution processable semiconductors and substrate materials renders a-Lith highly attractive for the manufacturing of large-area nanoscale opto/electronics on arbitrary size and shape substrates.

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INTRODUCTION

Nanogap electrodes have received significant attention during the last decades and several bottom-up and top-down nanotechnology approaches have been proposed to fabricate coplanar electrodes with a separation reaching atomic scale resolution.¹ However, in recent years, there has been a significant drive from an industrial standpoint to upscale nanogap electrode fabrication at low cost, preferably in ways that are compatible with high-volume printing technologies, while preserving the quality and reliability of these coplanar structures.

We have recently introduced adhesion lithography (a-Lith) as an alternative, scalable, low-temperature, and large-area patterning technique for the fabrication of sub-15 nm coplanar symmetric or asymmetric electrodes.² A-Lith is based on the modification of adhesion forces between two metals, one of which is functionalised with a suitable self-assembled monolayer (SAM). Following our initial report, we have shown its successful application to a number of electronic devices including high-speed Schottky diodes,^{3–5} memristors,⁶ and high-sensitivity photodiodes.⁷ Some variations on the a-Lith approach have also appeared in the literature; these validate its efficacy, reproducibility and broad application potential. More specifically, a-Lith fabricated electrodes combined with SAM-based gate dielectrics have been employed to fabricate molybdenum disulphide (MoS_2) field-effect transistors (FETs).^{8–10} In addition, functionalised CdSe quantum dots have been used in another instance to fabricate large-scale QD-Ag nanogap metamaterials via a similar technique, termed self-assembly lithography.¹¹

Herein, we focus on the development of symmetric and asymmetric coplanar electrodes with inter-electrode distances of < 15 nm and arbitrarily large aspect ratios. This is demonstrated using a variety of different substrate materials and implemented for *proof-of-concept* devices, including self-aligned-gate (SAG) metal oxide transistors, radio frequency (RF) diodes, nanoscale organic light-emitting diodes (nano-LEDs) and non-volatile memory cells. The present work highlights the tremendous versatility and adaptability of a-Lith to different devices of technological interest and demonstrates how it can be easily tailored to satisfy the electrode and substrate material, size and shape requirements posed by targeted applications.

RESULTS

Adhesion lithography (a-Lith)

The a-Lith patterning procedure has been described in detail previously.² Figure 1a (steps 1–5) summarises the main process steps: Deposition and patterning of the first metal (M1) on the substrate of choice is followed by its functionalization with a suitable SAM, which binds to the surface of M1 and then a second metal (M2) is deposited on top. To create the nanogap structures, an adhesive material (tape or glue) is applied over the surface of M2 and is subsequently peeled off either manually or with a semi-automated peeling machine; when a glue is used, it is allowed to set before peeling.³ The adhesive material removes that part of M2 that is in contact with (and weakly adhered to) the SAM-functionalised area of M1, leaving M2 on the areas directly in contact with the substrate. This leads to the fabrication of a

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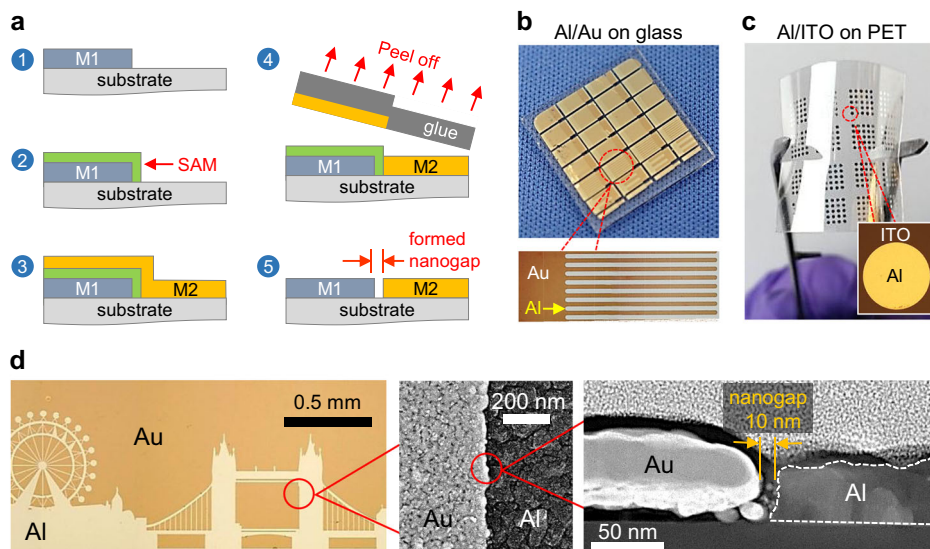


Fig. 1 Development of metal nanogaps via Adhesion lithography. **a** Adhesion lithography (a-Lith) process steps: (1) deposition and patterning of the first metal (M1) on the substrate; (2) application of the self-assembled monolayer (SAM); (3) deposition of the second metal (M2); (4) application of adhesive material and peel-off; and (5) resulting nanogap after SAM removal by oxygen plasma. **b** Low and high-magnification images of coplanar interdigitated Al/Au nanogap electrodes fabricated on glass. **c** Arrays of circular Al/ITO nanogap electrodes fabricated on a PET substrate. **d** Optical micrograph of a London skyline design accompanied by high-resolution (HR) plan-view SEM and cross-section HR-TEM images revealing the presence of a ≈ 10 nm size nanogap

coplanar metal structure, in which the two metals are spatially and electrically isolated by the presence of the SAM along the edge of M1. The lower limit electrode separation is ultimately determined by the SAM's head-to-tail length (herein ≈ 2 nm), although in practice granular fracture of the M2 film during peeling gives rise to somewhat larger separations ≈ 15 nm that are nevertheless highly uniform.^{2,3,5,7} However, we note that closer examination of the inter-electrode spacing has shown that the actual nanogap length is not constant and is characterised by a Gaussian-like distribution with minimum dimensions down to a few nm.² Finally, the SAM is removed, for instance via O_2 plasma or UV-ozone cleaning for a few minutes, leaving an empty nanogap between the two metals.

Figure 1b, c showcase some characteristic examples of the a-Lith process's unique attributes; specifically shown here are nanogap structures of arbitrary length and geometry using different electrode metal combinations (Al/Au and indium tin oxide (ITO)/Al) deposited on different substrate materials, namely glass (Fig. 1b) and polyethylene terephthalate (PET) (Fig. 1c). For reference, Al/Au asymmetric electrode gaps fabricated on PET have been used to demonstrate flexible RF Schottky diodes based on various solution processable semiconductors.⁵ Conversely, Al/Al symmetric electrode air-gaps patterned on plastic substrates have been used to realise semiconductor-free non-volatile memory devices,⁶ while ITO/Al asymmetric structures similar to those shown in Fig. 1c are anticipated to be attractive for certain optoelectronic applications in which semi-transparency is a desired characteristic.

To further highlight the versatility offered by a-Lith in terms of electrode designs, we fabricated a *London skyline* photolithography mask and used it to pattern Al (M1), followed by a-Lith patterning of Au (M2). Figure 1d shows an optical micrograph of this iconic silhouette accompanied by high-resolution scanning electron microscope (SEM) and transmission electron microscope (TEM) cross-section images. From the latter image, a uniform nanogap of <20 nm can easily be identified. The total width (along the electrode edge) of this somewhat irregular asymmetric electrode nanogap is defined by the contour of the London skyline shape and in this particular structure is 10 cm (Note: image in Fig. 1d shows only part of the whole structure). Another way of

controllably scaling the nanogap width is by using interdigitated electrode structures and varying the pitch and finger length, as shown in Fig. 1b. Most importantly the nanogap in all of the above-mentioned structures consistently remains <20 nm.

Self-aligned-gate transistors prepared by a-Lith

For any thin-film transistor (TFT) technology to be compatible with the emerging sector of printed microelectronics, it must satisfy the requirements for simple, scalable and low-temperature processing, while still maintaining high performance.¹² For the transistor channel semiconductor, the use of solution processable metal oxide semiconductors has been attracting mounting interest due to the combination of processing versatility and high carrier mobility; two important prerequisites for commercial applications.^{13–15} A further important performance metric of any emerging TFT technology is the maximum operating frequency, also known as the cutoff frequency.¹⁶ In the case of conventional TFT architectures, such as the one shown in Fig. 2a, the overlap of the gate electrode with the source (S) and drain (D) electrodes gives rise to parasitic capacitance, and hence to a reduced cutoff frequency. A way to circumvent this problem is to employ alternative device architectures, such as the SAG TFT structure. The latter TFTs are characterised by an extremely small overlap between gate and S-D electrodes and hence operate at high frequency compared to conventional TFTs.^{17–19} However, implementing the SAG TFT architecture on large-area substrates is generally costly, typically requiring additional process steps.

We report, here, the use of a-Lith to create SAG transistors (SAG TFTs) with negligible S-D/gate overlap. Our approach takes advantage of the merits of a-Lith to minimise the separation between the S-D and gate (G) electrodes placed within the same plane. The specific steps used to fabricate the a-Lith SAG TFTs using indium oxide (In_2O_3) as the semiconductor are shown in Fig. 2b (steps 1–5). First the aluminium gate (M1) was patterned and functionalised with the octadecylphosphonic acid (ODPA) self-assembled monolayer (SAM-1), then gold (M2) was evaporated through a shadow mask to form the adjacent S-D electrodes. Next, adhesive glue was spread as a film on top and used to remove the

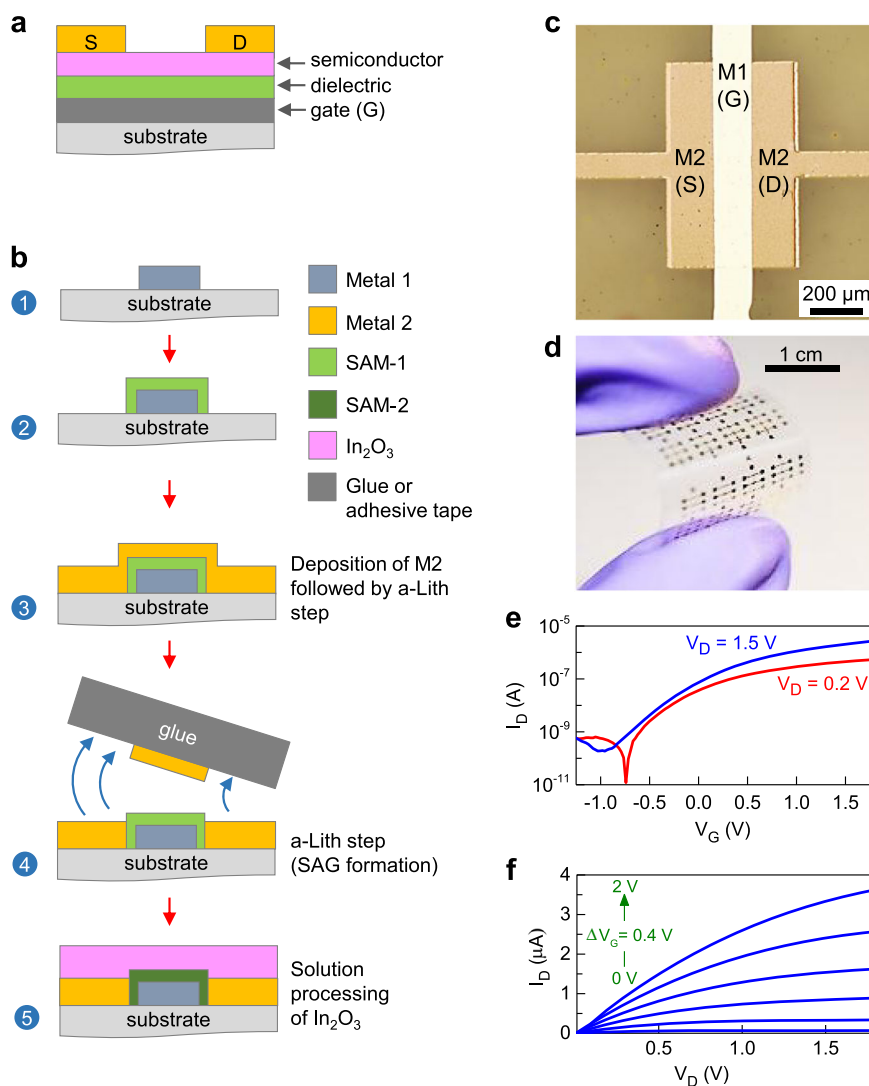


Fig. 2 Patterning of self-aligned gate thin-film transistors using a-Lith. **a** Schematic of a conventional TFT structure characterised by significant Source-Drain/Gate (S-D/G) overlap. **b** Processing steps used to fabricate the self-aligned-gate transistors (SAG TFTs). Resulting devices exhibit negligible S-D/Gate overlap. **c** Optical micrograph of Au source and drain separated by Al gate. **d** Arrays of SAG TFTs fabricated by a-Lith on a flexible PET substrate. **e** Transfer, and **f** output characteristics measured for an In_2O_3 -based SAG TFT with channel width and length of 1 mm and 50 μm , respectively

Au overlapping the ODPDA-coated Al gate, resulting in the formation of a coplanar S/G/D structure (see step 4 schematic in Fig. 2b). The SAM-1 was then removed by exposing the structure to UV- O_3 followed by the selective re-application of a device-performance-preferred SAM-2, namely 1-phosphonohexadecanoic acid (PHDA), onto the thin native alumina (AlO_x) layer atop the aluminium gate electrode. The AlO_x -PHDA combination serves as a hybrid nano-dielectric. TFT fabrication was then completed by spin-coating a thin (≈ 20 nm) In_2O_3 semiconductor layer across the whole structure (Fig. 2b (step 5)). Figure 2c shows an optical micrograph of an actual In_2O_3 SAG TFT fabricated on glass, while Fig. 2d shows an array of In_2O_3 SAG TFTs prepared on flexible plastic substrate.

The resulting In_2O_3 SAG TFTs exhibit low-voltage operation (< 2 V) with typical n-channel behaviour as evident in the transfer and output characteristics shown in Fig. 2e, f, respectively. Device operation is characterised by good on/off current ratios $> 10^3$ and an electron mobility > 2 cm^2/Vs . The latter value is comparable to that measured for conventional In_2O_3 transistor architectures (Fig. 2a) prepared by spin-coating.²⁰ Preliminary measurements of the dynamic response of our SAG TFTs show that, while the rise

time (τ_r) of a conventional In_2O_3 TFT (channel width, W , and length, L , of 1 mm and 50 μm , respectively) was 30 μs for a characteristic S-D/Gate overlap length of 50 μm , the SAG TFTs gave $\tau_r \approx 20$ μs . Although the reduction appears to be somewhat limited here, it may become a more significant factor on further downscaling of the channel length; parasitic effects are then expected to be more detrimental. It is noteworthy that our a-Lith process has recently been adopted by Kawanago et al. to produce MoS_2 -based SAG TFTs with high-performance and low-voltage operation.^{9,10} It is evident that a-Lith holds great promise for the development of SAG TFTs based on a variety of semiconductor materials including conventional thin-film as well as low-dimensional systems.

Radio frequency (RF) diodes

Solution-processed Schottky diodes are important for the field of radio frequency identification (RFID).¹⁶ Recently, we reported on a-Lith enabled flexible C_{60} diodes with cutoff frequencies in the range of hundreds of MHz and ZnO diodes with even higher performance.⁵ While the unique coplanar structure of the diodes allowed for frequency performance suitable for high frequency

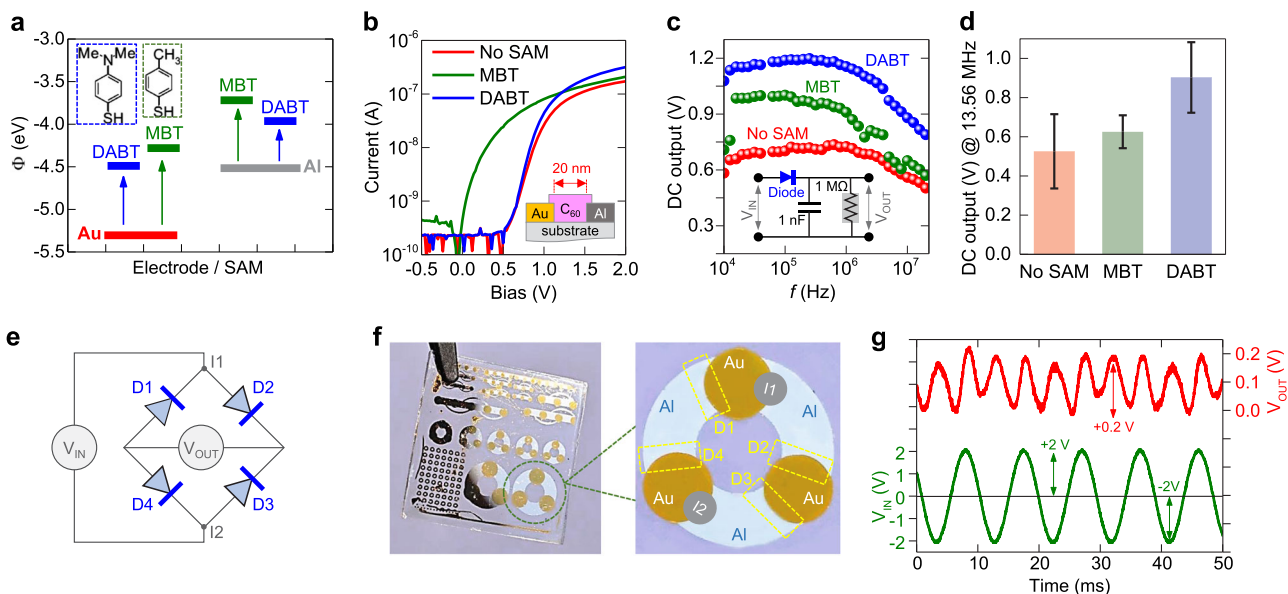


Fig. 3 RF diodes and monolithic full-wave rectifying bridges fabricated via a-Lith. **a** Work function of Au and Al electrodes before and after treatment with DABT and MBT SAMs. Inset: chemical structure of the DABT and MBT molecules. **b** Current-voltage characteristics of C_{60} nanogap diodes with untreated (No SAM) and DABT- and MBT-treated electrodes. Inset: Schematic of device architecture. **c** DC output voltage (V_{OUT}) as a function of input signal frequency (f) measured for C_{60} diodes with untreated as well as DABT- and MBT-treated electrodes. The amplitude of the input signal used in this experiment was ± 3 V. Inset: Half-wave rectifier (HWR) circuit. **d** Column chart of DC V_{OUT} obtained from in total 45 diodes with different surface SAM treatments at 13.56 MHz input signal frequency. Error bars represent standard deviation. **e** Circuit schematic for a full-wave bridge rectifier (FWBR). **f** Lower (left image) and higher (right image) magnification photographs of the fabricated FWBR circuits. **g** V_{OUT} measured for a full-wave rectifier with a 100 Hz sinewave input signal ($V_{IN} = \pm 2$ V amplitude)

(HF) and even ultra-high frequency (UHF) RFID technology, there appears to be significant room for improvement in terms of device performance. Specifically, in order to increase the DC output of the C_{60} rectifier circuit, the voltage drop across the diode should be addressed. We have, therefore, investigated the diode turn-on voltage and its dependence on Au/ C_{60} interface energetics, optimising this interface through selective treatment of the Au electrode. A recent report by Kang et al.²¹ shows that organic diodes can be fabricated to operate at GHz frequencies, although in this case the diode was a conventional normal to plane structure and the pentacene semiconductor was vacuum deposited.

Work function (Φ) modifying SAMs have long been known to affect the charge injection properties at metal/organic semiconductor interfaces.^{22,23} The dipole moment of the SAM has an effect on the work function of the metal at the interface, while also affecting the morphology of the semiconducting layer deposited on it, which can have a strong impact on charge transport.²¹ Thiol derivatives with electron withdrawing substituents such as nitro-groups or fluoro-atoms (such as pentafluorothiophenol (PFTP), also known as pentafluorobenzenethiol (PFBT)) have commonly been used to promote injection into p-type semiconductors from Au.^{21,24,25} Conversely, SAMs with amino and methyl tail groups have been shown to have the effect of decreasing the work function (Φ) of metals such as gold. In particular, 4-methylbenzenethiol (MBT) and 4-(dimethylamino)benzenethiol (DABT) have been successfully used to enhance injection from Au contacts to the C_{60} active region of a TFT resulting in higher linear mobility and device frequency performance.^{26,27} In addition, hexamethyldisilazane (HMDS) was used to achieve efficient electron injection into a C_{60} diode, resulting in higher DC output and frequency response (> 700 MHz).²⁸ SAM treatment is clearly seen, therefore, to be a promising tool for interface engineering, supporting effective device optimisation. This is particularly relevant for the a-Lith process, as self-assembly is inherently compatible with our precise yet high-throughput patterning

approach. Furthermore, asymmetric electrodes permit the use of SAMs with different anchoring groups that selectively bind to each metal.

To investigate the potential of SAMs we employed MBT and DABT (see chemical structure insets to Fig. 3a) and studied their impact on both the electrodes' Φ , and subsequent operating characteristics of C_{60} Schottky nanogap diodes. Figure 3a shows the evolution of Φ for Au and Al electrodes, as measured with scanning Kelvin probe technique in air, upon treatment with MBT and DABT. The work functions for untreated Au and Al electrodes are also shown for comparison. In agreement with previously published results, Φ_{Au} reduces by > 1 eV upon SAM functionalization and, as expected, MBT (with its larger dipole moment) has the more pronounced effect. In an unexpected result, however, the thiol SAMs also appear to modify Φ_{Al} . Such thiol-based SAMs are not expected to chemically attach to the Al surface, nor are the methyl or methylamino groups expected to have a particular affinity for Al/ Al_2O_3 . We hypothesise that SAM molecules must remain physisorbed on the metal affecting its surface characteristics; thorough removal of unbound molecules might be difficult within the nitrogen filled glove box. Whatever the origin for this observation, the overall effect is a reduction of Φ that is expected to improve electron injection into the LUMO of C_{60} (-3.6 eV), thus enhancing overall device performance. The work function of ODPa-treated Al electrodes was also investigated. This SAM (used in the a-Lith patterning process) was found to induce the largest shift in work function; a value of $\Phi = 3.65$ eV was measured by scanning Kelvin probe. The insulating nature of the aliphatic chain in ODPa, however, hinders charge injection and hence current transport across the metal-semiconductor contact, and thereby precludes its application as an electrode work function modifier.

The impact of SAM treatment on diode performance is shown in Fig. 3b, with a schematic of the device architecture inset. As expected, electrode treatment with MBT has the greatest overall effect on performance resulting in a reduced turn-on voltage (≈ 0 V) and higher on-current ($0.24 \mu A$ at 2 V) than for devices with

untreated electrodes. Both effects are ascribed to the reduction in electron injection barrier (Fig. 3a). Electrode treatment with DABT produces an even higher on-current, reaching $\approx 4 \mu\text{A}$ at 2 V, but there is very little accompanying shift in turn-on voltage.

C_{60} diodes based on SAM-treated electrodes were also found to exhibit improved DC output voltage (V_{OUT}) (Fig. 3c) when an AC input signal (V_{IN}) with amplitude ± 3 V was applied across the half wave rectifier (HWR) circuit shown in the inset to Fig. 3c. Circuits based on the DABT-treated electrodes show a 0 dB output voltage ≈ 1.2 V, while those based on MBT yielded 0 dB DC output ≈ 1 V, in both cases significantly higher than HWR circuits based on diodes with untreated electrodes, which showed 0 dB DC output ≈ 0.7 V. Figure 3d shows the average performance measured for 15 diodes each with No SAM, with DABT- and with MBT-treated electrodes, probed within a HWR circuit, using an RF input signal of ± 3 V amplitude at 13.56 MHz. On the basis of these results we conclude that limiting the diode on-current appears to be more detrimental to V_{OUT} than the current onset potential. The latter relates largely to the built-in (V_{bi}) potential at the critical Al/ C_{60} junction. What is also clear is the ability to dramatically improve diode performance by simple treatment of the corresponding metal contact with an appropriate work function modifying SAM.

A further advantage of a-Lith is its straightforward use to monolithically integrate several nanogap diodes in a simple coplanar configuration. We demonstrate this by fabricating full-wave bridge rectifier (FWBR) circuits similar to that shown schematically in Fig. 3e. Figure 3f displays lower (left image) and higher (right image) magnification photographs of these FWBR circuits based on solution deposited ZnO with a variety of different size diodes employed. The four Al/Au nanogaps (highlighted by the superimposed rectangular dashed line boxes in the right image) form the four diodes (denoted D1-4). The nanogaps denoted I1 and I2 (right image) were electrically shorted in order to connect D1 with D2 and D3 with D4, respectively, and define the input nodes for the circuit (see Fig. 3e schematic). The dynamic response of a representative FWBR is shown in Fig. 3g. When V_{IN} is a ± 2 V, 100 Hz sinewave, the circuit generates a full-wave output with peak-to-peak voltage $V_{\text{max}} \approx 0.2$ V, corresponding to a DC level $V_{\text{DC}} = (2/\pi)V_{\text{max}} \approx 0.13$ V. The frequency is limited, primarily, by the specific circuit utilised and our measurement set-up that makes characterisation at high frequencies rather challenging. We are confident, however, that circuit optimisation should lead to FWBRs capable of operating at 13.56 MHz, if not higher.

Nanoscale organic light-emitting diodes

Nanoscale light sources have received increasing attention by the research community in the last years due to the variety of potential applications they offer in several fields. Micron and sub-micron active region polymer light-emitting diodes (PLEDs) have been suggested more than 20 years ago to serve as light sources in scanning near-field optical microscopes (SNOMs)²⁹ and the use of a scanning tunnelling microscope tip as electrode allowed demonstration of nanoscale electroluminescence at current densities expected to be compatible with electrically pumped lasing.³⁰ A more commercially interesting application of nanopatterned organic light-emitting diodes (OLEDs), however, may be as an enabler for next-generation ultra-high definition small size displays, especially via developments in manufacturing techniques that will allow simultaneous fabrication of high density miniaturised light sources over large-area substrates.³¹ One of the big challenges associated with this end-application is the nanopatterning of OLED arrays that are efficient, bright, and reliable. Nanostructured OLEDs are, additionally, becoming particularly attractive in the emerging field of bioelectronics.³² Such applications do not necessarily demand high-definition patterning nor is efficiency and long-term stability of critical importance. For

instance, nano-OLEDs have been considered as excitation sources for photoluminescence (PL)-based sensing of several analytes. They have also been proposed as oxygen (and more general biochemical) sensors due to the sensitivity of their emission properties to the presence of oxygen and other molecular species (see ref. ³³ and references therein). Their ultra-small size and ease of fabrication using low-cost solution-processing routes renders them compatible with microfluidic lab-on-a-chip architectures. At the same time the versatility of substrate-choice (glass, metal foil, or various plastics) and the diversity of device shapes and sizes on offer constitute a significant advantage relative to other light sources in terms of facile integration with the other components commonly present in sensor arrays.

Electron-beam (e-beam) lithography has until now been generally employed to fabricate nanoscale OLED structures. This is, however, a prototype-only technique, with the drawbacks of being a slow process, limited to patterning small areas, and, therefore, incompatible with the high-throughput large-area manufacturing desirable for industrial uptake. Adhesion lithography can be seen as a viable alternative with which to manufacture planar, arbitrarily large aspect ratio, nano-OLED devices with high yield and at low cost. It further offers a plethora of possibilities for device optimisation and colour tunability. To demonstrate its potential we fabricated *proof-of-concept* nanogap OLEDs based on four different solution-processed light-emitting conjugated polymers: poly(9,9-dioctylfluorene) (PFO),³⁴ poly(9,9-dioctylfluorene-co-bithiophene) (F8T2),³⁵ poly(9,9-dioctylfluorene-co-benzothiadiazole) (F8BT)³⁶ and poly(2-methoxy-5-(3', 7'-dimethyloctyloxy)-1,4-phenylenevinylene) (MDMO-PPV).³⁷ The chosen device architecture comprised square-shaped (1×1 mm in size) asymmetric Al/Au nanogap electrodes (Fig. 4a). The metal electrode thickness used was on the order of 40 nm, while the resulting inter-electrode gap was consistently < 20 nm (Fig. 1d). The total width of each electrode was 4 mm (around the perimeter of the square) and as a result the aspect ratio (width divided by inter-electrode distance) of the nanodiodes was on the order of 200,000 with a device active area (defined as the electrode height (thickness) multiplied by its width) of $160 \mu\text{m}^2$. Figure 4b shows an optical micrograph of a real nanogap OLED device where the central Au electrode (anode) is surrounded by a common Al electrode acting as cathode.

Figure 4c shows the chemical structures of the four light-emitting polymers employed and corresponding micrographs of the resulting nano-OLED emission while biased at 7–12 V. In all four cases the emission zone is constrained to the nanogap area and, depending on the polymer employed, colours spanning the full visible spectrum can be generated. Figure 4d shows a log–log plot of current–voltage (I – V) characteristics for a representative nanogap OLED based on poly(9,9-dioctylfluorene-alt-bithiophene) (F8T2) biased in the forward direction and between 0–10 V. Overall, the nanogap OLEDs exhibit clear diode behaviour with low reverse bias currents and different transport regimes in the forward bias direction. Light emission is observed at relatively high bias that typically exceeds 6 V (Fig. 4e); this compares to 2.4 V for conventional vertical diode structure F8T2 LEDs using indium tin oxide/poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) anode and Ba/Al cathode contacts.³⁵ Taking into consideration the geometric area of these planar nanogap OLEDs, the estimated current densities reach $\approx 600 \text{ kA/m}^2$. The emission photographs indicate, however, that there is heterogeneity in the emission intensity, suggesting current densities are locally higher than the average value. We note that the fact that the polymer doesn't just fill the nanogap but also extends over the entire surface of both coplanar electrodes does not seem to create a significant shunt pathway, since the light emission is clearly confined to the nanogap area. We further note that prolonged DC operation (tens of minutes) of these nanogap OLEDs at voltages > 8 V, leads to eventual device breakdown by nanogap burnout, and highlights

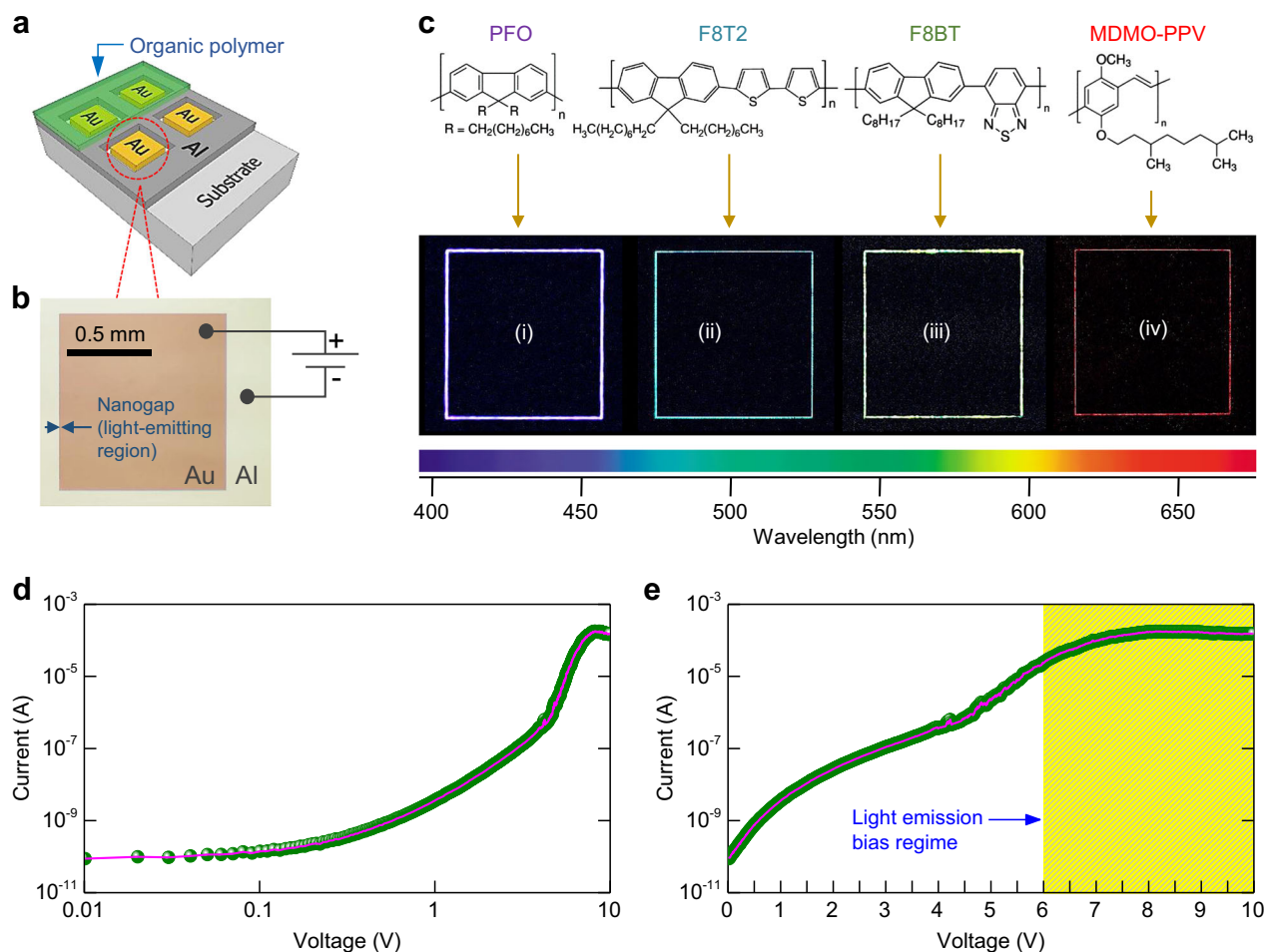


Fig. 4 Organic light-emitting nanogap diodes developed using a-Lith. **a** Schematic of coplanar nano-OLED devices. **b** Optical micrograph of square-shaped nano-OLED device consisting of asymmetric Al/Au electrodes. **c** Chemical structures of the various polymers employed and photographs of the corresponding nano-OLEDs in operation: (i) poly(9,9-di-*n*-octylfluorenyl-2,7-diyl) (PFO), (ii) poly(9,9-dioctylfluorene-*alt*-bithiophene) (F8T2), (iii) poly(9,9-dioctylfluorene-*alt*-benzothiadiazole) (F8BT), and (iv) poly[2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylenevinylene] (MDMOH-PPV). **d** Log–log plot of the current–voltage characteristics of a F8T2-based nano-OLED. **e** Semi-logarithmic plot of the I – V characteristics highlighting the bias region where detectable light emission occurs

the need for sustained device improvement. Finally, the radiative recombination processes in these nanogap OLEDs are the subject of further investigation.

Memristors

Memristive devices have seen a surge in interest since the early 2000s,^{38,39} as the demands for next-generation memory become ever more complex. Memristive devices are based on a resistive switching phenomenon, whereby a dielectric medium (generally with nanoscale dimensions) sandwiched between two electrodes exhibits a reversible shift in its bulk resistance on the application of an externally applied electric current or field. The process is non-volatile, and has the potential for applications in high-capacity, fast-switching, compact electronic memory.

The specific physical switching mechanism depends on the material system as well as the device structure. A popular model involves filamentous conduction or variations thereon. In this model, the low-resistance state (LRS) arises from the formation of conducting filament(s) through the insulating/semiconducting matrix during biasing. Rupture of the filament(s), through the application of an appropriate bias, then gives rise to the high-resistance state (HRS), with the process being highly reversible. A range of metal oxide based memristive devices have been reported in the literature.⁴⁰ Thermal redox and/or anodization

near the interface between the metal electrode and the oxide is widely considered to be the mechanism behind filament formation and rupture in unipolar switching,⁴¹ while for bipolar switching electrochemical migration of oxygen ions is regarded as the driving mechanism.⁴² Nevertheless, the exact nature of filament formation is still debated.⁴³ π -Conjugated polymers have been proposed as an alternative candidate for resistive switching, where filamentary models are explained through a fusing of carbon in the film or a migration of metal ions leading to shorting of electrodes.⁴⁴ Extensive reports have also been made on quasi-two-dimensional materials such as graphene, carbon nanotubes (CNTs)⁴⁵ and graphene oxide.⁴⁶ Switching in CNT films is attributed to either a small break junction and subsequent carbon filamentary conduction⁴⁵ or to the trapping and de-trapping of electrons causing conductive pathways.⁴⁷

Regardless of material, the favoured device structure tends to be a vertical metal/insulator or semiconductor/metal sandwich structure. Coplanar nanogap electrodes, however, present an alternative route to fabrication of functional devices. In this case, the advantage comes in the fact that the deposited active layer needs not be on the nanoscale since the active region of the device is defined, primarily, by the geometry of the nanogap. However, it is also worth noting that recent work has shown that empty nanogap electrodes can themselves be used as memristors

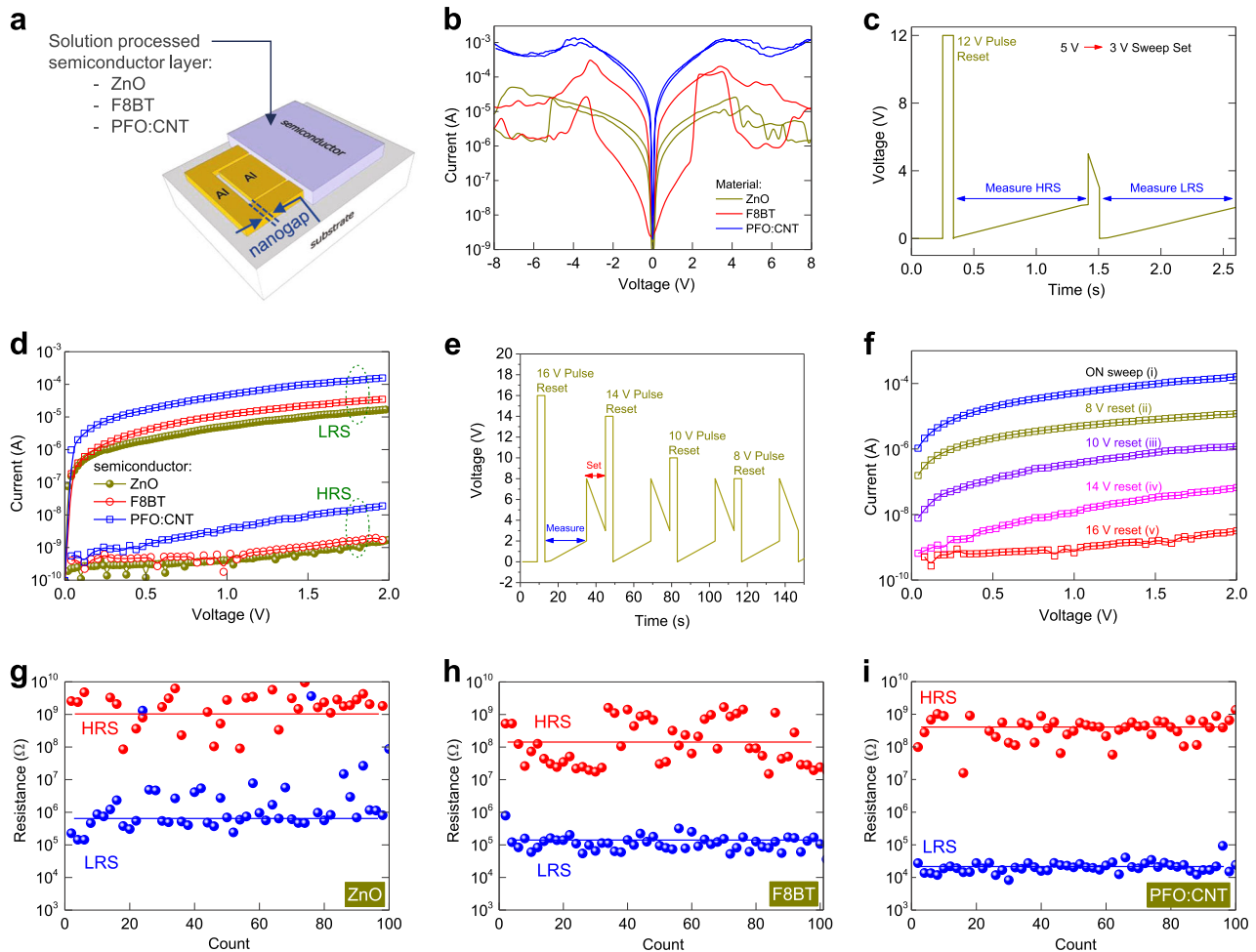


Fig. 5 Non-volatile memory nanogap devices developed using a-Lith. **a** Schematic of the memory device architecture fabricated via a-Lith. **b** I - V characteristics measured for nanogap devices based on ZnO, F8BT, and PFO:CNT. **c** Bias waveform used to programme the device resistance state and for subsequent endurance evaluation: The reset voltage (12 V pulse) applied for ≈ 100 ms puts the device into the HRS, after which the current is measured between 0 and 2 V. The set voltage (5–3 V sweep) puts the device into the LRS, after which current is again measured in the range between 0 and 2 V. **d** I - V curves depicting the low-resistance state (LRS) and high-resistance state (HRS) of the three device types tested using the waveform shown in **c** to switch between states and measure. **e** Bias waveform used to perform the multilevel programming of the device resistance state. **f** Multilevel switching characteristics measured from a representative PFO:CNT-based nanogap device. Endurance characteristics of **g** ZnO, **h** F8BT, **i** PFO:CNT nanogap devices obtained over 100 switching cycles. Resistance ratios in all cases are above 10^3 – 10^4

with the switching mechanism being attributed to both a change in the size of the nanogap (and tunnel current)^{48–50} and/or to filamentation occurring through the supporting substrate.^{51–53}

Recently, we employed a-Lith to fabricate empty symmetric Al/Al nanogap memristors on flexible substrates.⁶ The switching mechanism was attributed to migration of the electrode material into the gap and the formation of conductive nanoscale bridges that could be reset upon application of an opposite polarity bias. The initial forming process, however, is complex, requiring a bias-conditioning step. In an effort to gain better control over the programming (writing/erasing) cycles, we have now studied the influence of different semiconductor materials inserted into the nanogap. Three semiconductor types were investigated, namely the metal oxide semiconductor ZnO, the conjugated polymer F8BT and chirality selected PFO-wrapped semiconducting carbon nanotubes (PFO:CNT).⁵⁴

Figure 5a shows a schematic of the device architecture employed consisting of two symmetric Al/Al electrodes and a solution-processed semiconducting layer deposited on top. Figure 5b shows the low-voltage ($-8 < V < 8$ V) I - V scans for the three types of device. Interestingly, a negative differential resistance

(NDR) region is observed in all three cases irrespective of the semiconducting material employed. Although the characteristic NDR behaviour resembles that often seen in memristive devices,^{40,55} there is a marked difference in how the different materials affect the observed electrical behaviour. For instance, the PFO:CNT-based devices exhibit the highest maximum current, while those based on ZnO consistently show lower average currents despite ZnO's known higher charge carrier mobility.⁵⁶ The latter finding is most likely a consequence of the existence of resistive barriers at both Al electrode interfaces due to the native alumina that forms during ZnO deposition.⁵⁶

When the applied bias across the nanogap exceeds a critical voltage (usually > 8 V), the subsequently recorded I - V characteristics of even the more stable PFO:CNT and ZnO devices are found to exhibit hysteresis resembling that measured for the F8BT device in Fig. 5b. Importantly, the current flowing through the devices for low voltages is found to depend critically on the high-voltage biasing history of the sample. The conductive state of the device can, therefore, be “programmed” through the application of an appropriate voltage pulse. This observation is in agreement with our previous results suggesting that charge transport in these

devices is controlled by the formation of metallic/conductive paths (filaments) across the nanogap between the Al electrodes.⁶ We also note that, when compared to previously reported semiconductor-free (empty) nanogap devices, the programmability of the LRS and HRS states in all of the Al/semiconductor/Al devices appears to be significantly more reproducible across different devices and batches. Figure 5c shows an example voltage waveform used to programme the conductivity of the nanogap Al/semiconductor/Al devices between the LRS and HRS states, while Fig. 5d displays representative I - V curves measured for all three types of devices programmed in the LRS and HRS.

Finally, the large window between LRS and HRS (Fig. 5d) was exploited through the use of different programming waveforms (Fig. 5e) to demonstrate multilevel programming.⁴⁷ Figure 5f displays a representative set of low-voltage range I - V characteristics for a PFO:CNT device (the system that exhibits the largest window between LRS and HRS) programmed at five distinct conductivity states (numbered i to v). Although ZnO and F8BT devices exhibit similar multilevel resistance characteristics, the number of programmable states is smaller due to the reduced resistance window between HRS and LRS. In all cases, the conductivity of the device reduces as higher reset voltages are applied. Importantly, all three device types exhibit good endurance upon repeated programming as evident from Fig. 5g-i, albeit the PFO:CNT devices have the smallest variances.

We, therefore, conclude that symmetric coplanar nanogap devices incorporating different semiconductor materials can exhibit programmable resistivity with stable operation. While the physical switching mechanism may well be different between the different types of devices, the overall behaviour is qualitatively similar and resembles that seen in empty nanogap electrode-based devices.⁶

DISCUSSION

We have described the development and characterisation of different types of nanoscale electronic devices based on advantageous coplanar nanogap electrode structures enabled by a-Lith. The attractiveness of this method lies in: (a) its simplicity, as it requires only a few process steps, (b) low fabrication cost, since most of the steps are performed in ambient air, (c) high throughput, as a large number of distinct devices can be fabricated simultaneously on the same substrate using intrinsically scalable process steps (see ref. 3), (d) the possibility of fabricating symmetric or asymmetric nanogap electrodes based on different materials, (e) the use of rigid or flexible substrates, (f) patterning over small or large-area substrates (see ref. 3), (g) creating metal electrode structures of arbitrary size and shape, and (h) the ability to consistently deliver < 15 nm electrode nanogaps.

As a consequence of these attributes, a-Lith may stand out from several recent approaches to large-scale fabrication of nanogap-separated electrode arrays. For instance, atomic layer lithography and its variations have been presented as a high-throughput robust technique to produce sub-5 nm nanogap arrays at wafer scale, targeting mainly nanoplasmonic applications.⁵⁷⁻⁵⁹ The latter method requires conformal coating of the first metal with atomic layer deposited (ALD) alumina, Al_2O_3 , combined with adhesive tape, ion milling or extra lift-off steps for the planarization of the final surface. This adds complexity to the manufacturing process. An electrochemical approach was introduced by Lam et al., which utilises electroplating (via a so-called self-inhibited reagent depletion method) to narrow down macroscale gaps (originally fabricated with conventional low-cost techniques) to the nanoscale.⁶⁰ The authors demonstrated high-responsivity lead sulphide (PbS) quantum dot (QD)-based photodetectors based on these nanogaps. There were, however, some uniformity issues, while only symmetric electrode structures can be formed by this method.

Our research confirms that a-Lith fabrication of SAG transistors provides a route towards increasing transistor speed, consistent with the removal of parasitic capacitances arising from gate / S-D overlaps. It is expected that significant decrease in channel length combined with further contact resistance reduction will yield significant further device improvements. Our RF Schottky diodes, with a-Lith patterned asymmetric coplanar electrodes, show high cutoff frequencies and large output voltages. It is also possible to fabricate thousands of devices simultaneously and to integrate different circuit designs on large-area flexible substrates. This renders the a-Lith technique unique at present within the field of plastic RF electronics.

SAMs of varying chemical structure are widely used patterning tools in a multitude of ways.⁶¹ Here, we have shown their use as adhesion force modifiers, enabling fabrication of nanogap-separated coplanar electrodes through a-Lith. We have also shown their use as dielectric layers in a-Lith fabricated SAG TFTs and as work function tuning agents that enable efficient and selective (for asymmetric electrodes) metal/organic interface engineering. The latter behaviour was shown to allow optimisation of C_{60} -based RF diodes and should also allow adjustment of electrode injection/collection properties in nanoscale OLED and other optoelectronic devices. Our preliminary results thus provide ample evidence that careful materials and device engineering can provide solutions to many challenges.

From an operational standpoint, coplanar nanogap-based LEDs may well prove advantageous for certain applications relative to conventional vertical/sandwich structure LEDs. Higher current densities may be obtainable thanks to more efficient dissipation of Joule heating^{62,63} and short carrier transit times and reduced device RC time constants further help to deliver higher operating frequencies. Conversely, high turn-on voltages may lead to device degradation during operation and will need to be carefully addressed before any practical utilisation of the technology.

As regards a-Lith enabled memristive devices, the advantage of employing functional materials in the nanogap is that the forming process becomes a lot simpler, with resulting devices exhibiting inherent switching properties and robust operation. Most interestingly, the PFO:CNT devices show a resistance ratio between the HRS and LRS that exceeds 10^4 , combined with an enhanced stability under repetitive cycling, and multilevel switching. These attractive characteristics combined with the potential of scalable manufacturing³ and high device yield,⁵ make a-Lith a highly interesting approach for the development of a wide range of functional devices. These and the above-mentioned results confirm that there is plenty of scope for further investigations into the plethora of nanoelectronic devices enabled via a-Lith processing of a growing catalogue of functional materials.

METHODS

SAG TFT fabrication and characterisation

SAG TFT a-Lith electrodes were created using the standard a-Lith procedure, followed by immersion in 1-phosphonohexadecanoic acid (PHDA) solution in 2-propanol (1 mg/ml) for 14 h. Indium oxide was then formed from an indium (III) nitrate hydrate precursor solution [$0.5 \text{ M In}(\text{NO}_3)_3 \cdot x(\text{H}_2\text{O})$] in deionised water, spin-coated at 3000 rpm for 30 s and annealed at 200 °C for 30 min. Transient response measurements were carried out using a common drain amplifier configuration. A square wave input signal from a function generator (Agilent 33220 A) was applied to the gate electrode of the transistor, while a fixed voltage was applied to the drain electrode. A 100 Ohms resistor was connected in the source node and the output signal across the resistor was transformed with a current amplifier (Stanford Research system SR570) and measured with an oscilloscope (Agilent DSO6014A).

Schottky diode fabrication and characterisation

SAM treatment of the as-fabricated Al/Au nanogap electrodes was performed by immersing the structures in 1.6 mg/ml acetonitrile solutions of 4-methylbenzenethiol (MBT) and 4-(dimethylamino)benzenethiol (DABT) (Sigma Aldrich). The treatment was carried out overnight in a dry nitrogen glove box. Samples were then rinsed in acetonitrile and annealed at 80 °C to remove SAM and solvent residues. Scanning Kelvin probe and air photoemission measurements were carried out on the treated electrodes (SKP5050). Finally, C₆₀ was spin-coated on top, following previously reported procedures.⁵ Full-wave rectifiers were fabricated using the a-Lith process, followed by a second photolithography step to achieve the desired device architecture. A thin layer of ZnO was spin-coated from a precursor solution of zinc oxide hydrate in ammonium hydroxide (10 mg/ml) and annealed at 180 °C for 20 min. The spin and anneal process was carried out twice to ensure a thick enough layer.

Nanoscale OLEDs fabrication and characterisation

Poly(9,9-di-*n*-octylfluorenyl-2,7-diyl) (PFO), poly(9,9-dioctylfluorene-*alt*-bithiophene) (F8T2), poly(9,9-dioctylfluorene-*alt*-benzothiadiazole) (F8BT) and poly[2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylenevinylene] (MDMO-PPV) were purchased from Sigma Aldrich and used as received. PFO was dissolved in toluene and F8T2, F8BT, and MDMO-PPV in tetrahydrofuran (THF), all at a concentration of 5–10 mg/ml. Films were spin-coated at 2000 rpm and annealed at 70 °C for 10 min inside a N₂ filled glove box. Optical micrographs of the light-emitting nanogap devices were captured through a GXMXJL201A microscope with a GXCAM-3 High-Resolution Digital Microscope Camera attached to its eyepiece.

Memristor fabrication

Symmetric Al/Al nanogap electrodes were fabricated with a-Lith, with a second photolithography step used to create separated devices.⁶ ZnO and F8BT films were deposited as described above. The PFO:(5,7)CNT dispersion was prepared following the process described in refs. ^{54,64} and the respective chlorobenzene solution was spin-coated on the Al/Al nanogap electrodes followed by a mild annealing at 80 °C to remove the solvent.

Electrical characterisation of devices

Standard electrical characterisation measurements were carried out using a B2902A Agilent semiconductor parameter analyser under nitrogen atmosphere at room temperature. AC characterisation was carried out using an Agilent 33220A function generator and an Agilent DSO6014A oscilloscope.

SEM and TEM analysis of the nanogap electrodes

Plan-view high-resolution SEM images of Au-Al nanogaps were acquired with a Helios G4 UX microscope equipped with a field emission electron source (operated at 5 kV, yielding a current of 25 pA). Cross-section samples for TEM imaging were prepared in a Helios 400s FEI SEM using its nanomanipulator-equipped (Omniprobe, AutoProbe300) focused ion beam (FIB). Protective layers of carbon and platinum were deposited on top of the samples before milling. The bulk of the sample was milled using a gallium ion beam (30 kV, 9 nA) leaving a ca. 2 μm thickness slice. This slice was mounted on a copper grid and more slowly thinned (30 kV, 93 pA) and cleaned (5 kV, 28 pA) with the FIB prior to TEM measurements. TEM images were acquired with a Titan 80–300 FEI in scanning (STEM) mode at 300 kV operating voltage.

Data availability

Data is available on request from the authors.

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AUTHOR CONTRIBUTIONS

All authors contributed to this manuscript.

ADDITIONAL INFORMATION

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