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Guest Editor's Introduction

The recent past has seen a proliferation of embedded processor applications, resulting in numerous, and frequently conflicting constraints being placed on the processor architecture and the software running on it. This expansion and conflicting constraints have resulted in the necessity to reevaluate the current models for embedded processors and the associated software. The Workshop on Application Specific Processors (WASP) was formed in 2002 to provide a forum for discussing the underlying trends and implications on the hardware and software.

The *Workshop on Application Specific Processors (WASP)* aims to explore both research trends in academia and innovative applications and implementations in industry. It seeks papers in the various approaches possible for the processor architecture and for the associated software to enable the audience to compare and arrive at conclusions regarding the appropriate model. It encourages case studies so that the research principles can be observed in action and provide concrete data points.

As expected from such a vibrant field, in short order the workshop attracted a sizable community. 32 submissions from a wide variety of geographical locales were received. Slightly more than half of the submissions were received from Europe, befitting a truly international event. A quarter of the submissions were received from Asia, evenly split between Japan and the rest of Asia. The rest were received from North America. The program committee conducted a rigorous review process, with each paper receiving an average of five reviews. Nineteen of the papers were invited for presentation at *WASP*, organized in four sessions on *Network Processors*, *Low-Power Architectures*, *Compiler Support for Application Specific Processors*, and *Case Studies*. *WASP 2002* was held on November 19, 2002, in conjunction with *IEEE Micro*, a premier conference in the field of (general-purpose) micro-architecture. It attracted approximately 60 attendees making it the most popular workshop in the conference, thus enabling a significant degree of interaction with a wider architecture community. A second round of evaluation enabled a selection of five papers, deemed as worthy of publication in the *International Journal of Parallel Processing*.

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The five papers selected represent a wide range of issues in application specific processors and software.

The special issue starts off with a paper by Atasu, Pozzi, and Ienne, titled "Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints." The paper discusses an algorithm for compile-time extraction of application-specific instruction extensions. The algorithm operates on the data-flow graph of the program's basic blocks and identifies subsets for hardware specialization. The proposed approach is not limited to single-output connected subgraphs only, but effectively identifies disconnected components, a feature useful for generating custom SIMD instructions. The technique additionally supports the identification of multiple output subgraphs which results in the generation of multiple output VLIW instructions.

The second paper by Clark, Zhang, Tang, and Mahlke, titled "Automatic Design of Application Specific Instruction Set Extensions Through Dataflow Graph Exploration," outlines an approach for automatic identification of custom instructions for specialized embedded processor cores. Critical computation subgraphs are identified by the compiler and in a subsequent phase their desirability as a custom instruction is evaluated. Issues including performance gains, hardware cost, and instruction encoding are considered. The optimal such subgraphs are identified and replaced with specialized instructions.

In the third paper, "Power-Aware Compilation for Register File Energy Reduction," Ayala, Veidenbaum, and Lopez-Vallejo, propose an approach for optimally using the register file with the objective of minimizing its power consumption. Instead of having the entire register file active all the time, only the currently used registers are left available. The unused registers are put in a "drowsy" low-power mode which minimizes the static power consumption. The compiler is responsible for inserting instructions that select a pre-defined subset of registers and disables the rest. Register file power reductions of up to 60% are reported for a number of media applications.

The fourth paper by Surendra, Banerjee, and Nandy, titled "On the Effectiveness of Flow Aggregation in Improving Instruction Reuse in Network Processing Applications," presents an evaluation study of the effectiveness of flow aggregation for instruction reuse in network processors. They propose an instruction reuse scheme and architecture where different reuse buffers are used for the various network flows. Common control information in the packet headers belonging to the same flow enables higher instruction reuse utilization. Performance improvements of up to 24% have been observed compared to standard instruction reuse schemes.

The final paper by Kachris, Dollas, and Bourbakis, titled "A Reconfigurable Logic-Based Processor for the SCAN Image and Video Encryption Algorithm," discusses issues in implementing the SCAN algorithm on a reconfigurable platform. The structure of the algorithm is analyzed and efficient hardware architectures identified for the various modules. A high-performance FPGA implementation is achieved and detailed hardware cost analysis is presented.

We have provided a selection in this special issue of some of the best papers from WASP, addressing both hardware and software issues. We hope that this special issue proves not only informative but also manages to impart a sense of the vibrant discussions that took place during WASP. This interactive environment was made possible by the many WASP attendees, to whom we are grateful for their incisive discussions, but also by the Program and Organizing Committee members who through their diligent efforts helped select a high quality set of papers, of which this special issue provides a selected cross-section.

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