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IC Voltage to Current Transducers with Very Small Transconductance

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Abstract. This paper deals with the design of very small ac transconductance voltage to current transducers intended for the design of low frequency continuous-time filters, very large resistors and other applications. The first type of Operational Transconductance Amplifiers (OTA) is based on a triode biased transistor and a current division technique. The second one uses partial positive feedback which allows to reduce transistor dimensions but the sensitivity to transistor mismatches increases.

The proposed techniques can be used for the design of high-order low frequency IC filters, ladder or based on biquads, with moderated transistor dimensions while the dynamic range-cutoff frequency performance is comparable to previously reported structures. A 10 Hz third order lowpass ladder filter has been designed with these techniques, and it shows a dynamic range of 62 dB. Besides, a novel biasing technique for capacitive sources coupled preamplifiers is proposed. Experimental results for a prototype, fabricated in a 1.2 μm CMOS process, have shown very low distortion components (THD $<$ 1% for input signals up to 20 mV), noise level below 15 μV_{RMS} and dynamic range of 63 dB. The power consumption is only 10 μwatts and the supply voltages are $\pm$ 1.5 volts.

Key Words: integrated circuits, analog circuits, filters, amplifiers

I. Introduction

Low frequency circuits play a very important role in systems for biomedical, telemetry, real time speech recognition and other applications. The design of these circuits is not an easy task, especially for Integrated Circuits (IC) implementations; for instance IC filters with pole frequencies below 10 Hz require resistances larger than 1 GΩ because the limitations on the capacitance values. The implementation of these resistance values requires of special design techniques [1–2, 4–9].

The capacitive sources are very often used in several applications, such as electret microphones in hearing aid devices [1–3] where the capacitance is around 30 pF and its output signal lies in the range from 50 μV up to 20 mV [1–3,14]. A typical low-frequency capacitive coupled preamplifier is depicted in Fig. 1. The resistor is required to define the operating point of the preamplifier composed by two fully-differential OTAs. Since the low frequency corner of the hearing aid devices is around 100 Hz, the resistance coupled to the 30 pF capacitor has to be larger than 100 MΩ. The implementation of these resistances using poly or diffusion resistors is prohibited because the silicon area required.

In order to tackle this problem, several switched-capacitor topologies using charge dividers have been reported [4,5]. However, for many applications discrete-time processing is not allowed. Several approaches for the design of continuous-time integrators with very large time constant were also reported [1,2,6–8]; most of these techniques are based on OTA-C integrators. It is well known that the time constant of OTA-C filters is determined by the ratio of the load capacitor to the OTA's small signal transconductance. Typically the further reduction of the OTA's transconductance requires extremely large transistors.

In this paper, several techniques for the design of very small transconductance voltage to current transducers are proposed. The basic transducer employs a triode biased transistor and a current division technique. If further reduction of the small signal transconductance is needed, then cross coupled techniques can be employed. The disadvantage of this approach is that the sensitivity to transistor mismatches increases. Results for a single ended third order ladder filter, including $\pm$1% transistor mismatches, have shown random offset voltages of 40 mV and dynamic range of 62 dB. Experimental results for a high-performance 20 dB gain amplifier have shown a dynamic range of 63 dB and offset voltage below 20 mV.

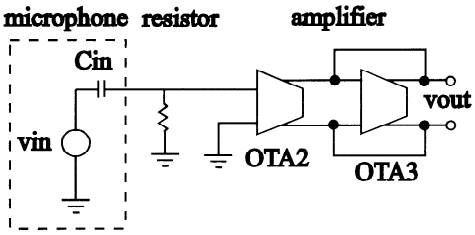

Fig. 1. Preamplifier architecture for capacitive sources.

The paper is organized as follows. The previously reported techniques for the design of OTAs with very small ac transconductance are briefly discussed in section II. The proposed techniques for the reduction of the small signal transconductance are presented in section III. In section IV these techniques are employed for the design of a high-performance preamplifier. The results are presented in section V and at the end of the paper the conclusions are addressed.

II. OTAs with Reduced Transconductance

In this section, several techniques for the design of very small frequency filters previously reported are discussed [6–8].

Current division by using current mirrors. In this technique, the current generated by the voltage to current transducer is further reduced by using current mirrors with large division factors. For moderated transistor dimensions, the transconductance of a differential pair can be as small as 10^{-7}–10^{-8} A/V. Hence, using current dividers, transconductors for filters in the range of few hertz can be obtained. The main cost of the current dividers is the large amount of silicon area required. In addition, the offset voltage increases if large current division factors are used.

Triode biased transistor. Another approach uses a transistor biased in linear region. Because the current of the MOS transistor biased in linear region is almost proportional to $V_{GS} - V_T$ then small drain-source conductance values can be obtained if very small $V_{GS} - V_T$ values are employed. However, this approach has two major disadvantages. Firstly, for very small $V_{GS} - V_T$ the value of the transistor conductance is not very well controlled. The conductance's sensitivity to both V_{GS} and V_T variations is inversely proportional to $V_{GS} - V_T$; hence the reduction of $V_{GS} - V_T$ increases the sensitivity. The second drawback is that the harmonic distortion components depend of $(V_{GS} - V_T)^{-1}$.

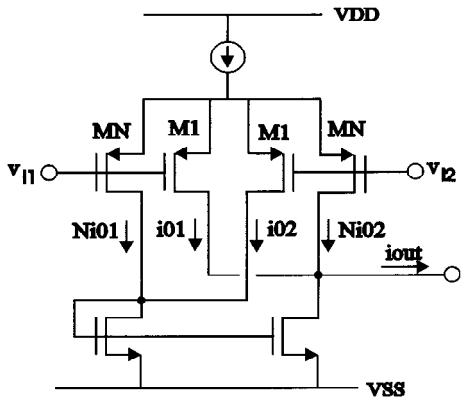

Fig. 2. Current cancellation technique using partial positive feedback [6].

Current Cancellation. In order to reduce the OTA transconductance a current cancellation technique can be used [7], see Fig. 2. Note that this topology employs partial positive feedback.

In this circuit, the OTA small signal transconductance is given by

$$G_m = \frac{N-1}{N+1} g_{m1} \tag{1}$$

where N is the ratio of the transconductance of MN to $M1$. According to this equation, G_m can be very small if N is nearly equal to 1; nevertheless the sensitivity to transistor mismatches increases further in this case. As a result of this N is usually limited to the range of 0.5 to 0.9.

III. Proposed Voltage to Current Transducers

The current generated by a transistor biased in linear region can be split by a current divider as shown in Fig. 3; note in this circuit the absence of positive feedback. If the conductance of MR is much smaller than the transconductance of MM, the small signal transconductance of the OTA becomes

$$G_m = \frac{2 g_{m1} g}{2g + (1+M) g_{m1}} \tag{2}$$

where g_{m1} is the small signal transconductance of transistor M1 and M is the ratio of the transconductance of

MM to M1, and g is the small signal conductance of MR. By using a simplified model g can be modelled by [10,11–13]

$$g \cong \mu C_{ox} \frac{W_R}{L_R}(V_{SGR} - V_{TR}) \tag{3}$$

where subscript R is used to denote parameters of MR. μ, C_{OX} and V_T are technological parameters; W_R and L_R are the width and length of the transistor's gate, respectively. If $2g \ll (M+1)g_{m1}$ equation 2 becomes

$$G_m = \frac{2g}{(1+M)} \tag{4}$$

According to this equation, the OTA transconductance can be further reduced by increasing the factor M. This approach allow us to use higher bias voltage for the triode biased transistor; therefore the OTA harmonic distortion components are reduced [10, 12, 13]. Unfortunately, the factor M can not be increased further because the dc current components of i_{01} and i_{02} decrease by the same factor. Hence the offset voltage due to leakage currents increases, mainly for nano power applications.

Because the low supply voltages used to reduce the offset voltage is a must. Neglecting the third order terms, it can be shown that the random offset voltage of the structure is given by [14]

$$V_{off} \cong \frac{I_B}{2g}\left(\frac{\Delta B_n}{B_n} + \frac{\Delta I_B}{I_B}\right) \tag{5}$$

Where Δ is a result of the mismatches in both current sources I_B and N-type transistors, and is typically of the order of 0.01, and B_n is given by $\mu_n C_{OX} W_n/L_n$. Note that the random offset voltage is not affected by factor M. According to equations 3 to 5, the factor M can be used to adjust the resistance value and the dimensions of transistors $M1$ and MM can be designed to optimize other parameters like reduction of both noise level and offset voltage.

Most of the noise drain current due to the transistors that implement the current sources I_B is absorbed by MM (assuming that $g_{mM} \gg g_{m1}$), therefore this noise component can be neglected. A similar effect reduces the noise current component of the triode biased transistor MR. The noise level is, mainly, the result of the noise contributions of $M1$, MM and N-type transistors. By using well known noise analysis techniques [11] it can be shown that the input referred noise spectral density of the topology is

$$v_{eqin}^2 \cong \frac{2}{G_m^2}\left[g_{mn}^2 v_{eqn}^2 + g_{m1}^2\left(v_{eq1}^2 + v_{eqM}^2\right)\right] \tag{6}$$

where $(v_{eqi})^2$ is the noise spectral density of transistor Mi and g_{mn} is the small signal transconductance of the N-type transistors. In low-frequency applications the flicker noise is a strong limitation for the OTA dynamic range. The flicker noise for an MOS transistor can be characterized by the following expression [11]

$$v_{eqf}^2 \cong \frac{K_f I_D}{C_{OX} L^2 f} \tag{7}$$

where K_f is the flicker noise constant. By using this equation, the input referred noise spectral density becomes

$$v_{eq\,inf}^2 \cong \frac{2}{f}\left[\frac{g_{mn}^2}{G_m^2}\frac{K_{fn} I_{Dn}}{C_{OX} L_n^2} + \frac{g_{m1}^2}{G_m^2}\frac{K_{fp} I_B}{C_{OX}(1+M)}\left(\frac{1}{L_1^2} + \frac{M}{(1+M)L_M^2}\right)\right] \tag{8}$$

According to this equation the flicker noise can be reduced by increasing the gate's length of the N-type transistors, $M1$ and MM. Also, it is desirable to reduce both g_{mn} and g_{m1} as much as possible.

If thermal noise is considered, then the input referred noise spectral density is approximately given by

$$v_{eq\,\mathrm{int}}^2 \cong \frac{16}{3}\frac{KT}{G_m}\left[\frac{g_{mn}}{G_m} + \frac{g_{m1}}{G_m}\right] \tag{9}$$

where K and T are the Boltzmann constant and the temperature in Kelvin degrees, respectively. From equations 8 and 9 it is clear that decreasing both g_{mn} and g_{m1} results in noises reduction.

If smaller ac transconductance are needed, then the cross-coupled technique can be incorporated to the topology of Fig. 3; the resulting structure is depicted in Fig. 4.

In this circuit the small signal transconductance is given by

$$G_m = \frac{2(N-1)}{M+N+1}\left(\mu C_{OX}\frac{W_R}{L_R}(V_{GSR} - V_{TR})\right) \tag{10}$$

If N is near to 1 very small OTA transconductance can be implemented. The noise contributions of $M1$ and MN are of the same order of magnitude, therefore the noise level of the OTA increases when compared with topology of Fig. 3.

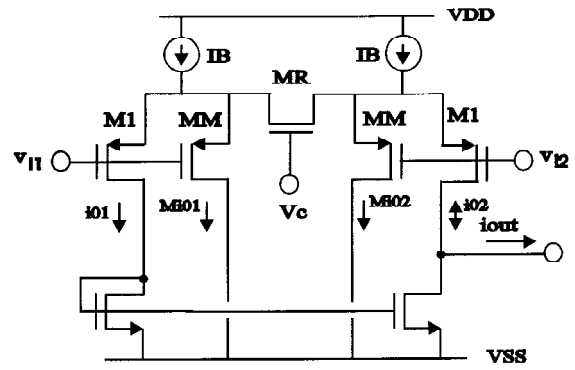

Fig. 3. OTA based on a triode biased transistor and current division.

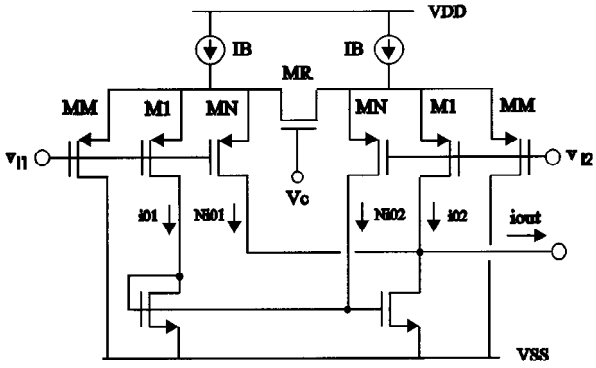

Fig. 4. OTA with very low transconductance.

IV. High-Performance Preamplifier

The previously discussed techniques can be used for several applications, an example is given in this section. A drawback of the preamplifier shown in figure 1 is that resistor is at the input of the preamplifier; therefore its offset voltage appears at the output amplified by the dc gain. An alternative to that preamplifier is depicted in Fig. 5. In this structure, OTA1 is connected in a differential mode feedback configuration to stabilize the circuit; the common-mode feedback circuit is not shown but it has to be included.

To reduce the harmonic distortion components, OTA2 and OTA3 must be linearized structures. For the implementation of OTA2 the topology proposed in [9] is used. This structure increases the linearity of the differential pair; it can be shown that for $v_{in} = 10$ mV and saturation voltages of 0.035 volts the even-order harmonic distortions are below -55 dB. OTA3 drives signals as large as 200 mV. Due to the reduced supply voltages, the bias voltages of the transistors can not be increased, hence this OTA is implemented with a more complex structure, see figure 6 [10,12]. The amplifier's overall gain is very well controlled because it depends on the ratio of transistor dimensions and the ratio of bias currents.

By using circuit analysis techniques, it can be found that the dc offset voltage at the output of the preamplifier is almost equal the offset voltage of OTA1.

If the parasitic capacitors are neglected, the circuit behaves as a first order high-pass filter with the inband gain given by g_{m2}/g_{m3}, and the low frequency pole at $\omega_p = (g_{m1}/C_{in})(g_{m2}/g_{m3})$. Note that the pole frequency is displaced to a higher frequency by the inband gain factor. To overcome this shortcoming g_{m1} must be reduced; this can be carried out with the topology shown in Fig. 7.

The circuit operates as follows. Connected in parallel to the input transistors of OTA3, as shown in Fig. 7, two transistors MOTA1 have been allocated. These transistors sample the amplifier output voltage and carry out the voltage to current conversion, and this current is fedback to the input of OTA2. If $g_{mOTA1} + g'_{m1}$ equals g_{m1}, then [14]

$$g_{mOTA1} = \frac{B}{2\left(1 + \frac{W_{M1'}L_{MOTA1}}{W_{MOTA1}L_{M1'}}\right)} \frac{g_{m1}}{1 + \frac{\beta_1}{4\beta_2}} \quad (11)$$

$$g_{mOTA3} = \frac{1}{2\left(\frac{W_{MOTA1}L_{M1'}}{W_{M1'}L_{MOTA1}}\right)} \frac{g_{m1}}{1 + \frac{\beta_1}{4\beta_2}} \quad (12)$$

where B is the scaling factor due to the current division. In order to reduce g_{mOTA1}, it is desirable to increase both $W_{M1'}/W_{MOTA1}$ and $L_{MOTA1}/L_{M1'}$. Note that the linearity of OTA1 is guarantied because its output current is a sample of the OTA3 current.

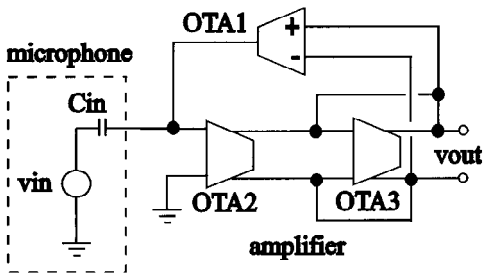

Fig. 5. Low-offset voltage amplifier.

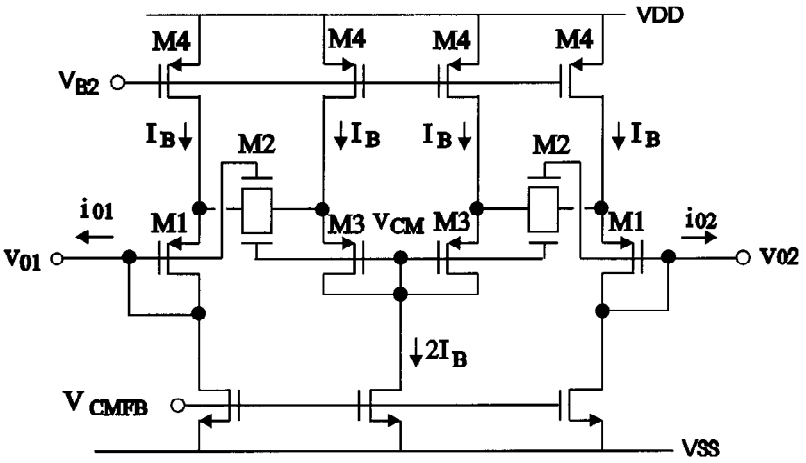

Fig. 6. OTA3 connected in a resistor configuration.

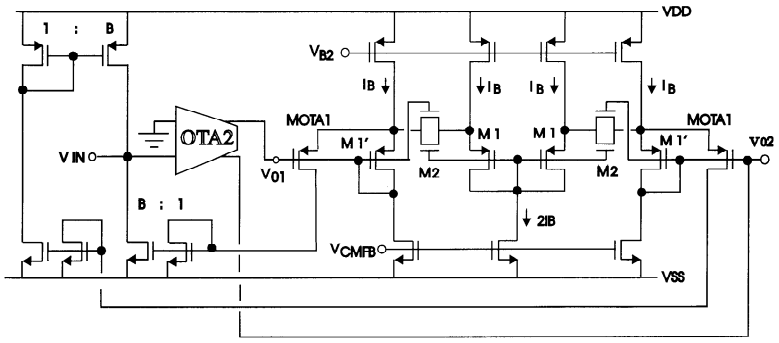

Fig. 7. Preamplifier with low DC-offset voltage.

V. Simulated and Experimental Results

The topology of figure 4 has been used for the design of a single-ended third order lowpass ladder filter with 10 Hz cutoff frequency. For this design, $N = 0.9$, $M = 200$ and 10 pF capacitors have been used. Dimensions and bias conditions for the transistors are given in table 1. To reduce the noise contributions of the N-transistors, $W = 10\ \mu$m and $L = 500\ \mu$m has been employed.

Using montecarlo analyses the filter has been extensively simulated. The magnitude response, with $\pm 1\%$ transistor mismatches, is depicted in Fig. 8. The passband ripple changes from 0.1 dB up to 0.5 dB.

The output referred offset voltage for the single ended filter is below to 120 mV, with systematic and random offset voltages of 80 mV and 40 mV, respectively. The systematic offset voltage can be further reduced by using fully-differential structures. The random offset voltage, obtained from simulations, is in good agreement with equation 5 ($R = 1\ G\Omega$, $I_1 = 2$ nA and $\Delta = 0.01$). For this design $V_{SGR} - V_T$ is 0.5 volts, which result in small harmonic distortion components; e.g., $HD2 < 2\%$ and $HD3 = 0.1\%$ for input signals up to 0.45 V_{RMS}.

Table 1. Dimension and bias conditions for the voltage to current transducer of Fig. 4.

transistor	$W/L\ (\mu m/\mu m)$	$I_D\ (\mu A)$
MR	20/200	0.0000
M1	10/530	0.0022
MN	10/430	0.0027
MM	50/12	0.6000

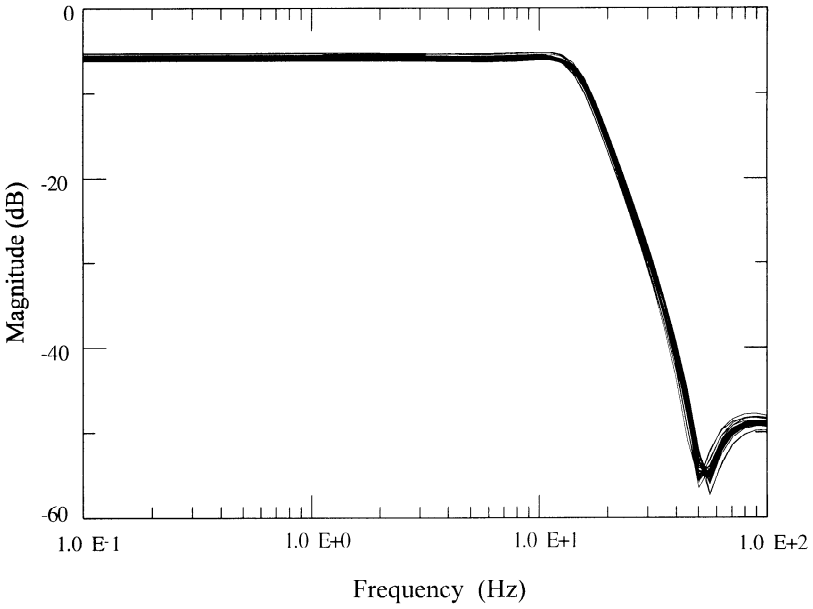

Fig. 8. Magnitude response for the third-order lowpass ladder filter.

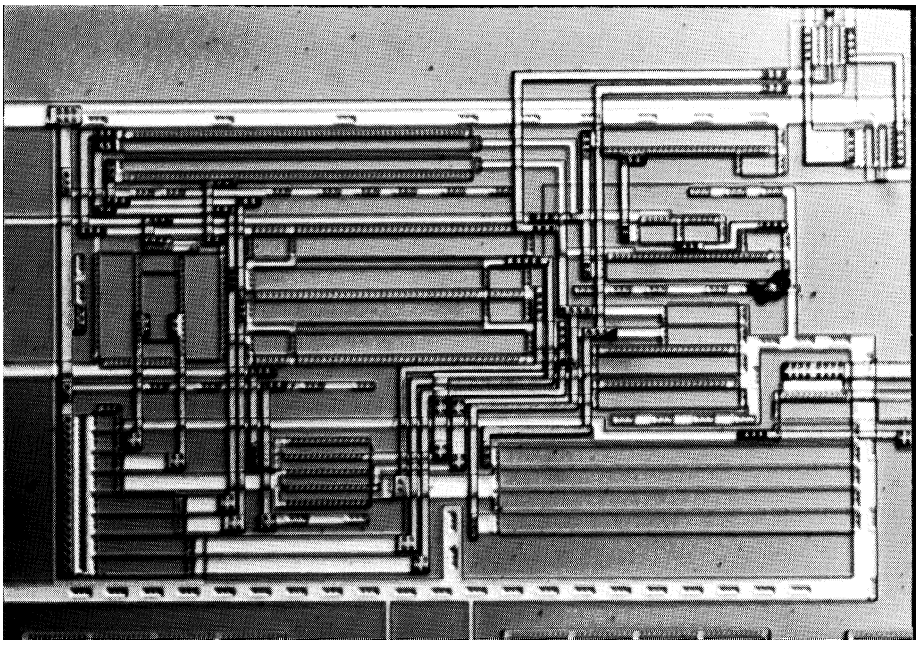

Fig. 9. Microphotograph of the preamplifier.

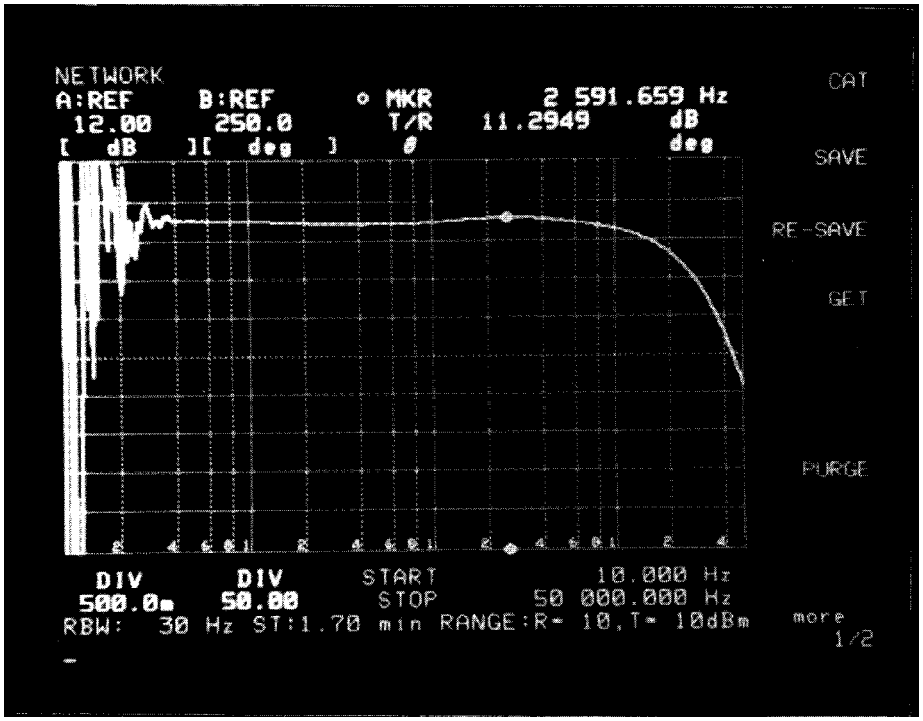

Fig. 10. Magnitude response for the amplifier.

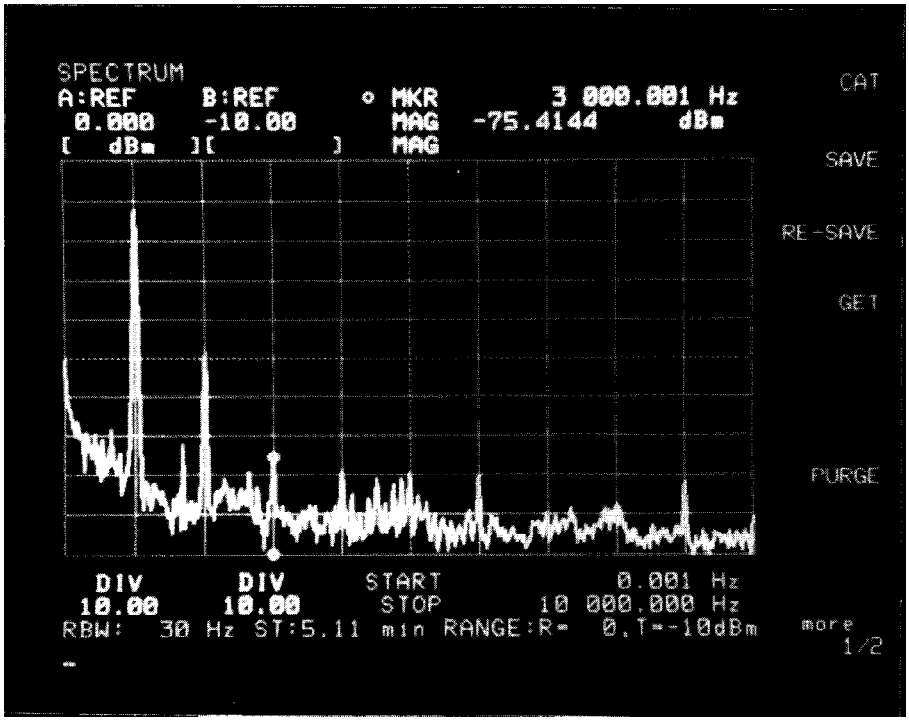

Fig. 11. Single ended output spectrum for the preamplifier.

The preamplifier of figure 7 has been fabricated in a 1.2 μm CMOS process. The chip microphotograph is shown in figure 9.

The measured single ended magnitude response for the preamplifier is shown in figure 10. In order to characterize the chip a -4 dB attenuator was employed. The inband gain is 19.75 dB and the -3 dB frequency is 40 kHz. The single ended output spectrum for $v_{in} = 20$ mV is shown in figure 11; the second order distortion is -40 dB while the third order harmonic distortion is below -60 dB.

The input referred noise (integrated from 100 Hz up to 10 kHz) is around 15 μV, leading to a dynamic range of 63 dB. The offset voltage at the output is below 25 mV. The supply voltages are $\pm$ 1.5 volts and the resulting power consumption is only 10 μwatts.

Conclusions

A pair of OTAs for the implementation of very-low frequency continuous-time filters have been proposed. It has been shown that a tradeoff between offset voltage and cutoff frequency is present in the structure. Nevertheless, it has been shown that the design can be optimized. Results for a third order lowpass ladder filter have shown a dynamic range of 62 dB while the power consumption is only 15 μwatts.

Besides, a CMOS preamplifier for capacitive sources has been introduced. The overall gain of the preamplifier is very well controlled because it depends on the ratio of transistor dimensions and the ratio of bias currents. The amplifier consumes 10 μwatts and the dynamic range is 63 dB. The supply voltages are only $\pm$ 1.5 volts and can be reduced down to $\pm$ 1 volts. All this has been achieved due to the use of a structure based on a current division principle.

Acknowledgments

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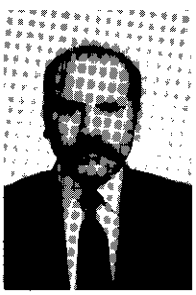

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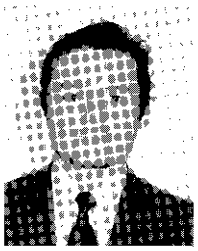

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