Journal of Power Electronics (2024) 24:946–954
https://doi.org/10.1007/s43236-024-00804-6

ORIGINAL ARTICLE

Analyzing and mitigating parasitic capacitances in planar transformers for high-frequency operation

Sujeong Lee[1] · Seokwon Kim[1] · Jong-Won Shin[2] · Wonhee Kim[3]

Received: 25 January 2024 / Revised: 14 March 2024 / Accepted: 15 March 2024 / Published online: 16 April 2024

Abstract
Planar magnetic components are compact and less susceptible to skin effect due to their thin copper layers. However, the increase in parasitic capacitance has been a challenge in high-frequency operation of planar transformers (PTs). Parasitic capacitances resonate with inductance and may damage switch devices. Thicker printed circuit board (PCB) and reconfigured windings are suggested in this paper to mitigate the parasitic capacitances. A detailed analysis of the parasitic capacitances is performed with a prototype PT. The resonant frequency increased from 1.27 to 1.63 MHz with a 0.4 mm thicker PCB. The reconfigured PT was 1.38 MHz, 0.3 MHz higher than the original PT.

Keywords Multi-layer PCB · Planar transformer · High frequency · Parasitic capacitance · Resonance · Impedance analysis

1 Introduction

Converters for urban air mobility or electric vehicle are required to be compact and light. Variable methods to attain high-power density and high-efficiency converters have been studied [1–5]. Miniaturization of magnetic components, such as a transformer and an inductor, is essential for high-density converters as they are typically bulky and heavy.

High-frequency (HF) operation decreases the size of magnetic components, leading to high-power density. Contemporary semiconductors with wide-bandgap (WBG) material enable HF operation to elevate switching frequency. However, conventional wire-wound magnetic components are limited in operating at high frequencies. Typical ferrite cores used in mass production are currently available up to 2 MHz [6]. Skin and proximity effects in copper wires increase winding loss at frequencies above 100 kHz [7]. Thin copper layers on a printed circuit board (PCB) in planar magnetic components replace conventional round copper wires. The utilization of flat conductors in planar magnetic components has been proven to reduce the skin and proximity losses in the windings, even though the converter operates at high frequency [8–11].

The benefits of planar magnetic components have prompted research on their design methodologies. Planar magnetic components inherently offer low profiles compared to wire-wound counterparts, allowing a reduction in the size of power converters. Planar magnetic components have high-power density, excellent mass productivity, and good thermal characteristics [12, 13]. Planar magnetic components also permit flexible winding configurations. Various PCB winding technologies have been covered in Refs. [8, 10], and [14–18] to optimize the magnetic components. An interleaved winding structure is applied to avoid voltage spikes at semiconductors by minimizing the leakage inductance [22]. The interleaved structure is often employed in planar transformers (PTs) to decrease winding losses and enhance efficiency [19]. However, it concurrently elevates inter-winding capacitance, posing challenges in HF operation. There is a trade-off between the winding loss and the inter-winding capacitance.

Despite the aforementioned advantages, one of the drawbacks of PTs is the parasitic capacitances. Overlapped copper traces in PCB cause the parasitic capacitances of a PT. The resonance with the parasitic capacitances and

✉ Jong-Won Shin
jongwonshin@snu.ac.kr

✉ Wonhee Kim
whkim79@cau.ac.kr

[1] Department of Smart Cities, Chung-Ang University, Seoul, Republic of Korea

[2] Department of Electrical and Computer Engineering, Seoul National University, Seoul, Republic of Korea

[3] School of Energy System Engineering, Chung-Ang University, Seoul, Republic of Korea

inductances at high frequencies leads to HF oscillations, inducing electromagnetic interference (EMI) issues. Bulky EMI filters hinder the high-power density converter. A low-impedance path along the parasitic capacitances results in voltage/current spikes at switch devices. Therefore, reducing the parasitic capacitances is critical to prevent converter performance from degrading.

Modeling the parasitic capacitances of the transformer was described in Refs. [20, 21]. Studies for multi-layer planar transformer (MLPT) were examined in Refs. [22, 23] based on Refs. [20, 21]. Simple methods to mitigate the parasitic capacitances are suggested to mitigate the parasitic capacitances in this paper. The parasitic capacitances of an MLPT are modeled and calculated. This paper also compares the values using finite-element analysis (FEA). Impedance analysis is implemented to establish the resonant frequency of the MLPT for the purpose of operating at a frequency below the resonant frequency. In Sect. 2, the process of constructing the equivalent circuit of MLPT is explained. Section 3 discusses two simple approaches of increasing the resonant frequency of the MLPT and verifies their effect by impedance analysis. Experimental results are shown in Sect. 4. The measured impedances of prototype PTs are compared with calculated and simulated impedances. Two improved PTs are compared to the measurement and calculation values, respectively. The conclusion is provided in Sect. 5.

2 Estimation of the parasitic capacitances

Parasitic capacitances arise from the overlap between the two consecutive copper layers of the PT, as demonstrated in Fig. 1. The HF components of the current or voltage that causes EMI issues flow along the low-impedance path provided by the parasitic capacitances. Parasitic capacitances also resonate with the inductance of the PT, causing oscillations in the current and voltage. Accurate estimation of the parasitic capacitances in the PT is essential to ensure optimal performance at high frequencies.

This paper is based on Refs. [20–23]: Fundamental capacitance modeling for transformer is explained in Refs. [20, 21]; the analyses of the PT are presented in Refs. [21, 22]; modeling of MLPT is described in Refs. [22, 23]. Section 2.1 reviews parallel-plate capacitance model to precisely calculate the parasitic capacitance of the PT depending on the winding methods. Section 2.2 discusses the estimation of the capacitance for two adjacent layers from different windings. The equivalent circuit of the MLPT is derived in Sect. 2.3. Capacitances computed by modeling the MLPT and simulating by the FEA are also included in this section.

2.1 Capacitance model of the same winding in two adjacent copper layer

Various static capacitance models, including the parallel-plate and cylindrical models [23], have been studied. The parallel-plate model is adopted to represent the parasitic capacitances of the PT as illustrated in Fig. 2. The parallel-plate capacitance, denoted as C_0, is computed using (1):

$$C_0 = \varepsilon_0 \varepsilon_r \frac{w \cdot l}{d} = \varepsilon_0 \varepsilon_r \frac{A}{d}. \tag{1}$$

The parameters d, w, l, and A in Fig. 2 and (1) refer to the distance between two adjacent copper layers, the width, the length, and the area of the copper layer. Vacuum permittivity is defined by ε_0, and relative permittivity is ε_r. The voltage distribution between the layers establishes the equivalent inter-layer capacitance, labeled as C_{il}, along with the electrical energy stored in capacitance C_0. Charge distribution varies with voltage distribution, causing changes in C_{il} with the applied winding methods. A straight-connected winding method between two layers, as drawn in Fig. 3, is only examined in this paper. When C_{il} between the layers of windings in a PT, it is assumed that the layers are equipotential and the skin effect is negligible. The energy stored between two layers, $W_{E,layer}$, is found in (2):

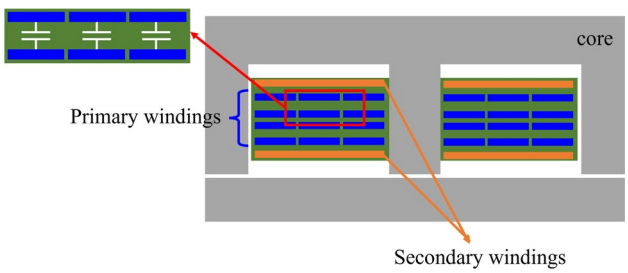


Fig. 1 Cross-section of multi-layer PT

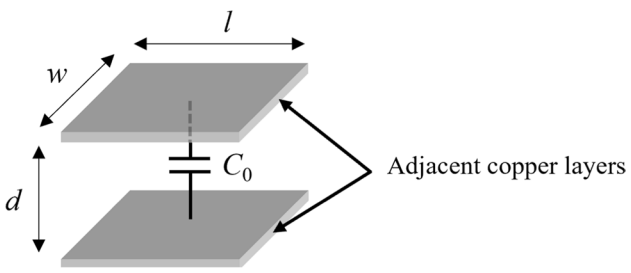


Fig. 2 Parallel-plate capacitance model

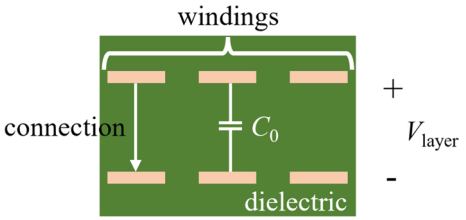


Fig. 3 A straight-connected winding method

$$W_{E,layer} = \frac{2}{3}C_0\left(\frac{V_{winding}}{\text{Number of layers}}\right) = \frac{1}{2}C_{il}V_{winding}^2. \quad (2)$$

The voltage of one winding is represented by $V_{winding}$. The expression for the relationship between C_0 and C_{il} is finally provided by (3):

$$C_{il} = \frac{C_0}{3}. \quad (3)$$

2.2 Capacitance model of the different winding in two adjacent copper layer

The equivalent capacitance constructing the different windings is represented by a two-layer transformer capacitance model. Intra-winding capacitance (capacitance in single winding) and inter-winding capacitance (capacitance between two different windings) are determined with the six-capacitance equivalent circuit as depicted in Fig. 4a. The intra-winding capacitances C_1 and C_6 and the inter-winding capacitances C_2, C_3, C_4, and C_5 are decided by considering the electrical energy W_E in (4). The voltage across C_k is U_k ($k=1, 2, 3, 4, 5$, or 6) as expressed by (5). A six-capacitance network in Fig. 4b is then constructed using the values calculated by (4) and (5). The voltages aV_1 and bV_1 are measured at nodes A and B to the end of the primary-side windings, respectively. The voltages on the secondary side, cV_2 and dV_2, are also found in the same way as the primary side. The voltage values are defined as the ratios of the input and output voltages, V_1 and V_2. For example, a, b, c, and d have the values of 3/4, 1/2, 1, and 1/2, respectively, in the network shown in Fig. 4b:

$$W_E = \frac{1}{2}\sum_{k=1}^{6} C_k U_k^2, \quad (4)$$

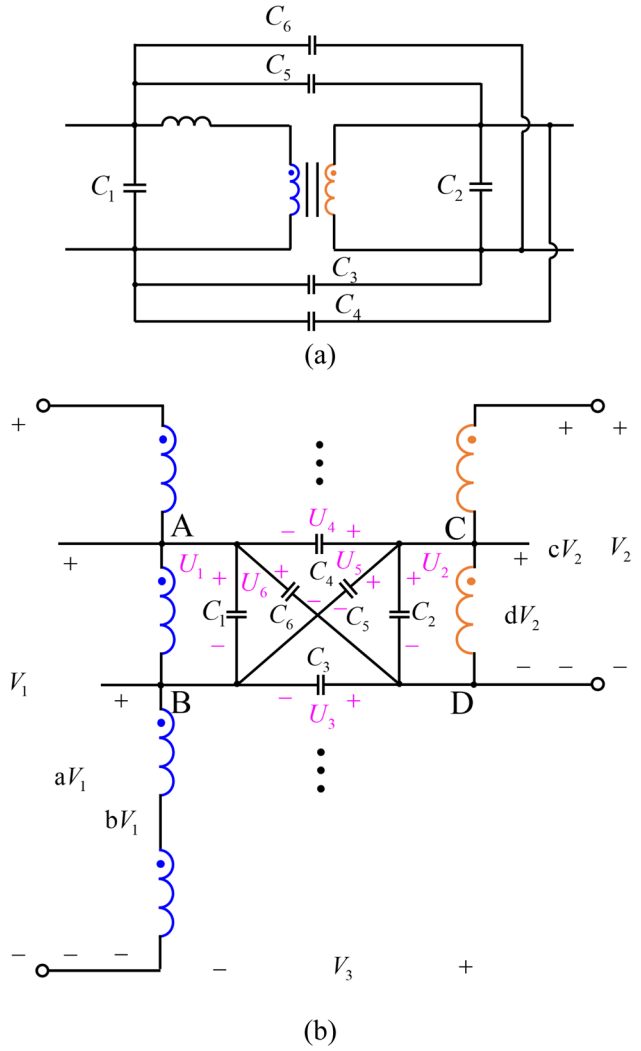


Fig. 4 A Equivalent six-capacitance circuit; **b** six-capacitance network of MLPT

$$\begin{aligned} U_1 &= (a-b)V_1 \\ U_2 &= (c-d)V_2 \\ U_3 &= -bV_1 + dV_2 + V_3 \\ U_4 &= -aV_1 + cV_2 + V_3 \\ U_5 &= -bV_1 + cV_2 + V_3 \\ U_6 &= -aV_1 + dV_2 + V_3. \end{aligned} \quad (5)$$

By employing (4) and (5) to derive (6), C_1 through C_6 are acquired. The comprehensive calculation procedure is elaborated in Refs. [20, 23]:

$$
\begin{aligned}
C_1 &= -\frac{C_0}{6}(2a^2 + 2b^2 + 2ab - 3a - 3b)\\
C_2 &= -\frac{C_0}{6}(2c^2 + 2d^2 + 2cd - 3c - 3d)\\
C_3 &= \frac{C_0}{6}(6 - 3a - 3b - 3c - 3d + 2ac + 2bd + ad + bc)\\
C_4 &= \frac{C_0}{6}(2ac + 2bd + ad + bc)\\
C_5 &= \frac{C_0}{6}(3c + 3d - 2ac - 2bd - ad - bc)\\
C_6 &= \frac{C_0}{6}(3a + 3b - 2ac - 2bd - ad - bc).
\end{aligned}
\tag{6}
$$

2.3 Estimation of the parasitic capacitance model of multi-layer planar transformer

The parallel-plate capacitance in the multi-layer, $C_{0,ij}$ in (7), is important in calculating the equivalent capacitances of the n-layer MLPT [23]:

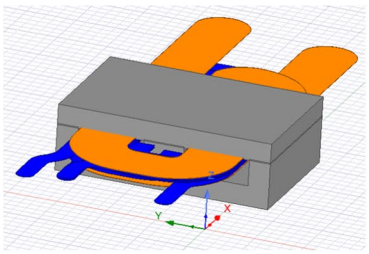
$$
C_{0,ij} = \varepsilon_0 \varepsilon_{r\_ij,eff} \frac{A_{ij,eff}}{d_{ij}}. \tag{7}
$$

The variable i in (7) represents the layer number, i.e., $i = 1, 2, 3, \ldots, n-1$, and j is defined as $j = i+1$. The distance between the two successive layers is expressed as d_{ij}, while the effective area between these layers is denoted as $A_{ij,eff}$. The effective permittivity between the ith and jth layers, $\varepsilon_{r\_ij,eff}$, is calculated using (8):

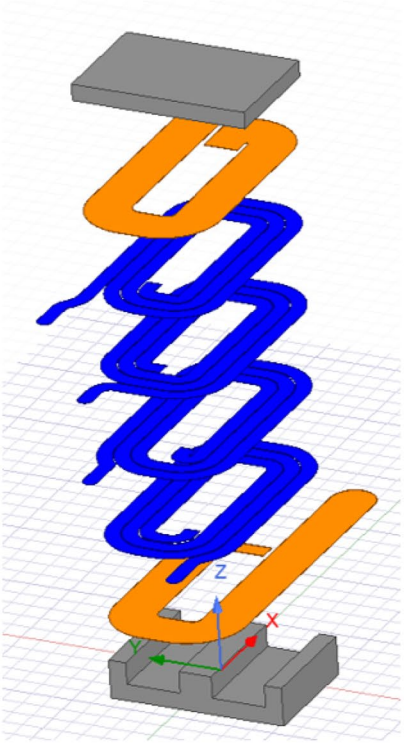
$$
\varepsilon_{r\_ij,eff} = \frac{\varepsilon_{r,1} \cdot z_1 + \varepsilon_{r,2} \cdot z_2 + \cdots + \varepsilon_{r,m} \cdot z_m}{z_1 + z_2 + \cdots + z_m}. \tag{8}
$$

In the context of a multi-layer PCB, the dielectric layers between two contiguous copper layers exhibit a permittivity designated as $\varepsilon_{r,m}$ and their thickness as z_m:

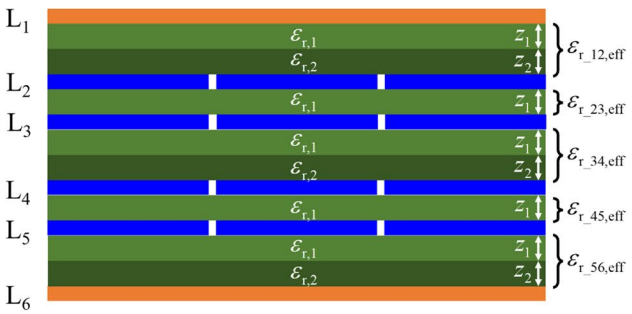
This paper investigates a six 2-oz layers PT in Fig. 5a with a 12:2 turns ratio, using Maxwell 3D on Ansys Electronics Desktop 2021 R2.2. The orange windings at the top and bottom layers are the secondary-side windings, while the blue windings in the middle layers indicate the primary-side ones. An exploded view in Fig. 5b facilitates a detailed examination of the winding configuration. The equivalent inter-layer capacitance $C_{il,ij}$ at the same winding was obtained through Sect. 2.1. Figure 5c represents a cross-sectional view of the MLPT with the values determined by (8). Parameters in Fig. 5c are identified using the PCB stack-up information in Table 1. The equivalent $C_{il,pri}$ is obtained according to (9). In (9), $C_{il,23}$, $C_{il,34}$, and $C_{il,45}$ are the inter-layer capacitances on the primary side:



(a)



(b)



(c)

Fig. 5 A 3D view of the designed MLPT; **b** an exploded view of **a**; **c** a detailed winding configuration of **a**

$$
C_{il,pri} = \frac{1}{\frac{1}{C_{il,23}} + \frac{1}{C_{il,34}} + \frac{1}{C_{il,45}}}. \tag{9}
$$

Table 1 PCB stack-up information

Layer	Material	Thickness [μm]	Relative permittivity
L_1	Cu	70	
	Pre-Preg (7628)	200	4.45
	Pre-Preg (1080)	60	4.23
L_2	Cu	70	
	Core	300	4.45
L_3	Cu	70	
	Pre-Pre (2116)	100	4.36
	Pre-Pre (2116)	100	4.36
L_4	Cu	70	
	Core	300	4.45
L_5	Cu	70	
	Pre-Preg (1080)	60	4.23
	Pre-Preg (7628)	200	4.45
L_6	Cu	70	

The inter-layer capacitance on the secondary side is neglected because the distance between the top and bottom layers is large enough.

The equivalent circuit for the PT in Fig. 5 is demonstrated in Fig. 6. Each layer is denoted as L_i, where i is 1, 2, 3, 4, 5, or 6. The parasitic capacitances between L_2 and L_5 are combined into a single capacitance $C_{il,pri}$. Inter-layer capacitance $C_{il,pri}$ is connected to C_1 in parallel. Layers L_1 and L_6 connect the six-capacitance network to L_2 and L_5. Layers L_3 and L_4 are excluded from the network as they do not construct different windings. Two six-capacitance networks are connected in parallel as described in Ref. [23]. The absolute capacitances of C_1 to C_6 are calculated as (10) using Figs. 4b and 6:

$$
\begin{aligned}
C_1 &= \frac{5}{48}C_{0,12} + \frac{5}{48}C_{0,56} \\
C_2 &= \frac{1}{6}C_{0,12} + \frac{1}{6}C_{0,56} \\
C_3 &= \frac{1}{12}C_{0,12} + \frac{5}{24}C_{0,56} \\
C_4 &= \frac{5}{24}C_{0,12} + \frac{1}{12}C_{0,56} \\
C_5 &= \frac{1}{24}C_{0,12} + \frac{2}{3}C_{0,56} \\
C_6 &= \frac{2}{3}C_{0,12} + \frac{1}{24}C_{0,56}.
\end{aligned}
\tag{10}
$$

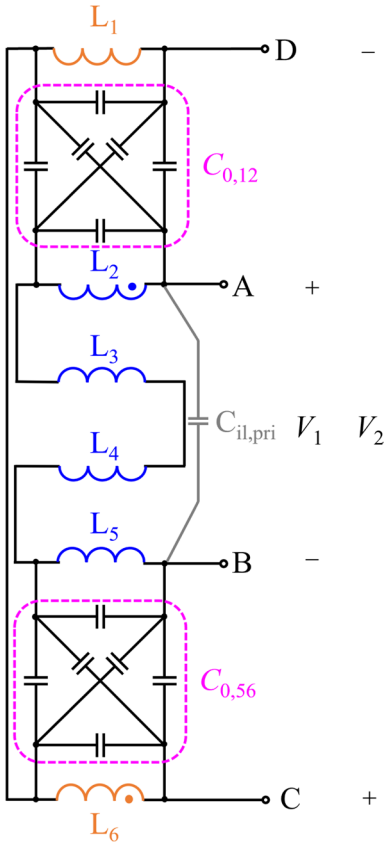


Fig. 6 Equivalent circuit of Fig. 5

Assuming that the area between conductors on each layer is negligible, $A_{ij,eff}$ is equal for every layer. The calculated C_1 to C_6, employing $C_{0,12} = C_{0,56} = 178.14$ pF, are in the second column of Table 2. Simulated parallel-plate capacitances are provided in the third column using $C_{0,12} = 214.9$ pF and $C_{0,56} = 189.66$ pF from Ansys Maxwell 3D. Slight deviations in $A_{ij,eff}$ for each layer in Fig. 5b appear as discrepancies between the calculated and simulated capacitances. Section 4 compares the impedances of the two equivalent circuits derived from Table 2.

Table 2 Calculated and Simulated Parasitic Capacitances

Parameters	Calculated [pF]	Simulated [pF]
$C_{il,pri}$	19.42	23.56
C_1	37.11	41.99
C_2	59.38	67.29
C_3	51.96	57.42
C_4	51.96	60.41
C_5	126.18	135.36
C_6	126.18	150.63

3 Decreasing the parasitic capacitances

Proper operation of the converter requires maintaining an adequate separation between the resonant frequency and the switching frequency. Two methods are proposed to achieve the difference. Section 3.1 discusses how thicker PCB is utilized to reduce the parasitic capacitances. The resonant frequency is increased by minimizing the overlapped area between PCB traces. Winding reconfiguration to achieve a higher resonant frequency is provided in Sect. 3.2.

3.1 Increasing the distance between the layers

A simple way to increase the resonant frequency is to reduce the parallel-plate capacitance in (1) and (3) by increasing the thickness of the dielectric layers on the PCB. Winding reconfiguration or transformer redesign is unnecessary. For example, the distance z_3 between L_1 and L_2 of the PCB described in Fig. 7 is larger than z_1+z_2 between L_1 and L_2 in Fig. 5c. Section 4 discusses the comparison result with the original PT to verify the resonant frequency shift to a higher frequency.

3.2 Improvement of the winding configuration

Parasitic capacitances amplify when copper traces in PCB are overlapped. Minimizing the overlapped area suppresses the parasitic capacitances. However, the limited width of the window area of the planar core necessitates the use of eight 2-oz PCB for the improved winding configuration as depicted in Fig. 8. The magnitude of the equivalent six-capacitance of the PT in Fig. 8 is derived as (11) following Sect. 2.3. Each capacitance is obtained by expanding Fig. 4b to 8 layers and applying the values to (6). Capacitances in (11) are used to analyze the total impedance to prove that the reconfiguration of the windings decreases the capacitances:

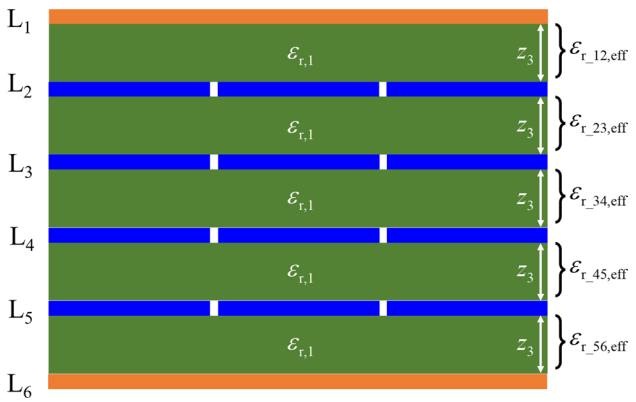


Fig. 7 A cross-sectional view of the thicker PCB

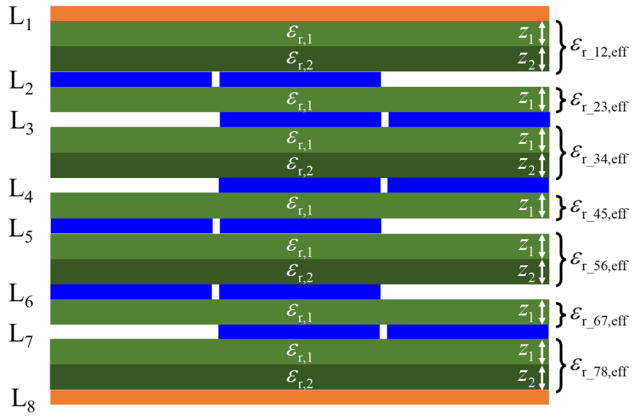


Fig. 8 A detailed reconfiguration of the windings

$$
\begin{aligned}
C_1 &= \frac{2}{27}C_{0,12} + \frac{2}{27}C_{0,78}\\
C_2 &= \frac{1}{6}C_{0,12} + \frac{1}{6}C_{0,78}\\
C_3 &= \frac{1}{18}C_{0,12} + \frac{2}{9}C_{0,78}\\
C_4 &= \frac{2}{9}C_{0,12} + \frac{1}{18}C_{0,78}\\
C_5 &= \frac{1}{36}C_{0,12} + \frac{25}{36}C_{0,78}\\
C_6 &= \frac{25}{36}C_{0,12} + \frac{1}{36}C_{0,78}.
\end{aligned}
\tag{11}
$$

4 Experimental results

The parasitic capacitances estimated in Sect. 2 and inductances are resonate. Impedance peaks near the resonant frequency generate undesirable oscillation that damages the switch devices or causes EMI issues. The resonance was validated with a prototype hardwareshown in Fig. 9 which

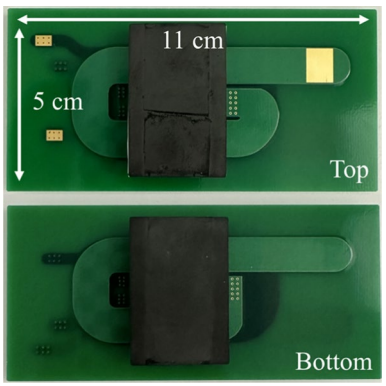


Fig. 9 Prototype hardware of the MLPT in Fig. 5

realized the transformer shown in Fig. 5. The planar cores utilized in the analyses are E43/10/28 and PLT43/28/4.1, manufactured by 3F4 material from Ferroxcube.

The impedance curve was obtained by evaluating the primary side with the secondary side open. The curve is comparable to a typical LC resonant circuit. The magnetizing inductance dominates at low frequency, while the parasitic capacitances dominate at high frequency. The effect of the leakage inductance on the resonance is negligible. Impedance curves with calculated and simulated values in Table 2 are plotted using LTspice XVII. An LCR meter, IM3570 from HIOKI, was utilized for measuring the impedance of the prototype transformer.

4.1 Impedance analysis

Figure 10 displays the calculated, simulated, and measured impedance curves for the PT in Fig. 5. The green graph was drawn with the calculated capacitances in Table 2. Simulated values were used to plot blue lines, and the measured capacitances were in red. The measured resonant frequency was approximately 1.27 MHz, which is close to the calculated and simulated values of 1.11 MHz and 1.01 MHz, respectively. Inductances resonate with the parasitic capacitances at high frequencies, which causes impedance peaking.

4.2 Planar transformer with thicker PCB

A modified PCB stack-up was proposed to prove that larger d_{ij} results in higher resonant frequency as mentioned in Sect. 3.1. The specification of the suggested PCB is tabulated in Table 3. It is about 0.4 mm thicker than the original PCB in Table 1. Figure 11 illustrates two measured curves for the PTs manufactured using the original and thicker PCBs. The red graph from the original PCB has a resonant frequency of 1.27 MHz, while the yellow from the thicker PCB has 1.63 MHz. Increasing the thickness of the dielectric layers is validated to attain a higher resonant frequency of about 0.4 MHz in the experiment. It should be noted that, however, increasing the thickness of the dielectric may decrease the cost effectiveness of the PCB and increase the winding loss if the windings are placed closer to the air gap of the cores due to the fringing magnetic flux.

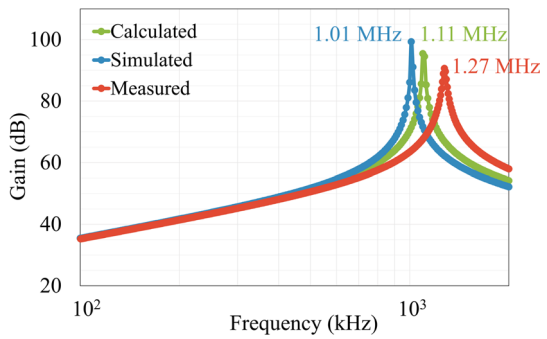


Fig. 10 Overall impedance curves of Fig. 5

Table 3 Modified PCB Stack-Up Information

Layer	Material	Thickness	Permittivity
1	Cu	70 µm	
	Pre-Preg (7628)	400 µm	4.45
2	Cu	70 µm	
	Core	400 µm	4.45
3	Cu	70 µm	
	Pre-Preg (7628)	400 µm	4.45
4	Cu	70 µm	
	Core	400 µm	4.45
5	Cu	70 µm	
	Pre-Preg (7628)	400 µm	4.45
6	Cu	70 µm	

4.3 Planar transformer with reconfiguration of windings

The winding configuration is revised for the reduction of the overlapped area according to Sect. 3.2. Table 4 shows the parasitic capacitances of the revised PT. Inter-layer capacitance, $C_{il,pri}$, and six-capacitance are derived from (11). Table 1 is also applied to calculate the effective permittivity, and $\varepsilon_{r\_67,eff}$ and $\varepsilon_{r\_78,eff}$ for the additional layers have the same value with $\varepsilon_{r\_23,eff}$ and $\varepsilon_{r\_12,eff}$; accordingly, inter-layer capacitance on the secondary side is insignificant since the distance between the layers is sufficiently large, as indicated in Fig. 8. The parallel-plate capacitances $C_{0,12} = 131.48$ pF and $C_{0,78} = 87.2$ pF are computed through (11). The green curve in Fig. 12 was illustrated with the calculated capacitances from Table 2, and the values in Table 4 were represented with purple color. The reconfiguration of the windings yields a resonant frequency of 0.3 MHz than the original transformer.

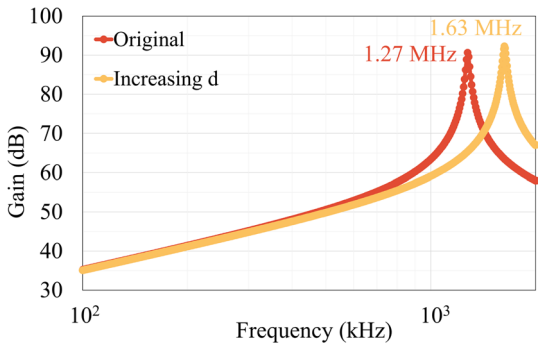


Fig. 11 Comparison with the measured impedance curves of the original and modified PT

Table 4 Calculated Parasitic Capacitances with Two PTs

Parameters	Original [pF]	Reconfiguration [pF]
$C_{il,pri}$	19.42	4.63
C_1	37.11	16.19
C_2	59.38	36.45
C_3	51.96	26.68
C_4	51.96	34.06
C_5	126.18	64.21
C_6	126.18	93.73

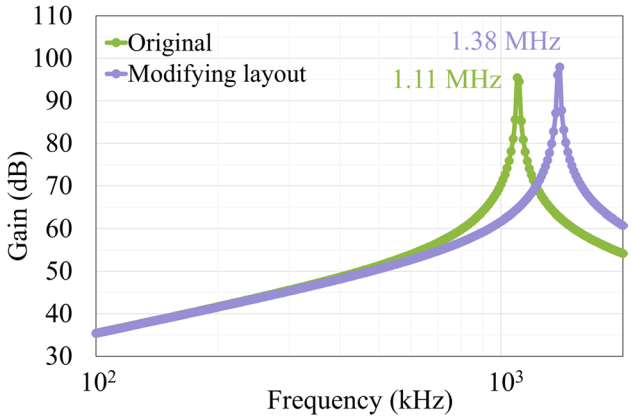


Fig. 12 Comparison with the calculated values of the original and revised PT

5 Conclusion

This paper introduced a detailed explanation of how to calculate the parasitic capacitances of the PT. Parasitic capacitances damage switch devices and generate EMI issues due to the low-impedance path in HF operation. Current oscillation, induced by the resonance with inductance, has a detrimental effect on the converter. Impedance analysis facilitates the verification of the parasitic capacitance effect. A prototype PT with a 12:2 turns ratio and six 2-oz layers is precisely modeled, simulated, and measured. Two methods are suggested for increasing the resonant frequency. Increasing the thickness of the dielectric layers was confirmed as a practical solution to achieve higher resonant frequency. Revising the winding configuration also showed its effectiveness in HF operation by improving the resonant frequency.

Acknowledgements This research was supported by the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT under Grants RS-2023-00217270 and 2022R1C1C1010027, and Chung-Ang University Graduate Research Scholarship in 2021.

Funding Open Access funding enabled and organized by Seoul National University.

Declarations

Conflict of interest Jong-Won Shin was the Associate Editor of the Journal of Power Electronics while conducting this study. Editorial Board Member status has no bearing on editorial consideration.

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Sujeong Lee received the B.S. degree in energy system engineering from Chung-Ang University, Seoul, South Korea, in 2021. She is currently working toward the Ph.D. degree in department of smart cities, Chung-Ang University, Seoul, South Korea. Her research interests include power conversion, planar magnetics, and electric vehicle system.

Seokwon Kim received the B.S. degree in energy system engineering from Chung-Ang University, Seoul, South Korea, in 2021. He received the M.S. degree in department of smart cities from Chung-Ang University, Seoul, South Korea, in 2023. He is currently working toward the Ph.D. degree in department of smart cities, Chung-Ang University, Seoul, South Korea. His research interests include power conversion, converter control, and electric vehicle system.

Jong-Won Shin received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2006 and 2013, respectively. He was a Postdoctoral Researcher with Virginia Tech, Blacksburg, VA, United States, from 2013 to 2015, and a Senior Scientist with the Electronics Research Department, Toyota Research Institute of North America, Ann Arbor, MI, United States, from 2015 to 2018. From 2018 to 2024, he was with Chung-Ang University, Seoul, South Korea. He joined Seoul National University, Seoul, South Korea, in 2024. He was also a Visiting Associate Professor at Nagoya University, Nagoya, Japan, from 2021 to 2024. His research interests include power conversion, energy management, and power semiconductor packaging.

Wonhee Kim received the B.S. and M.S. degrees in electrical and computer engineering and the Ph.D. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2003, 2005, and 2012, respectively. From 2005 to 2007, he was with Samsung Electronics Company, Suwon, South Korea. In 2012, he was with the Power and Industrial Systems Research and Development Center, Hyosung Corporation, Seoul. In 2013, he was a Post-Doctoral Researcher with the Institute of Nano Science and Technology, Hanyang University, and a Visiting Scholar with the Department of Mechanical Engineering, University of California at Berkeley, Berkeley, CA, USA. From 2014 to 2016, he was with the Department of Electrical Engineering, Dong-A University, Busan, South Korea. He is currently a Professor with the School of Energy Systems Engineering, Chung-Ang University, Seoul. His current research interests include nonlinear control and nonlinear observers, and their industrial applications. He has served as an Associate Editor for IEEE/ASME Transactions ON Mechatronics, IEEE ACCESS, and the *Journal of Electrical Engineering & Technology*.