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ORIGINAL ARTICLE

Hybrid DC circuit breaker with reduced fault isolation time and current limiting capability

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Abstract
DC circuit breakers (DCCBs) are key pieces of equipment to ensure the safe and stable operation of DC grids. However, current DCCB schemes generally have problems such as a slow fault clearing speed and a poor current limiting effect. This paper proposes a current-limited hybrid DC circuit breaker (CLHCB) that limits fault current and has fast fault isolation, which reduces the capacity requirements. The current limiting inductor in the fault current limiter (FCL) provides the current limiting capability. In addition, the energy dissipation circuit (EDC) is in parallel to reduce the energy dissipation in metal oxide arresters (MOAs) and to decrease the fault isolation time (FIT), which can reduce the thermal effects of MOAs and improve their reliability. Simulation results verify the working principle and advantages of the proposed CLHCB. When compared to an ABB HCB under the same simulation parameters, the CLHCB enables fault current limiting and faster fault isolation. Finally, experiments have verified the effectiveness of the proposed CLHCB.

Keywords HVDC · DC line fault · Fault current limiter · Energy dissipation circuit · Fault isolation

1 Introduction

In the future, the development of smart grids and the global energy internet will heavily depend on high-voltage, high-capacity DC grid technology [1]. Using HVDC systems based on modular multilevel converters (MMC) has made it easier to build DC grids, which has resulted in new opportunities in the power industry. However, one of the most significant challenges facing DC grid systems is the issue of DC fault protection [2]. Due to their low inertia and impedance, DC grids cannot withstand severe DC short circuits. During a fault, the sub-capacitance module of the converter rapidly drains to the fault point, which leads to a sudden increase in DC current that can cause severe damage to the DC grid [3]. DCCBs are used in DC power grids and do not have a zero crossing point when a short circuit fault occurs. This is a major difference between DCCBs and AC circuit breakers. In addition, when the fault current increases, the biggest challenge for DCCBs is improving the breaking capacity.

The following are some different application scenarios for DCCBs. DCCBs are widely used in industrial automation systems, including robot control, automatic production lines, and factory equipment. In renewable energy systems such as solar panels and wind turbines, DCCBs are used to disconnect circuits to protect battery packs, inverters, and grid connectors. DCCBs are also used in DC power distribution systems, such as ship, train, and aircraft power systems.

Typically, a DCCB is used to interrupt fault current in these situations. However, when the capacity of a DC grid expands, the fault current can surpass the current limit of power electronics in a shorter amount of time [4]. Mechanical DC circuit breakers (MCBs) offer the most cost-effective and energy-efficient solution, but their breaking durations are typically prolonged [5]. On the other hand, solid State DC circuit breakers (SSCBs) can interrupt faulty currents within milliseconds [6]. SSCBs have the advantages of a fast response time and high accuracy. However, they also have the disadvantages of low voltage and current levels and high costs.

Nonetheless, the conduction losses in DC grid systems are severe. Hybrid DC circuit breakers (HCBs) combine

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the benefits of MCBs and SSCBs, which makes them more suitable for DC grid systems [7]. HCBs have the advantages of withstanding high voltages and currents as well as having higher reliability and safety. However, their response speed is not as fast as SSCBs, and they are larger.

To reduce the rate of fault current, the current stresses that DCCBs are subjected to when opening, and the cost of DCCBs, current limiting reactors are frequently fitted to both ends of DC lines and DCCBs. However, the addition of reactors increases the construction cost and affects the dynamic characteristics of the whole DC system, which results in system instability due to the poor damping of specific modes [8]. Consequently, the study of HCBs with a current-limiting function to lessen the pressure on equipment at all levels of a DC system has become a popular topic of domestic and international research.

There are three common methods to embed current limiting function in DCCBs: adding inductors or resistors, operating in the chopper mode with freewheeling diodes, and utilizing the saturation region of switches [9–11]. An effective solution is a DCCB topology that is capable of regulating fault currents, which can safeguard the power electronics of DCCBs. The current-limited DCCB topology proposed in [12] employs DC reactors to limit the increase of fault current that affects the current transmission [13]. The authors of [14] proposed a hybrid fault current limiter topology for HVDC systems. The authors of [15] proposed a DCCB topology with a current limiting function. However, the breaking speed of the fault current is slow. The authors of [16] proposed a solid-state current-limiting DCCB topology. However, it requires a DC voltage source, which limits its use in medium-voltage DC grid systems. The authors of [17] proposed an H-type DCCB with a current-limiting function. However, it requires a large number of IGBTs.

This paper proposes a CLHCB with fast fault isolation. In the event of a fault, the FCL can limit the increase in fault current. This paper provides a detailed analysis of the factors related to MOA energy dissipation during fault current interruptions and introduces an EDC. The CL-HCB can dissipate the inductor energy of the FCL through the EDC, which ensures rapid fault isolation. This paper analyzes the topology composition and DC fault current characteristics, carries out parameter design, and verifies the effectiveness of the proposed CLHCB through simulation and experimental results.

2 Topology of the proposed CLHCB and DC grid fault equivalent circuit

2.1 Topology of the proposed CLHCB

Figure 1 shows the topology of the proposed CLHCB. It is comprised of a load current path and a current commutation path.

The load current path comprises load commutation switches (LCSs) and an ultra-fast mechanical disconnector (UFD). UFDs are mechanical switches that use a high-speed electromagnetic repulsion mechanism to disconnect the LCS from the load current path branch. The UFD isolates the LCS and protects it from high-voltage spikes.

The current commutation path includes an FCL and MB. The FCL includes a current-limiting inductor L_0, an EDC, a series-connected IGBT, and MOA. The EDC is composed of an energy-dissipating resistor R_d and a diode D in series. The MB comprises a series-connected IGBT and MOA2. The diode rectifier is used for bidirectional turn-off. Each MOA connected with the IGBT module in parallel compensates for voltage unbalance.

2.2 DC grid fault equivalent circuit

Within 8 ms following a bipolar short-circuit fault in the DC grid, the AC short-circuit current is insignificant when compared to the sub-module (SM) capacitor discharge current due to the bridge arm reactor. Assuming the converter is not blocked, Fig. 2a shows a standard half-bridge MMC, and Fig. 2b shows an equivalent fault circuit diagram.

R_{arm} is the resistance of one phase of the bridge arm, which consists of the diode in the discharge circuit and the IGBT. R_C, L_C, and C_C are the resistor, inductor, and capacitor in a converter side fault. In addition, Fig. 2b shows the circuit parameters.

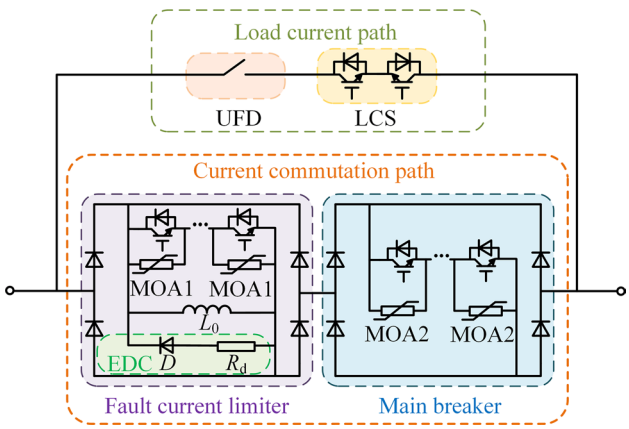

Fig. 1 Topology of the proposed CLHCB

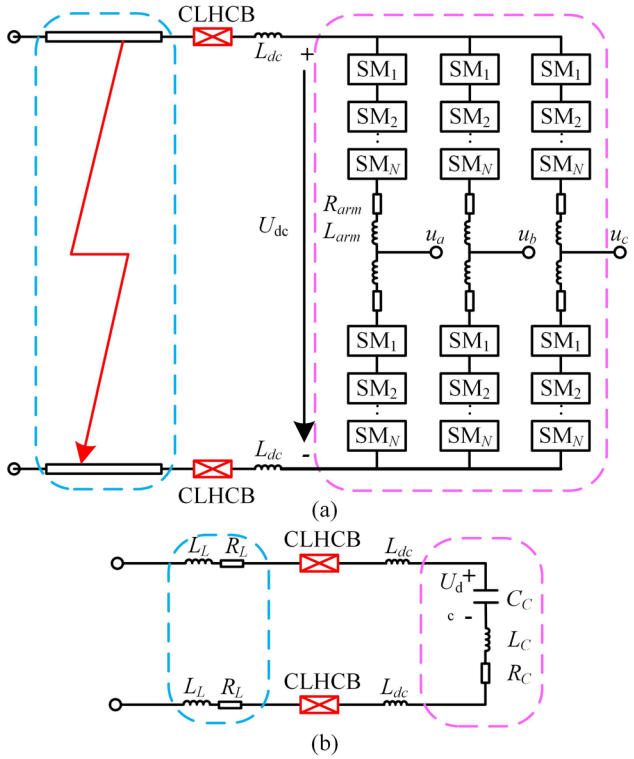

Fig. 2 Discharging circuit under a DC pole-to-pole fault: **a** traditional half-bridge MMC, **b** equivalent fault circuit

$$\begin{cases} R_C = 2R_{arm}/3 \\ L_C = 2L_{arm}/3 \\ C_C = 6C_{arm}/N \end{cases} \tag{1}$$

where C_C is the SM capacitance value, and N is the number of SMs in one phase of the bridge arm.

Since the capacitance of the overhead line to the ground is negligible, the DC line is simplified to a series structure that consists of a resistor and an inductance. The line impedance of the DC side fault circuit is equal to R_L, L_L.

3 DC fault current characteristics of a MMC-HVDC with CLHCB

3.1 L_0 non-parallel with MOA

This section only focuses on the function of the FCL input current-limiting inductor L_0. The fault discharge circuit can be equated to an *RLC* series circuit in the case of a dc fault at t_0. The UFD opens at t_2. At the same time, the IGBT in the FCL opens. In addition, i_{dc} represents the loop current. Figure 3 shows an equivalent discharging circuit after being put into the inductor L_0. The effect on the fault voltage

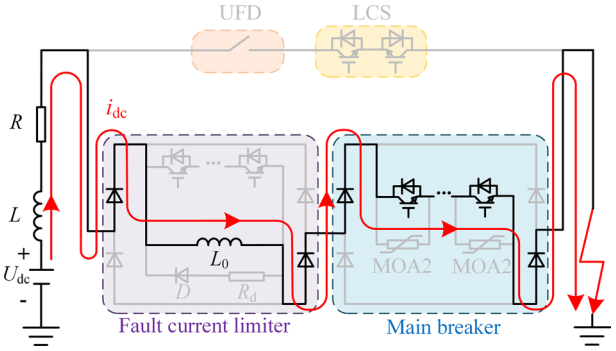

Fig. 3 Equivalent discharging circuit at $t_2 < t < t_4$

during the input of L_0 in the FCL is not considered. At t_4, the IGBT in the MB receives a signal to turn off.

The capacitive voltage U_{dc} and the inductive current I are not zero until the current-limiting inductor L_0 in the FCL begins operation. $R = R_C + R_L$, $L = L_C + L_L + L_{dc}$, and $C = C_C$. In the system, R is less than $2L/C$. Thus, the discharge process before latching is the known circuit beginning state of the oscillatory discharge process. The capacitance–voltage is computed using the formula:

$$U_C = e^{-\alpha t}\left[\frac{U_{dc}\omega_0}{\omega}\sin(\omega t + \beta) - \frac{I}{C\omega}\sin(\omega t)\right] \tag{2}$$

where the circuit parameters can determine the variables in the following formula:

$$\begin{cases} \alpha = \dfrac{R}{2L} \\ \omega = \sqrt{\dfrac{1}{LC} - (\dfrac{R}{2L})^2} \\ \omega_0 = \sqrt{\omega^2 + \alpha^2} = \sqrt{\dfrac{1}{LC}} \\ \beta = \arctan\dfrac{\omega}{\alpha} \end{cases} \tag{3}$$

Generally, $(R/2L)^2 << 1/LC$ can be considered $\omega \approx \omega_0$. The loop current is solved as follows:

$$U_{dc} = R_0 I + (L_0 + L\frac{R_1 + R_L + R_2}{3(R_1 + R_L) + R_2})\frac{dI}{dt} + \frac{(R_1 + R_L)(R_1 + R_L + R_2)}{3(R_1 + R_L) + R_2} I + \frac{2R_2(R_1 + R_L)}{3(R_1 + R_L) + R_2} I \tag{4}$$

When the CLHCB is put into the inductor L_0 at t_1, the instantaneous flux linkage can be obtained as follows:

$$R_e = R_0 + \frac{2R_2(R_1 + R_L)}{3(R_1 + R_L) + R_2} + \frac{(R_1 + R_L)(R_1 + R_L + R_2)}{3(R_1 + R_L) + R_2} \tag{5}$$

According to the law of the conservation of magnetic chains:

$$R_q = \frac{R_1 + R_L + R_2}{3(R_1 + R_L) + R_2} \tag{6}$$

Equation (5) can be solved as follows:

$$i_{dc}(t_{1+}) = \frac{L_C + L_{dc} + L_L}{L_C + L_{dc} + L_L + L_0} i_{dc}(t_{1-}) \tag{7}$$

Based on Eqs. (4–7), i_{dc} is a function of (I, L_0). The *RLC* parameters of the discharge circuit can be referred to as the converter parameters of a Zhangbei four-terminal DC grid to examine the peculiarities of the current i_{dc} under various L_0 configurations in the discharge circuit shown in Fig. 3. The parameters of C, R_C, and L_C are 300 μF, 1.5Ω, and 0.075H. Δt is the fault detection time, and U_{dc} is 320 kV. $L = L_C + L_L + L_{dc}$ can be 0.1H. L_0 is 0.2H. The dc fault point is located on the output side of the converter station, where $R_L = L_L = 0$. The resistance to the load $R_S = 320\Omega$.

The fault current waveform is shown in Fig. 4. There are two inflection points: A and B. The current values are 4.16 kA for i_A and 1.41 kA for i_B.

The verification of Eq. (7) is as follows:

$$i_B = \frac{L}{L + L_0} i_A \tag{8}$$

At t_3, $i_C = 3.52$ kA, the current increase rate after current limiting satisfies the following formula:

$$\frac{k_1}{k_2} = \frac{i_A - 1}{i_C - i_B} = \frac{L}{L + L_0} \tag{9}$$

Theoretically, $\mathrm{d}i_{dc}/\mathrm{d}t = \infty$ and an infinite voltage is instantly produced at both ends of the CLHCB. The current limiting inductor L_0 is parallel to the MOA, which means it does not produce excessive voltage.

Assuming that the inductance L is constant, the fault current in the CLHCB is observed for different values of L_0.

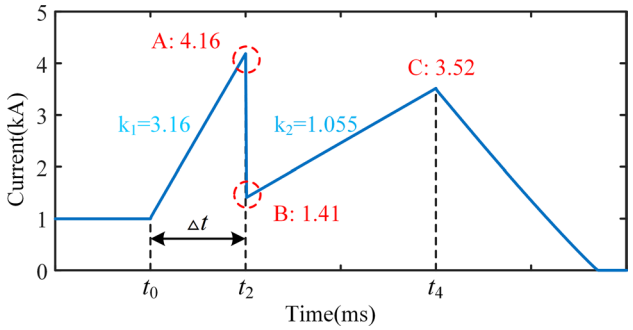

Fig. 4 Fault current waveform

As shown in Fig. 5, when fault current is detected, L_0 is put into the circuit, and the current value drops suddenly. When the inductance L_0 value increases, the peak value of the fault current and the rate of the current increase gradually decrease.

3.2 L_0 parallel with MOA

The fault current changes suddenly when L_0 is put into the faulty circuit. The MOA linked in parallel at both ends of the FCL initiates an operation to absorb a portion of the energy to avoid severe overvoltage. The segmental function characteristic can approach the *U-I* characteristic of the MOA. Figure 6 shows the link between i_{MOA} and u_{MOA} for the *U-I* characteristics, where the reference value is the rated voltage of the MOA U_{MOAN}.

Figure 7 shows an equivalent circuit of CLHCB fault current considering the characteristics of the parallel MOA1 in L_0. i_{MOA} represents the current of MOA1, and i_{L0} represents the current of L_0.

According to the law of the conservation of flux linkage, the instantaneous flux linkage can be determined as follows:

$$\begin{cases} \psi_L\{t_{1-}\} = (L_C + L_{dc} + L_L) \cdot i_{dc}(t_{1-}) \\ \psi_L\{t_{1+}\} = (L_C + L_{dc} + L_L) \cdot i_{dc}(t_{1+}) + L_0\left[i_{dc}(t_{1+}) - i_{MOA}\right] \end{cases} \tag{10}$$

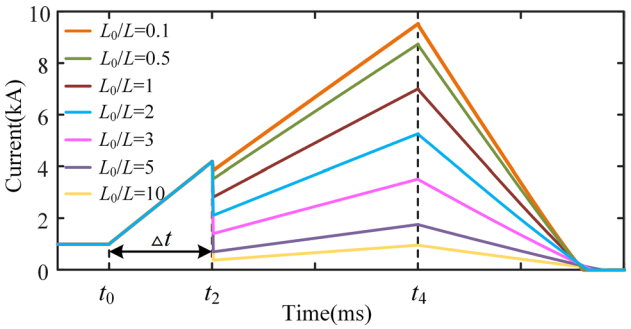

Fig. 5 Fault current waveform under different values of L_0

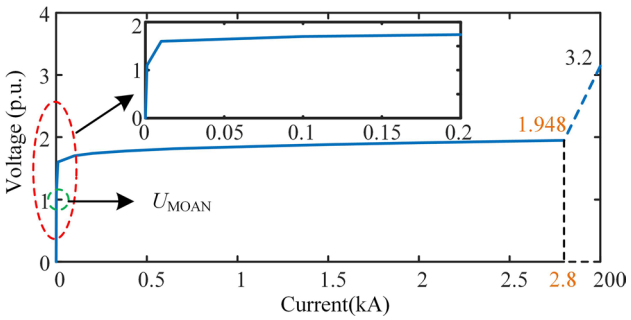

Fig. 6 U-I characteristic of MOA

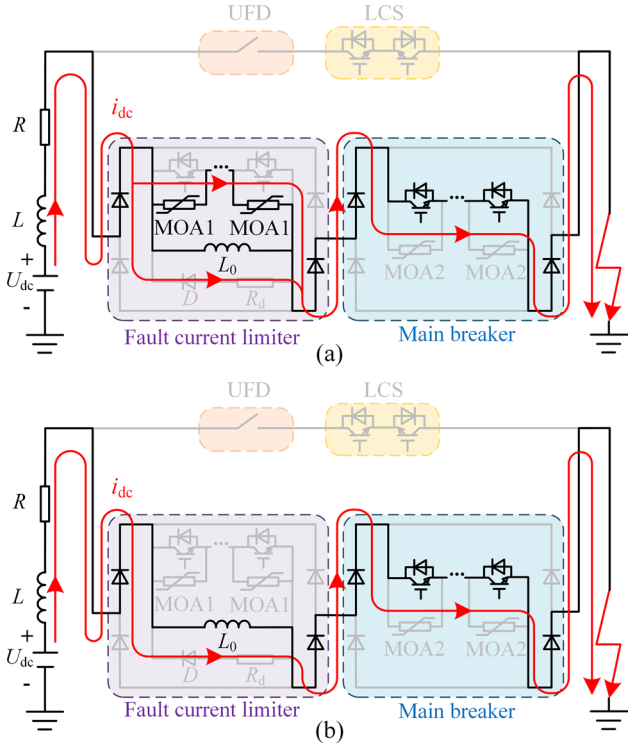

Fig. 7 Equivalent discharge circuit: **a** $t_2 < t < t_3$, **b** $t_3 < t < t_4$

According to the law of the conservation of flux linkage:

$$\psi_L^{\}}(t_{1-}) = \psi_L^{\}}(t_{1+}) \tag{11}$$

Equation (10) can be solved as follows:

$$i_{dc}(t_{1+}) = \frac{L_C + L_{dc} + L_L}{L_C + L_{dc} + L_L + L_0} i_{dc}(t_{1-}) + \frac{L_0}{L_C + L_{dc} + L_L + L_0} i_{MOA} \tag{12}$$

where i_{MOA} and i_{dc} satisfy:

$$i_{dc} = i_{L0} + i_{MOA} \tag{13}$$

The voltage across the MOA is:

$$u_{MOV} = L_0 \frac{d(i_{dc} - i_{MOA})}{dt} \tag{14}$$

Figure 7a shows that the parallel MOA1 prevents rapid changes in faulty current at t_1 by generating overvoltage. As can be seen in Fig. 7b, when $u_{\mathrm{MOA}} < U_{\mathrm{MOAN}}$, MOA1 exits at t_3 and no longer absorbs energy. At this time, the inductor L_0 is fully put into the circuit, which reduces the fault current increasing rate.

Figure 8 shows a waveform diagram of the system current with and without MOA1. At t_3, MOA1 is not operating and no longer absorbs energy. The increasing current rate

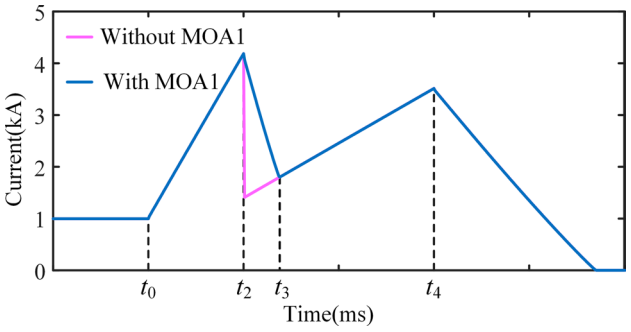

Fig. 8 Fault current waveform

after t_2 is unaffected by the existence or absence of MOA1. Simultaneously, the inductor L_0 is placed into normal circuit functioning, and the fault current increase rate solely depends on the value of L_0.

As shown in Fig. 9, when inductor L_0 increases, the value of i_{dc} decreases further when MOA exits, and the power-dissipated turn-off time of MOA steadily increases. The growth of i_{dc} slows since the MOA exits. Simultaneously, the FIT grows steadily.

3.3 Energy absorbed by MOA

Voltage and current waveforms when the MOA is operating are shown in Fig. 10. I_{max} is the peak fault current. U_{act} and U_{re} indicate the operating and residual voltages of the MOA.

The fault current at t` 3 is $0.5I_{\mathrm{max}}$. U_{re} is the peak voltage.

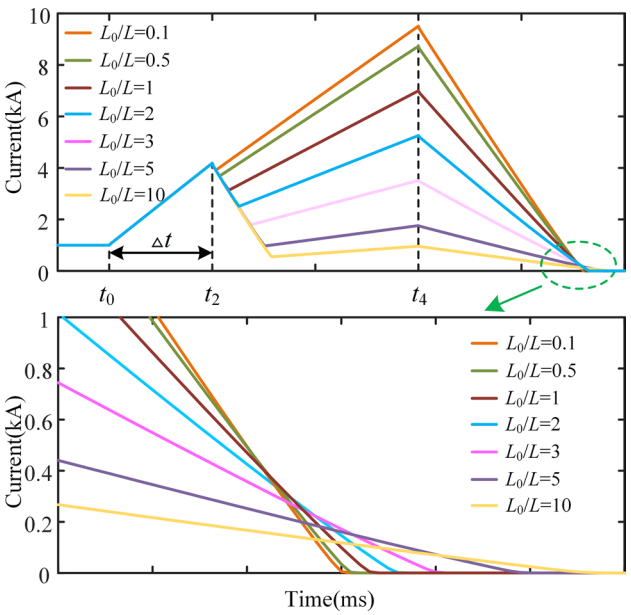

Fig. 9 Fault current waveform under different values of L_0

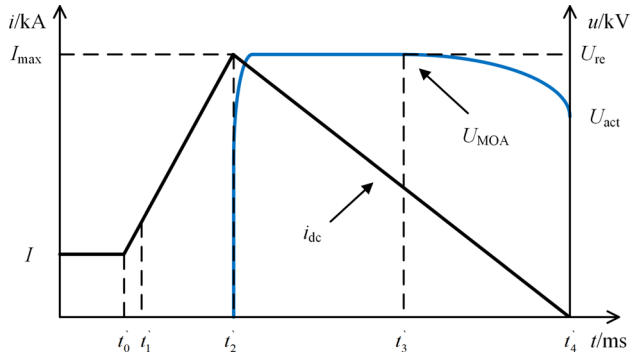

Fig. 10 Voltage and current waveforms during MOA operation

$$U_{\mathrm{MOA}} = U_{\mathrm{re}},\ I > 0.5I_{\max} \tag{15}$$

The following equation can be listed in phases t` 2 through $t$` 3.

$$L_T \frac{di_{dc}}{dt} + U_{re} = U_{dc} \tag{16}$$

The system current of the solution is as follows:

$$i_{dc} = I_{\max} + \frac{U_{dc} - U_{re}}{L_T} \tag{17}$$

The time required for the current to fall linearly from its peak to $0.5I_{\max}$ and the energy provided at this stage is as follows:

$$t_{MOA1} = \frac{L_T I_{\max}}{2(U_{re} - U_{MOA})} \tag{18}$$

$$E_{MOA1} = \int_{t_2}^{t_3} vidt = \frac{3}{8}\frac{U_{re}}{U_{re} - U_{MOA}} L_T I_{\max}^2 \tag{19}$$

After t` 3, the resistance of the MOA is set to RMOA. The following equation can be listed as:

$$L_T \frac{di_{dc}}{dt} + U_{act} + R_{MOA} i_{dc} = U_{dc} \tag{20}$$

The above equation can be solved as follows:

$$i_{\mathrm{dc}} = \frac{1}{2} I_{\max} e^{-R_{\mathrm{MOV}}/L_T t} + \frac{U_{\mathrm{act}} - U_{\mathrm{dc}}}{R_{\mathrm{MOA}}} e^{-R_{\mathrm{MOA}}/L_T t} - \frac{U_{act} - U_{\mathrm{dc}}}{R_{\mathrm{MOA}}} \tag{21}$$

The time required for the current i_{dc} to decrease from 0.5 $I_{\max}$ to zero is as follows:

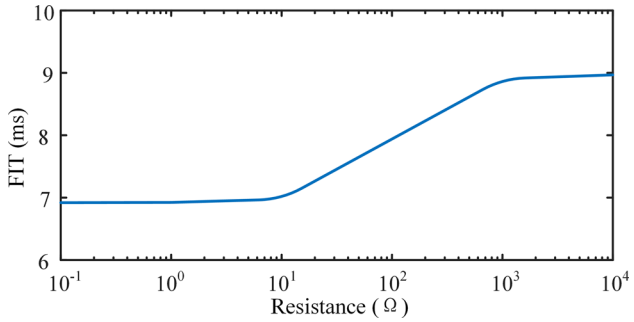

Fig. 11 FITs under different values of R_{d}

$$t_{\mathrm{MOA2}} = -\frac{U_{\mathrm{act}} - U_{\mathrm{dc}}}{R_{\mathrm{MOA}}} + \frac{L_T}{R_{\mathrm{MOA}}} \ln\left[\frac{I_{\max} R_{\mathrm{MOA}} + 2(U_{\mathrm{act}} - U_{\mathrm{dc}})}{R_{\mathrm{MOA}}}\right] e^{-R_{\mathrm{MOA}}/L_T t} \tag{22}$$

The energy absorbed by the MOA during this phase is given as follows:

$$E_{MOA2} = \int_{t_3}^{t_4} vidt = \frac{1}{4}\frac{U_{dc} I_{\max} L_T}{R_{MOA}} \ln\left[\frac{I_{\max} R_{MOA}}{2(U_{act} - U_{dc})} + 1\right] \tag{23}$$

Combining (19) and (23), the total energy absorbed by the MOA is as follows:

$$\begin{aligned} E_{\mathrm{MOA}} &= E_{\mathrm{MOA1}} + E_{\mathrm{MOA2}} + \frac{1}{2} L_T I_{\max}^2 \\ &= \frac{1}{2} L_T I_{\max}^2 + \frac{3}{8}\frac{U_{\mathrm{re}}}{U_{\mathrm{re}} - U_{\mathrm{MOA}}} L_T I_{\max}^2 \\ &\quad + \frac{1}{4}\frac{U_{dc} I_{\max} L_T}{R_{\mathrm{MOA}}} \ln\left[\frac{I_{\max} R_{\mathrm{MOA}}}{2(U_{\mathrm{act}} - U_{\mathrm{dc}})} + 1\right] \end{aligned} \tag{24}$$

The energy absorbed by the MOA consists of two parts: the energy stored in the inductor and the energy supplied by the power supply. Therefore, the proposed CLHCB introduces EDC, as shown in Fig. 1. The EDC dissipates the energy in the inductor and shortens the fault isolation time.

4 Simulation results

4.1 Parameter design

The fault isolation process can select an appropriate R_{d} value. By analyzing the curve-fitted fault isolation times in Fig. 11, it is observed that FIT decreases as R_{d} decreases. However, the R_{d} value cannot be too small due to production process limitations. Therefore, this paper selects an R_{d} value of 10 Ω.

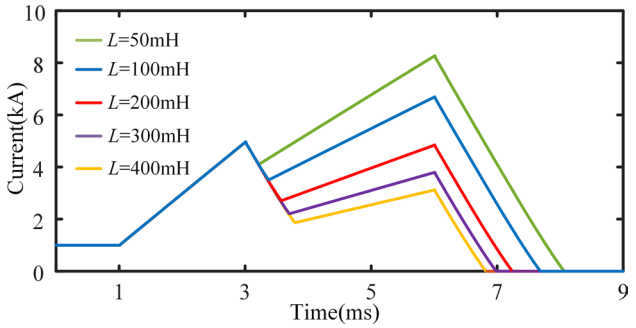

Fig. 12 Current i_{dc} in the case of different values of L_0

Based on the value of R_d taken as 10 Ω, Fig. 12 shows that the input time of L_0 increases with the increase in the value of L_0. To limit the rate of increase of the fault current, L_0 should be input as soon as possible. Therefore, the value of L_0 should not be too large.

However, once the current limiting inductor L_0 is put into full operation, the secondary increase rate of the fault current slows down with the increase of L_0, which can reduce the manufacturing difficulty of the circuit breaker. Thus, the value of L_0 should not be too small. The value of the current limiting inductor is selected as 200 mH.

4.2 CLHCB simulation verification

A monopolar test system integrated within the PSCAD/EMTDC platform is used to validate the proposed CLHCB. The major parameters of the simulation model are shown in Table 1.

Figure 13 shows a control flowchart of the CLHCB in the present interruption mode after the onset of a fault. A short circuit occurs at t_0. A trip signal is sent to the CLHCB at t_1. At t_2, the UFD is entirely disconnected. Simultaneously, the IGBT opens in the FCL. MOA1 quits operation after absorbing energy at t_3. At t_4, the IGBT opens in the MB. MOA2 absorbs the energy of the fault current during turn-off until the CLHCB isolates the fault at t_5. The simulation verification process is separated into six periods.

(1) $t < t_0$: The system is operating stably in this stage, and the fault occurs at t_0.
(2) $t_0 < t < t_1$: The proposed CLHCB receives the trip signal at t_1. Figure 14a shows the present current flow path of i_{dc}.
(3) $t_1 < t < t_2$: The LCS is opened at t_1, while the IGBTs in the FCL and MB turn on. The UFD starts to turn off. The fault current increases rapidly during this period. Figure 14b shows the present current flow path of i_{dc}.
(4) $t_2 < t < t_3$: Fig. 14c shows the present flow path of i_{dc}. After the UFD in the load current path is opened to a safe distance, the IGBTs in the FCL are turned off. The voltage across MOA1 in the FCL reaches its operational voltage. When MOA1 finishes absorbing fault current energy at t_3, its current value decreases to zero. The UFD opens when the safe breaking distance is reached. The UFD is a mechanical switch with an opening resistance that is much higher than the opening resistance of the LCS. The UFD prevents overvoltage in the LCS.

Table 1 Major parameters of the simulation model

Parameters	Value
Rated voltage U_{dc}	320 kV
Equivalent inductance L	150 mH
Equivalent resistance R	3 Ω
current-limiting inductor L_0	200 mH
EDC R_d	10 Ω
Load resistance R_s	320 Ω

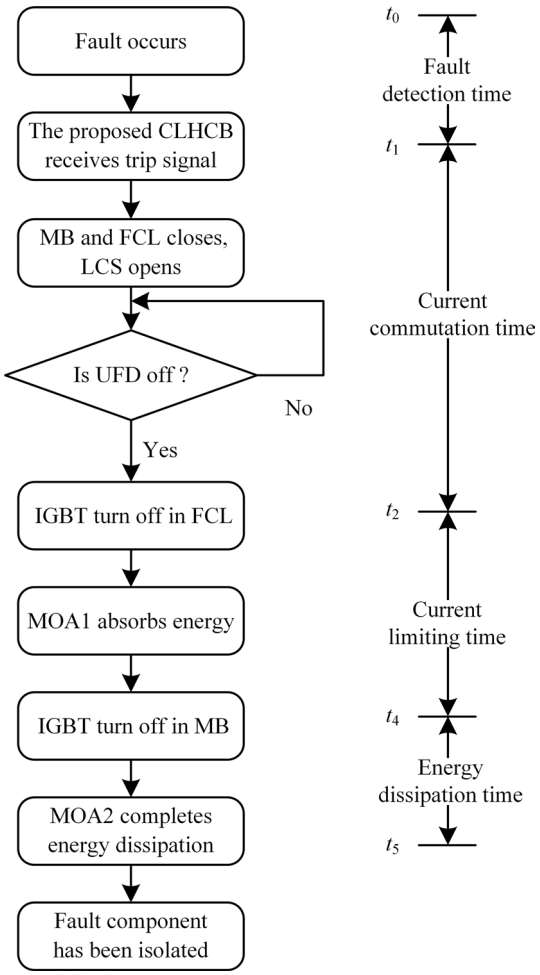

Fig. 13 Control flowchart of the proposed CLHCB

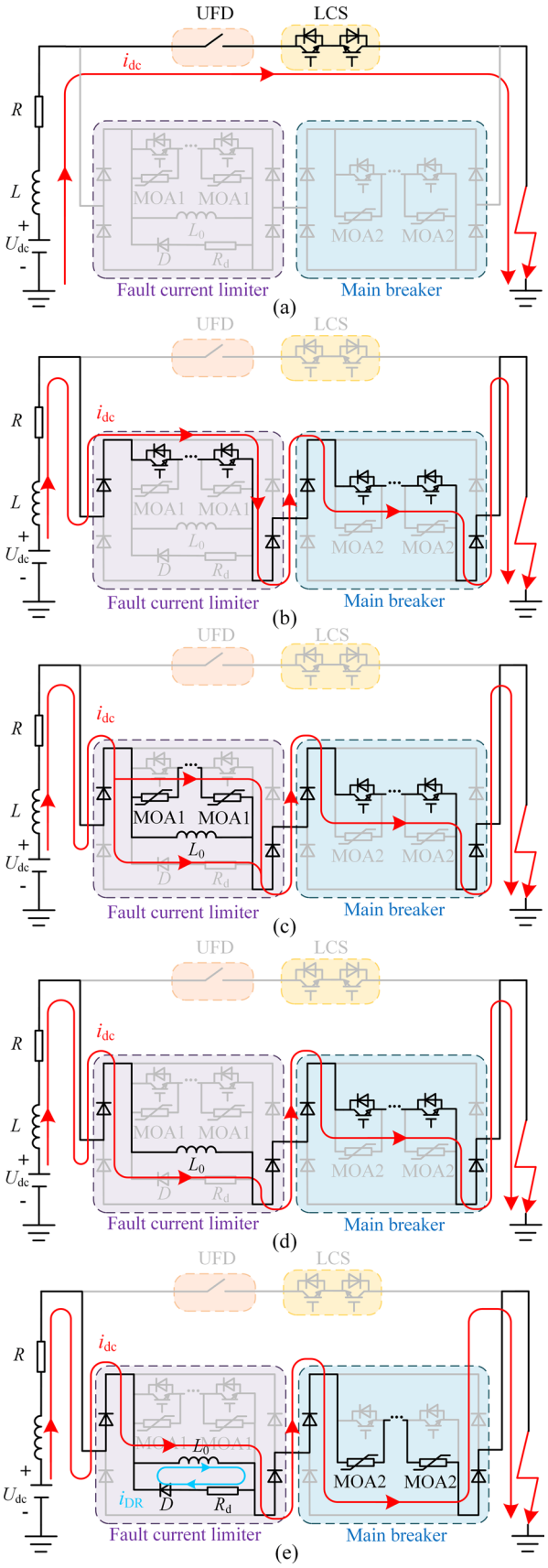

Fig. 14 Working principle of the CLHCB: **a** $t_0<t<t_1$, **b** $t_1<t<t_2$, **c** ▶ $t_2<t<t_3$, **d** $t_3<t<t_4$, **e** $t>t_4$

(5) $t_3<t<t_4$: Fig. 14d shows the present flow path of i_{dc}. During this period, MOA1 exits operation after completing fault current energy absorption, and L_0 in the FCL is input into the circuit. As can be seen in Fig. 15a and Fig. 15b, the current growth rate is noticeably slowed, and the proposed CLHCB has achieved the current limiting function.

(6) $t>t_4$: Fig. 14e shows the present flow path of i_{dc} and i_{DR}. L_0 starts releasing energy through the EDC at t_4. The voltage at both ends increases when the IGBT in the MB is turned off at t_4. MOA2 starts to operate for energy dissipation after its operating voltage is reached, and the fault current drops rapidly. When the fault current is reduced to zero, fault isolation is achieved. Figure 15c shows the energy dissipated by the MOA.

Figure 16 shows comparative simulation results with or without the fault current limit function. From the simulation comparison results, it can be seen that the CLHCB can reduce the fault current value by 58.3% 5 ms after fault occurrence. The fault current limiting function is realized.

4.3 CLHCB simulation verification in a dc grid

Figure 17 shows the system for the simulation test. The main parameters of the simulated test system are listed in Table 2.

This section assesses the feasibility of the proposed CLHCB in a DC grid. Before $t=3$ s, the system operated in a stable state. At $t=3.5$ s, a fault occurred, which caused a rapid increase in the current within the faulty line. The CLHCB received a trip signal at $t=3.5005$ s, followed by the opening of the UFD and the IGBT in the FCL. The voltage subsequently surged to the action voltage of MOA1, with the current limiting inductor L_0 being fully incorporated into the circuit to constrain the current increase rate once the current in MOA1 decreased to zero. At $t=3.505$ s, the IGBTs in the MB were switched off, and MOA2 absorbed the fault energy until fault isolation is completed.

A fault current waveform of the system is shown in Fig. 18. Simulation results show that the CLHCB achieves the function of fault current limitation and fault isolation.

4.4 Performance comparison

Using the same parameter settings, Fig. 19a depicts that the fault isolation speed of the CLHCB with EDC is 27.4% faster than that of the CLHCB without EDC. Figure 19b compares the energy absorption of the MOA. EDC consumes the energy stored in L_0, which reduces the

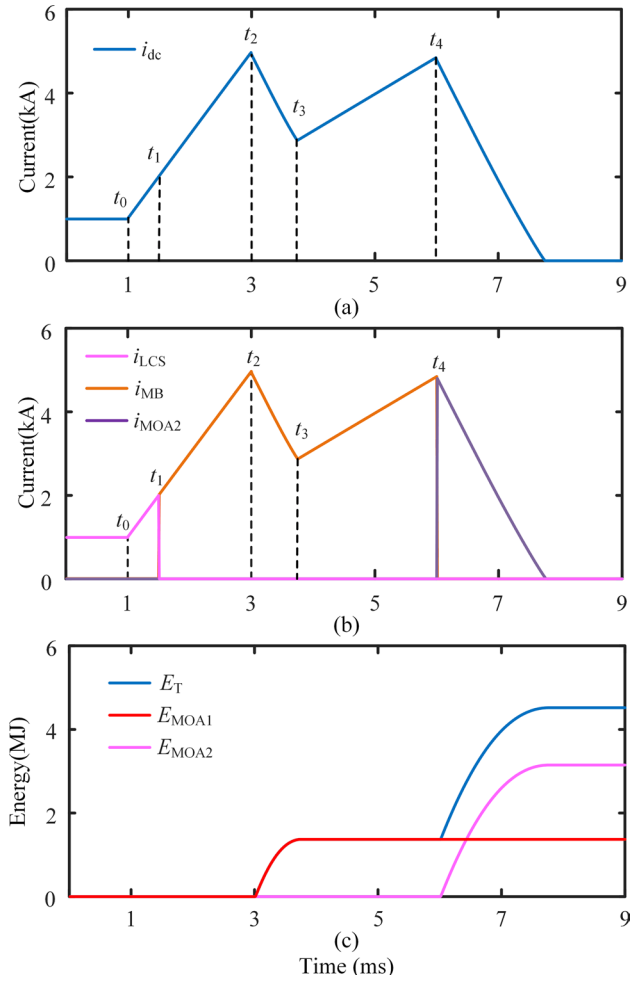

Fig. 15 Simulation results: **a** currents i_{dc} flowing through CLHCB, **b** currents i_{dc}, i_{LCS}, i_{IGBT}, i_{MOA2} flowing through, LCS, IGBT, and MOA2, **c** E_T, E_{MOA1}, and E_{MOA2} absorbs the total energy (the absorbed energy of MOA1 and MOA2)

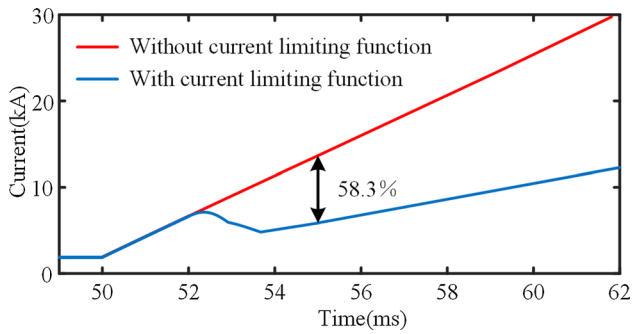

Fig. 16 Fault current comparison waveforms

MOA energy consumption by 46.4% when compared to the CLHCB without EDC.

The proposed CLHCB is compared to the ABB HCB for a complete performance evaluation using the same simulation

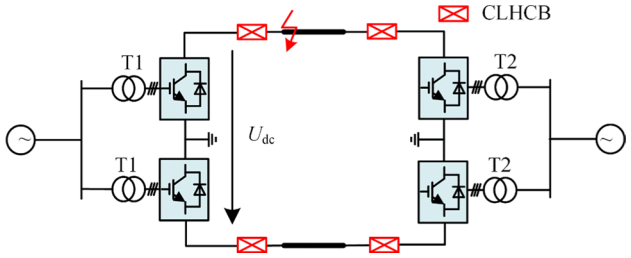

Fig. 17 Simulation test system

Table 2 Simulation test system parameters

Parameter	Symbol	Value
DC voltage	U_{dc}	640 kV
Voltage ratio of transformer	T1	33/370
Voltage ratio of transformer	T2	370/230
Line reactance	L_n	130 mH
Number of sub-modules	n	76
Overhead line length	l	120 km

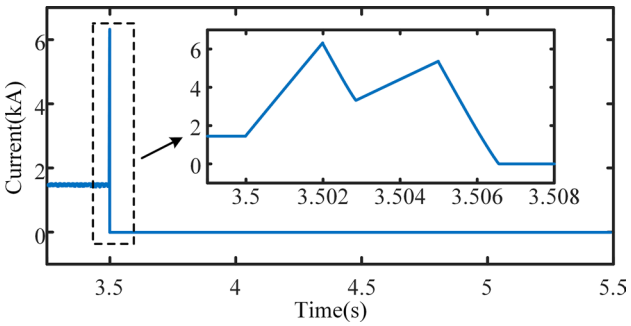

Fig. 18 Fault current waveform of the system

parameters. Figure 20a illustrates fault current simulation results. The CLHCB with a fault current-limiting function exhibits a current of only 4.8 kA at the same moment, which represents a reduction of 55.6% when compared to the ABB HCB. In terms of FIT, the fault isolation speed of the CLHCB is 22.9% faster than that of the ABB HCB. Figure 20b shows result of the energy absorption of the MOA. When compared to the ABB HCB, the energy absorption of the MOA in the CLHCB was reduced by 70.8%.

5 Economic analysis

This paper compares the proposed CLHCB to the ABB HCB economically. Semiconductor components and the MOA are more costly than other components. The commercially

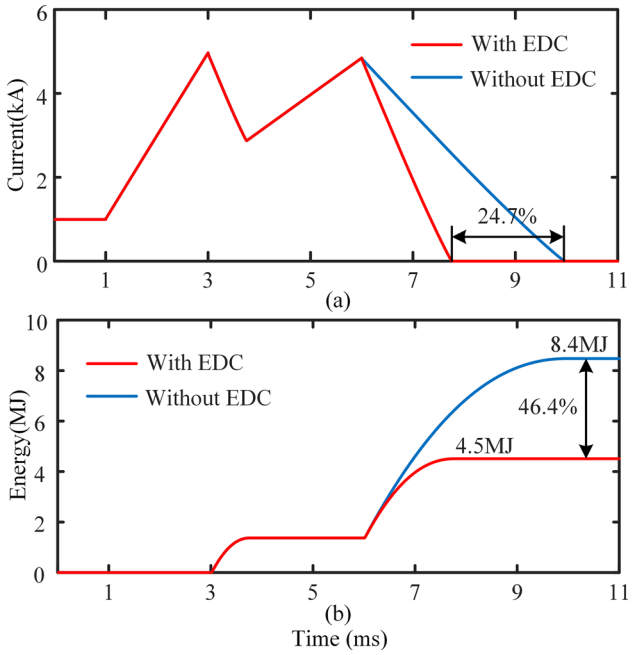

Fig. 19 Simulation comparison results: **a** fault current waveforms, **b** energy absorption by MOA

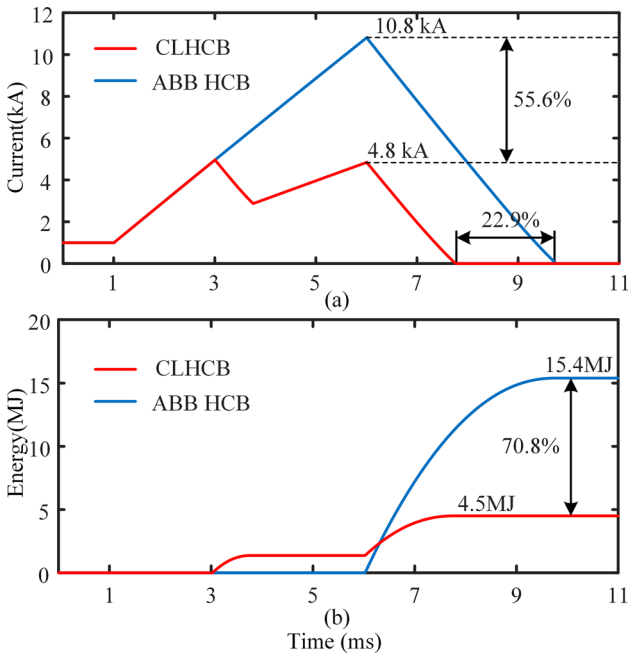

Fig. 20 Simulation comparison results: **a** fault current waveforms, **b** energy absorption by MOA

available high-power IGBT module 5SNA 2000K451300 (4.5 kV, 2 kA, 2480 USD), the current limiting inductor L_0 PKK-320–5000-200 (320 kV, 5 kA, 200 mH 0.95MUSD) and the MOA are 15,485 USD/MJ.

Table 3 Simulation DC grid system parameters

Component	Solutions	
	CLHCB	ABB HCB
IGBT	648	1290
MOA (MJ)	4.5	15.4
Current limiting inductor	0.95	0
Total cost (MUSD)	2.62	3.44

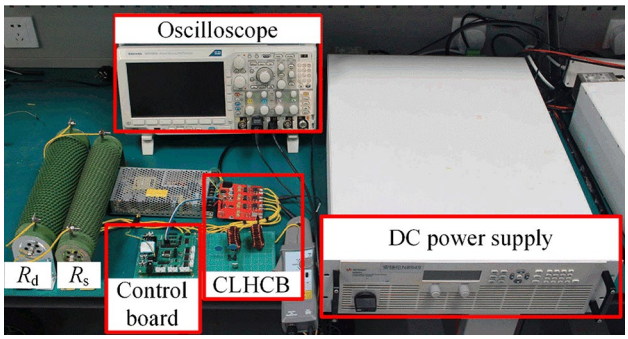

Fig. 21 Experimental platform

Table 4 Major parameters of the experimental platform

Parameters	Value
Rated voltage U_{dc}	50 V
Equivalent DC line inductor L	3 mH
current limiting inductor L_0	4 mH
EDC R_d	5 Ω
Load resistance R_s	25 Ω
MOA	14D101K

Table 3 shows that the CLHCB solution described in this paper can lower investment costs by 23.8%. The CLHCB with current-limiting capabilities is more cost-effective and can greatly minimize the need for power electronics.

6 Experimental verification

To verify the effectiveness of the proposed CLHCB, the prototype shown in Fig. 21 was established based on the experimental platform shown in Fig. 1. The main parameters of the prototype are provided in Table 4. To ensure precise control of the action time, the UFD in the experimental circuit is equivalent to an IGBT module.

The experimental fault current and MB voltage are shown in Fig. 22. After a fault occurs, the CLHCB receives the shunt signal and starts to operate. When the current limiting

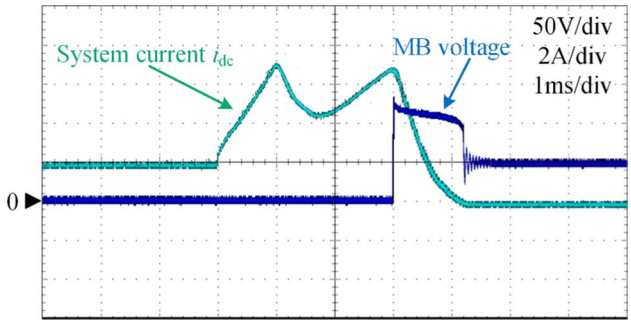

Fig. 22 MB voltage and system current waveforms

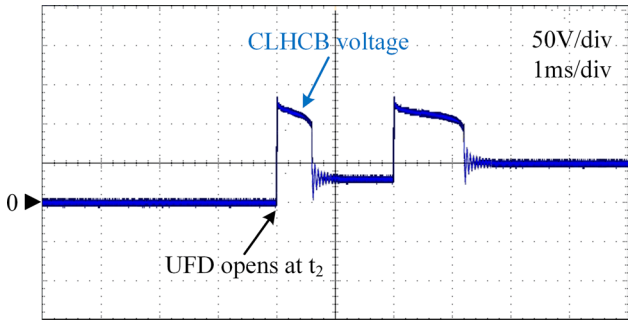

Fig. 23 CLHCB voltage waveform

inductor is fully engaged in the circuit, the growth rate of the fault current is significantly reduced compared to when the fault first occurred. In addition, the fault current limiting function is realized. The IGBT of the MB then disconnects, and MOA2 starts to absorb the fault current energy. Then the voltage across the MB stabilizes to the supply voltage.

The voltage across the CLHCB in the experiment is shown in Fig. 23. When the UFD is turned off, the voltage at both ends of it increases and then falls until it stabilizes to a certain value. When the MB is turned off, the voltage reaches the operating voltage of MOA2, which starts to absorb the energy of the fault current. Subsequently, the fault current decreases to zero, and the voltage at both ends of the CLHCB is stabilized at the supply voltage.

7 Conclusion

This paper proposed a current-limited HCB. An FCL was shown to reduce the capacity requirement of the CLHCB, speed up fault isolation, and provide a current limiting function. An EDC was shown to consume the energy stored in L_0 and to reduce the energy absorbed by MOA2, which reduced the FIT. Simulation results showed that the energy dissipation of the MOA can be reduced by 70.8% when compared to the ABB HCB, with a 22.9% lower FIT. When compared with the ABB HCB solution, the topology of the proposed CLHCB reduced investment cost by 23.8%. Finally, experiments verified the effectiveness of the proposed CLHCB.

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Data availability The data are available from the corresponding author on reasonable request.

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