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ORIGINAL ARTICLE

Balancing control scheme of DC-link capacitor voltages for five-level hybrid T-type inverters without auxiliary circuit

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Abstract
In this paper, a balancing control scheme of DC-link capacitor voltages for five-level hybrid T-type (5L-HT) inverters is proposed, where existing auxiliary balancing circuit is eliminated. The 5L-HT inverter has a significant advantage of the reduced number of devices compared with other five-level inverter topologies. However, this inverter requires an auxiliary balancing circuit, which is used to rectify the voltage imbalance at the DC-link capacitors, and thus negates the competitiveness of this topology in terms of device count and converter volume. To eliminate the auxiliary circuit, a carrier-overlapped PWM (COPWM) is applied in place of the conventional level-shifted PWM (LSPWM) to control the neutral-point currents, where the duty ratios of switches are adjusted by PI controllers. As a result, although the THD of the output voltage is rather increased, the cost and volume are saved by 27% and 52%, respectively, for a 1-MW/6.6-kV system. The effectiveness of the proposed balancing control method for the 5L-HT inverter has been verified through the simulation and experimental results for the prototype hardware.

Keywords Auxiliary balancing circuit · Carrier-overlapped pulse-width modulation · Capacitor voltage balancing · Level-shifted pulse-width modulation · Multilevel inverter · Medium voltage application

1 Introduction

Various types of multi-level inverter (MLI) topologies have been studied and developed for medium and high-voltage applications for several decades since they have several advantages, such as lower total harmonic distortion (THD), reduced voltage stress of devices, low *dv/dt*, reduced electromagnetic interference (EMI), etc. [1–4].

There are three typical types of MLI topologies, namely neutral-point-clamped (NPC), flying-capacitor (FC) and cascaded H-bridge (CHB) inverters. The three typical topologies have a common disadvantage that the number of required devices increases significantly as the voltage level becomes higher. In addition, the NPC inverter has the drawback that the loss of the switches is distributed unequally, the FC inverter has the complexity of control and the CHB inverter requires an independent isolated DC source for each bridge circuit [5–8]. Therefore, lots of researchers have explored and developed various topologies with the reduced number of devices, modulation technique and capacitor voltage balancing control for various applications such as photovoltaic (PV) inverters, motor drives, grid-connected systems and electric vehicles (EV) [9–17].

A five-level hybrid T-type (5L-HT) inverter topology, which consists of two half-bridge (HB) cells and one 3L-T-type cell per phase, has been proposed in [18]. The number of devices and power loss of the 5L-HT inverter are significantly reduced compared with other types of five-level inverters [19–24]. However, it is difficult to maintain the voltages of DC-link capacitors with the conventional level-shifted pulse-width modulation (LSPWM) over the full range of the modulation index (MI) [19, 24, 25]. Hence, an auxiliary balancing circuit (ABC) had to be used in [18]. The ABC consists of two active switches, two inductors and one diode. This circuit supports to boost the middle capacitor voltages as a boost DC–DC converter. However, the rated voltage of the auxiliary devices is relatively high, and the large volume of the inductors is a burden.

Meanwhile, a carrier-overlapped pulse-width modulation (COPWM) has been proposed to control the DC-link capacitor voltage for NPC type of inverters [26, 27]. In the

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COPWM, two carriers are basically level-shifted, and the other carriers are modified by being bent at particular points between two level-shifted carriers. In the LSPWM, all voltage levels are generated in a fundamental period (50/60 Hz). To change the voltage level, the large change of duty ratio is required in the LSPWM. On the other hand, in the COPWM, all voltage levels are generated in a carrier period. So, the COPWM can create different voltage levels with a very small change in duty ratio, which makes it possible to control the neutral-point current generated according to each voltage level. Therefore, the COPWM has the flexibility to control the DC-link capacitor voltage without significantly affecting THD of output current.

In this article, a balancing control scheme of the DC-link capacitor voltage for the 5L-HT inverter without the auxiliary balancing circuit is proposed. For this purpose, the COPWM is applied to control the duty ratio of each switch. The effectiveness of the balancing capability of the DC-link capacitor voltage for the 5L-HT inverter is verified by the various simulation results for medium-voltage and high-power applications. Moreover, the experimental verification for a prototype hardware set-up is provided.

2 Structure and operation scheme of 5L-HT inverter

Figure 1 shows the three-phase circuit diagram of the 5L-HT inverter. The inverter consists of a 3L-T-type cell and two HB cells per phase and four common DC-link capacitors. The 5L-HT inverter requires only 24 active switches and four DC-link capacitors without any clamping diode and flying capacitor. Comparing with other type of 5L-inverters, the number of devices is significantly reduced. A comparison of several five-level inverter topologies is listed in Table 1 [19–24].

Figure 1a shows the 5L-HT inverter with the auxiliary balancing circuit (ABC) needed for the DC-link capacitor voltage control. The ABC consists of two active switches, one diode and two inductors. Since the middle capacitors (C_1, C_2) of the 5L-HT inverter are naturally discharged when the LSPWM is applied, the ABC is utilized to boost the capacitor voltages. Likewise, the voltage balancing control can be easily achieved with the ABC, but the additional cost should be paid and the system volume is bulky.

The auxiliary switches ($S_{\text{aux1}}, S_{\text{aux2}}$) and diode ($D_{\text{aux}}$) require the high-voltage rated devices. The blocking voltage of additional devices is calculated as:

$$V_{S_{\text{aux}}} = V_{S_{\text{aux1}}} = V_{S_{\text{aux2}}} = \frac{V_{\text{dc}}}{4} + V_{\text{Laux}}, \tag{1}$$

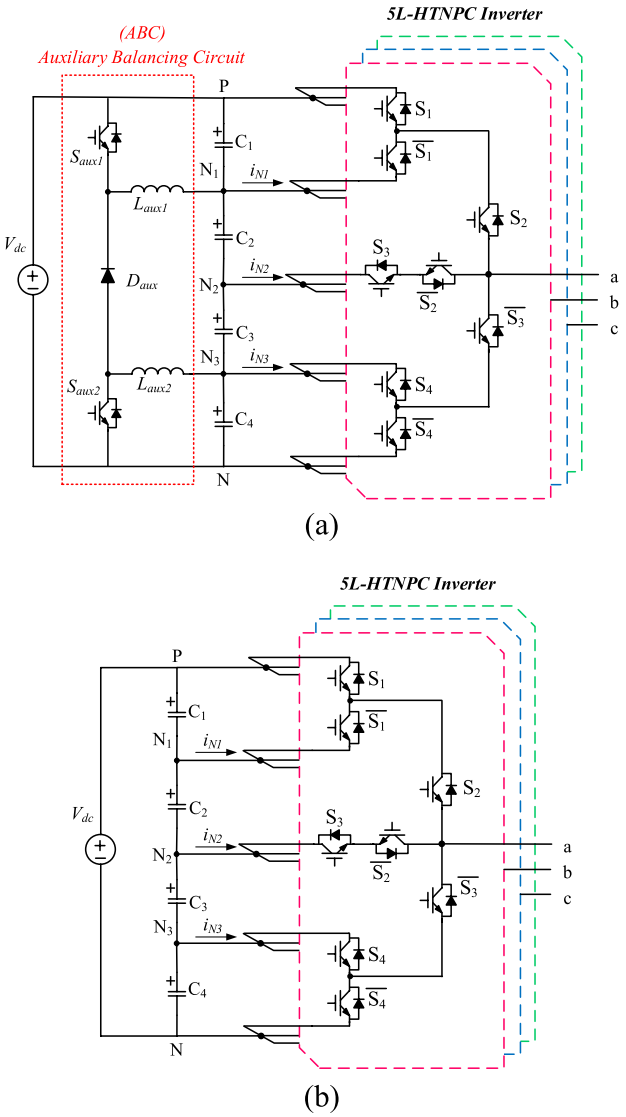

Fig. 1 Three-phase 5L-HT inverter: **a** with auxiliary balancing circuit; **b** without auxiliary balancing circuit

$$V_{D_{aux}} = \frac{V_{dc}}{2} + 2V_{Laux}, \tag{2}$$

where $V_{S_{\text{auxn}}}$, V_{Laux} and $V_{D_{\text{aux}}}$ are the voltage stress of auxiliary active switches, inductor and diode, respectively. The maximum voltage stresses across active switches and diode are approximately $V_{\text{dc}}/2$ and V_{dc}, respectively.

The voltage fluctuation of the DC-link capacitors is caused due to neutral-point (NP) currents. The switching states for the 5L-HT inverter and the NP currents according to the voltage level are listed in Table 2, where the letter "x" means the phase and the "1" and "0" indicate ON and OFF state of switches, respectively. When the voltage level

Table 1 Comparison of device counts for different five-level inverters

Topology	Components					ABC
	SW	CD	DL	FC	DC	
5L-NPC	24	18	4	0	1	N
5L-ANPC	24	0	2	3	1	N
[19, 24]	24	0	3	3	1	N
[20]	24	6	0	9	1	N
[21]	20	6	2	0	2	N
[22]	21	12	2	3	1	N
[23]	30	0	3	6	1	N
5L-HT	24	0	4	0	1	R

SW active switches, *CD* clamping diodes, *DL* DC-link capacitors, *FC* flying capacitors, *DC* DC sources, *N/R* not required/required

is either V_{dc} or 0, the NP current does not flow through DC-link capacitors, and thus barely affects the capacitor voltages. However, NP currents i_{N1}, i_{N2} and i_{N3} flow through each neutral point when the voltage level is $3V_{dc}/4$, $V_{dc}/2$ and $V_{dc}/4$, respectively. These NP currents causes the capacitor voltage imbalance. So, the NP currents need to be controlled to suppress the voltage imbalance, by which the ABC can be eliminated. The 5L-HT inverter without the ABC is shown in Fig. 1b.

From Table 2, the pole voltage V_{xN} is expressed by the sum of four switching states as.

$$V_{xN} = (S_{x1} + S_{x2} + S_{x3} + S_{x4}) \cdot \frac{V_{dc}}{4}, \tag{3}$$

where S_{xn} is the state of switch in phase x.

3 Modulation and balancing control of DC-link capacitor voltage scheme

If the LSPWM is applied to the 5L-HT inverter, the DC-link capacitor voltage is not able to be controlled only by modulation technique. Since the modulation technique has the carriers with the different level in the same phase, the duty ratio of each device cannot be adjusted as long as the reference voltage waveform is not modified in a carrier period. Therefore, in this work, a carrier-overlapped PWM (COPWM) is applied to the 5L-HT inverter to eliminate the ABC, which has the distorted and level-shifted carriers [26–28]. Since these modified carriers can produce all voltage levels from 0 to V_{dc} in a switching period, the duty ratio can be adjusted with no voltage distortion which is an issue in the LSPWM.

The concept of the COPWM is shown in Fig. 2. The COPWM for five-level inverters has two level-shifted and two bent carriers. It is hard to implement in DSP due to the distorted characteristics of carriers. Alternatively, the equivalent transformation with a single carrier and multi-reference voltages is performed rather than multi-carriers and a single reference voltage. The reference voltage is given by

$$v_{refx} = 1.15 \cdot m \cdot 2 \cdot (\sin(\omega t + \theta)) \quad 0 \le m \le 1, \tag{4}$$

where m, ω and θ is the modulation index (MI), fundamental angular frequency and phase angle of the voltage. The offset voltage is injected into the reference voltage, which can extend the utilization of the DC-link voltage by 15.5%. The offset component is given by [19]

$$v_{ofs} = -\frac{\max(v_{refa}, v_{refb}, v_{refc}) + \min(v_{refa}, v_{refb}, v_{refc})}{2}. \tag{5}$$

The equivalent transformation from multi-carriers to multi-references is calculated according to the polarity of the reference voltage as

$$\begin{cases} v_{refx1} = d_{x1} = \frac{1}{2}(v_{refx} - 2) \\ v_{refx2} = d_{x2} = \frac{1}{3}(v_{refx} - 1) \\ v_{refx3} = d_{x3} = \frac{1}{6}(v_{refx} + 2) \\ v_{refx4} = d_{x4} = 1 \end{cases} \quad 0 \le v_{refx} < 2, \tag{6}$$

$$\begin{cases} v_{refx1} = d_{x1} = 0 \\ v_{refx2} = d_{x2} = \frac{1}{6}v_{refx} \\ v_{refx3} = d_{x3} = \frac{1}{3}v_{refx} \\ v_{refx4} = d_{x4} = \frac{1}{2}v_{refx} \end{cases} \quad -2 \le v_{refx} < 0, \tag{7}$$

Table 2 Switching states of 5L-HT inverter

S_{x1}	S_{x2}	S_{x3}	S_{x4}	i_{N1}	i_{N2}	i_{N3}	V_{xN}
1	1	1	1	–	–	–	V_{dc}
0	1	1	1	i_{ox}	–	–	$3V_{dc}/4$
0	0	1	1	–	i_{ox}	–	$V_{dc}/2$
0	0	0	1	–	–	i_{ox}	$V_{dc}/4$
0	0	0	0	–	–	–	0

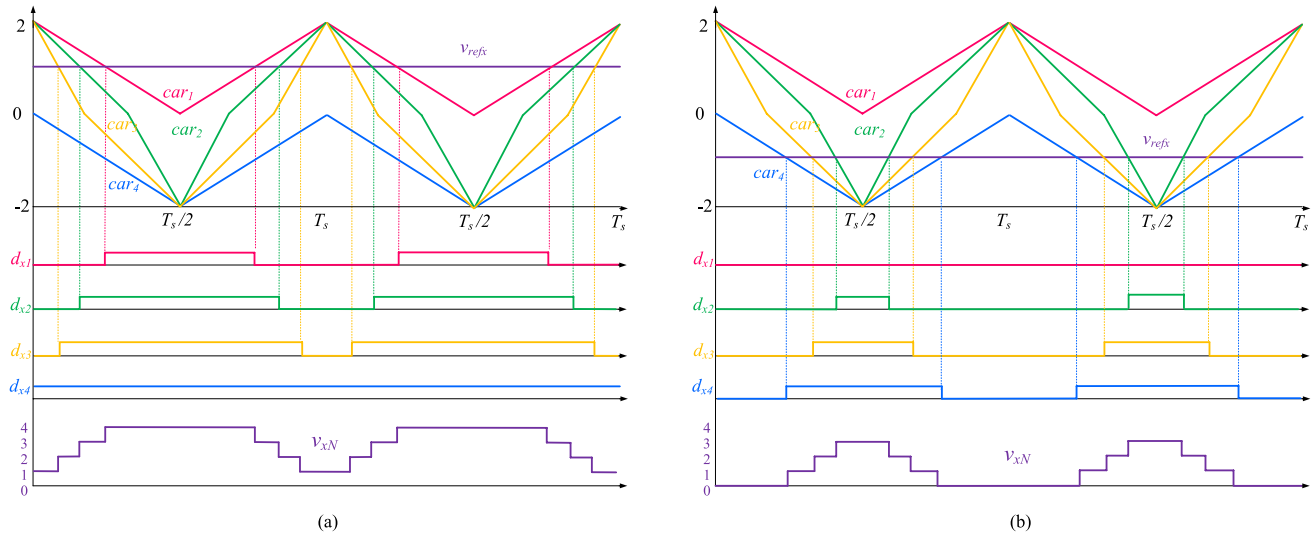

Fig. 2 COPWM according to the voltage reference: **a** positive; **b** negative

where $v_{\mathrm{ref}xn}$ and $v_{\mathrm{ref}xn}$ are multi-reference voltage and duty ratios of switches, respectively.

The multi-reference voltages are normalized between 0 and 1 through the equivalent transformation, which means that the multi-reference voltages are equal to duty ratios of switches.

The NP currents flow through the N_1, N_2 and N_3 when the voltage level is $3V_{dc}/4$, $V_{dc}/2$ and $V_{dc}/4$, respectively. From Fig. 2a and b, the NP currents in a carrier period are expressed as

$$\begin{aligned} i_{N1x} &= (d_{x2} - d_{x1}) \cdot i_{ox}, \\ i_{N2x} &= (d_{x3} - d_{x2}) \cdot i_{ox}, \\ i_{N3x} &= (d_{x4} - d_{x3}) \cdot i_{ox}, \end{aligned} \tag{8}$$

where i_{N1x}, i_{N2x} and i_{N2x} are NP currents flowing through N_1, N_2 and N_3, respectively. The NP currents are expressed as the product of the difference between duty ratios of the two consecutively numbered switches and the output current of each phase, which means that the NP currents are determined according to the duty ratio and the output current (i_{ox}).

The voltage fluctuations at the DC-link capacitors are caused by the NP currents. Figure 3 shows the flow of NP currents according to the voltage level. Assuming that the DC-link capacitance is $C_1 = C_2 = C_3 = C_4 = C$, the deviation voltage of capacitors is expressed as

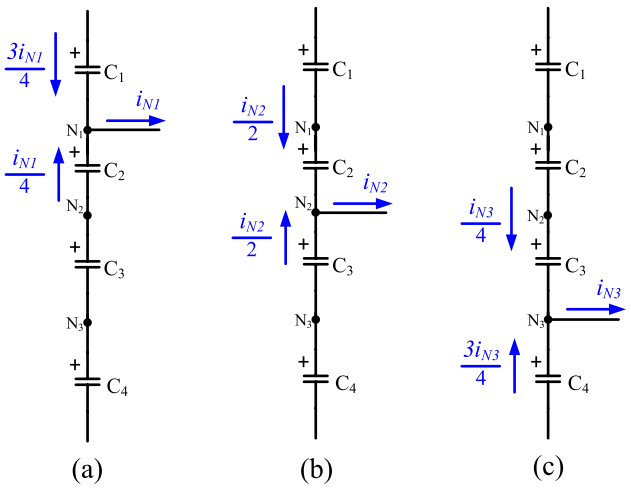

Fig. 3 Flow of NP currents according to the voltage level: **a** $3V_{dc}/4$; **b** $V_{dc}/2$; **c** $V_{dc}/4$

$$\begin{aligned}
\Delta V_{C1} &= (0.75i_{N1x} + 0.5i_{N2x} + 0.25i_{N3x}) \cdot \frac{T_s}{C}, \\
\Delta V_{C2} &= (-0.25i_{N1x} + 0.5i_{N2x} + 0.25i_{N3x}) \cdot \frac{T_s}{C}, \\
\Delta V_{C3} &= (-0.25i_{N1x} - 0.5i_{N2x} + 0.25i_{N3x}) \cdot \frac{T_s}{C}, \\
\Delta V_{C4} &= (-0.25i_{N1x} - 0.5i_{N2x} - 0.75i_{N3x}) \cdot \frac{T_s}{C},
\end{aligned} \tag{9}$$

where T_s is a sampling period. The fluctuation of capacitor voltages is affected by NP currents.

For balancing the DC-link capacitor voltages in the 5L-NPC inverter with the COPWM [27], three voltage relations are controlled by adjusting the duty ratios, so that $\Delta V_{c2} = \Delta V_{c3}$ and $(\Delta V_{c2} + \Delta V_{c3}) = (\Delta V_{c1} + \Delta V_{c4})$ can be achieved. In addition, $\Delta V_{c1} = \Delta V_{c4}$ can be obtained by injecting the zero-sequence voltage (ZSV), which is complex to implement. In this work, however, the balancing algorithm is simplified by controlling equally the deviations of the two adjacent capacitor voltages ($\Delta V_{c1} = \Delta V_{c2}$, $\Delta V_{c2} = \Delta V_{c3}$ and $\Delta V_{c3} = \Delta V_{c4}$) without the injection of ZSV. The difference of voltage deviation in the two adjacent DC-link capacitors is expressed by

$$\Delta V_{C(n+1)} - \Delta V_{C(n)} = -i_{N(n)x} \cdot \frac{T_s}{C} = (d_{x(n)} - d_{x(n+1)}) \cdot i_{\text{ox}} \cdot \frac{T_s}{C}, \tag{10}$$

where n means the device number, which is ranged from 1 to 3.

In (10), parameters T_s and C are constant values. So, capacitor voltage can be regulated only by adjusting the duty ratios $d_{x(n+1)}$ and $d_{x(n)}$ depending on the polarity of the output current i_{ox}. If the polarity of the output current is positive and $\Delta V_{c(n+1)} > \Delta V_{c(n)}$, the capacitor voltages $V_{c(n)}$ and $V_{c(n+1)}$ need to be charged and discharged, respectively. Accordingly, the variance of duty ratio $\Delta d_{ad(n)}$ is added to $d_{x(n+1)}$ and subtracted from $d_{x(n)}$. Since the variance of total duty ratio needs to be zero to avoid the deviation in the average output voltage, both the amounts of the increased duty ratio and the decreased one should be equal.

Let's consider that there is an imbalance condition between V_{c2} and V_{c3}, where it is assumed that V_{c2} is higher than V_{c3}. The difference between two voltages is calculated as

$$\Delta V_{C3} - \Delta V_{C2} = i_{N2x} \cdot \frac{T_s}{C} = (d_{x3} - d_{x2}) \cdot i_{\text{ox}} \cdot \frac{T_s}{C} \tag{11}$$

and, if the polarity of i_{ox} is positive, d_{x2} needs to be increased and d_{x3} to be decreased. Then, the adjusted amount of duty ratios is expressed as

$$\Delta d_{x2}^{(2)} = +\Delta d_{\text{ad2}}, \tag{12}$$

$$\Delta d_{x3}^{(2)} = -\Delta d_{\text{ad2}}. \tag{13}$$

Table 3 Adjusted amount of duty ratio for balancing control

For between V_{c1} and V_{c2}				
i_{ox}	$\Delta d_{x1}^{(1)}$	$\Delta d_{x2}^{(1)}$	$\Delta d_{x3}^{(1)}$	$\Delta d_{x4}^{(1)}$
$i_{ox} > 0$	Δd_{ad1}	$-\Delta d_{ad1}$	0	0
$i_{ox} < 0$	$-\Delta d_{ad1}$	Δd_{ad1}	0	0
For between V_{c2} and V_{c3}				
i_{ox}	$\Delta d_{x1}^{(2)}$	$\Delta d_{x2}^{(2)}$	$\Delta d_{x3}^{(2)}$	$\Delta d_{x4}^{(2)}$
$i_{ox} > 0$	0	Δd_{ad2}	$-\Delta d_{ad2}$	0
$i_{ox} < 0$	0	$-\Delta d_{ad2}$	Δd_{ad2}	0
For between V_{c3} and V_{c4}				
i_{ox}	$\Delta d_{x1}^{(3)}$	$\Delta d_{x2}^{(3)}$	$\Delta d_{x3}^{(3)}$	$\Delta d_{x4}^{(3)}$
$i_{ox} > 0$	0	0	Δd_{ad3}	$-\Delta d_{ad3}$
$i_{ox} < 0$	0	0	$-\Delta d_{ad3}$	Δd_{ad3}

Since the increment and decrement in duty ratios are equal, there is no change in the total duty ratio.

Next, it is necessary to control the difference between the sum of the outer capacitor voltages and that of the inner capacitor voltages, which is the same process as the aforementioned example. The adjustment of duty ratio for balancing control is summarized in Table 3 and the control block diagram is shown in Fig. 4. The adjustments (Δd_{ad1}, Δd_{ad2}) of duty ratio are performed by PI controllers. The letter "sgn" indicates the *signum* function to determine the output current polarity.

$$\text{sgn}(i_{\text{ox}}) = \begin{cases} 1 & i_{\text{ox}} \geq 0 \\ -1 & i_{\text{ox}} < 0 \end{cases}. \tag{14}$$

Finally, the adjusted amounts of duty ratio are added to the original duty ratio. So, the resultant duty ratio is given by

$$d'_{xn} = d_{xn} + \Delta d_{xn}^{(1)} + \Delta d_{xn}^{(2)} + \Delta d_{xn}^{(3)}. \tag{15}$$

4 Evaluation of THD of output voltage and cost

In this section, the THD of output voltage is analyzed in the cases with and without the auxiliary circuit and the cost evaluation is performed for a 1-MW/6.6-kV system. The system parameters are listed in Table 4.

The comparison of THDs of the line-to-line voltage between the LSPWM with the ABC and the COPWM without the ABC is shown in Fig. 5. At the low modulation MIs, the THD of line-to-line voltage in both cases are similar. At the medium and high MIs, the THD in the COPWM case is worse since the bent carriers are used for the modulation process.

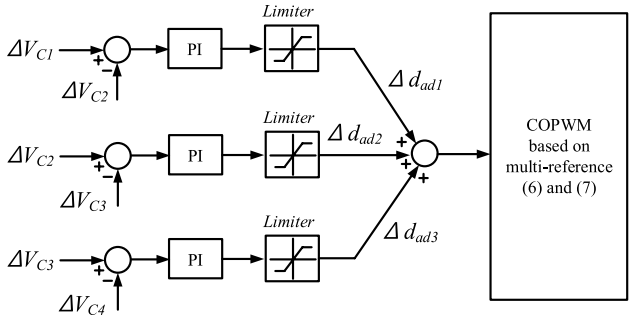

Fig. 4 Block diagram of DC-link capacitor voltage balancing control

However, harmonic components of output current are simply filtered by inductive loads. So, THD of output current is enough low [26–28].

The auxiliary balancing circuit requires the additional devices, which are two active switches, one diode, and two inductors. The voltage rating of additional devices is high, which is known from (1) and (2). To operate the ABC, it is required that the active switches should be able to withstand the half of the DC-link voltage and that the diodes do the full DC-link voltage. The auxiliary inductor is designed as [29]:

$$L_{\text{aux}} = \frac{V_{\text{dc}}/4}{\overline{I_{\text{aux}}} \cdot x\%} \cdot \frac{d_{\max}}{f_{\text{car}}}, \tag{16}$$

where $\overline{I_{\text{aux}}}$ is the average current of inductor. The inductance is determined depending on the allowable range of current ripple (x %) and maximum duty ratio $d_{\max}$ of the additional switches.

For the 1-MW/6.6-kV 5L-HT inverter, FF450R33T3E3 (3300 V/450A) model and DD500S65K3 (6500 V/500A) are selected for dual IGBT switches [30] and dual diode module [31] and C44UOGT7110M52K (900 V/1.1mF) are selected for the DC-link capacitors [32]. However, two diodes need to be connected in series to withstand the entire input voltage. For an auxiliary inductor, the allowable range of current ripples is set to 40%. The maximum duty ratio is limited to 0.8 and the average current from the simulation is obtained as about 200 A, but it is set to 400 A for the margin of safety. As a result, the auxiliary inductance is selected as 2.5 mH and the HCS-801 M is selected as the auxiliary inductors which has parameters of 0.8 mH and 350 A [33]. The estimation of cost and volume for the 5L-HT inverter and the auxiliary balancing circuit are listed in Table 5.

As listed in Table 5, the significant savings of cost and volume can be achieved by eliminating the auxiliary circuit. For example, for the 5L-HT inverter with 1-MW/6.6-kV system, the total cost and volume are saved by 27% and 52%.

Table 4 System parameters

Parameters	Value
Rated power	1 MW
Output voltage	6.6 kV
DC-link voltage	10 kV
DC-link capacitors	1100 μF
Fundamental frequency	60 Hz
Carrier frequency	3 kHz
Load PF	0.9

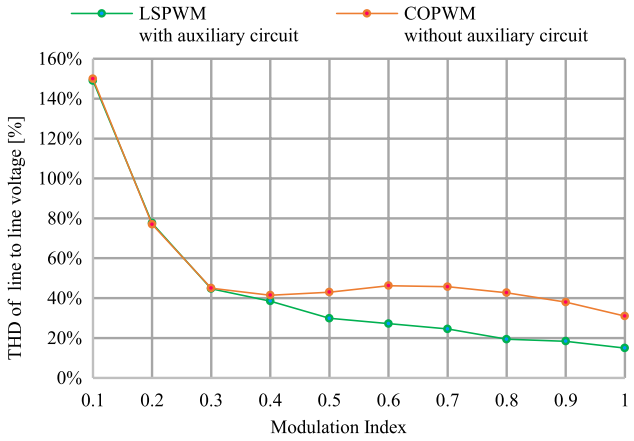

Fig. 5 THD comparison of line-to-line voltage

5 Simulation results

To verify the performance of the 5L-HT inverter, simulations have been conducted under diverse conditions. The simulation parameters are summarized in Table 4.

Figure 6 shows the simulation result at a MI for the 5L-HT inverter without the ABC. Figure 6a and b show the line-to-line voltage and output current, where their THDs are 32.2% and 1.18%, respectively. The ripple of the outer capacitor voltage is larger than that of the inner one since the utilization of the outer capacitor is dominant when generating the high-voltage levels. Figure 6c shows the outer capacitor voltages. Voltage ripples of both outer capacitors are 1.5%. The voltage fluctuation is within the allowable range of ± 10% of the reference value. Figure 6d shows the inner capacitor voltages. Both inner capacitor voltages are regulated with smaller ripples compared to those of the outer capacitor voltages. So, the four DC-link capacitor voltages are well controlled by adjusting the duty ratio without the auxiliary balancing circuit.

Table 5 Estimation of cost and volume for the 5L-HT inverter and auxiliary balancing circuit

Devices	Rated value	No	Price (US $)	Volume (mm^3)
For 5L-HT inverter				
IGBTs (FF450R33T3E3)	3.3 kV/450 A	21	31,206	18,345,600
Capacitor (C44UOGT7110M52K)	900 V/1.1mF	36	5688	1,616,953
Total			36,894	19,962,553
For Auxiliary Balancing circuit				
IGBTs (FF450R33T3E3)	3.3 kV/450 A	2	2972	1,747,200
Diodes (DD500S65K3)	6.5 kV/500 A	2	3580	1,747,200
Inductors (HCS-801 M)	0.8 mH/350 A	4	7000	17,947,444
Total			13,552	21,441,844

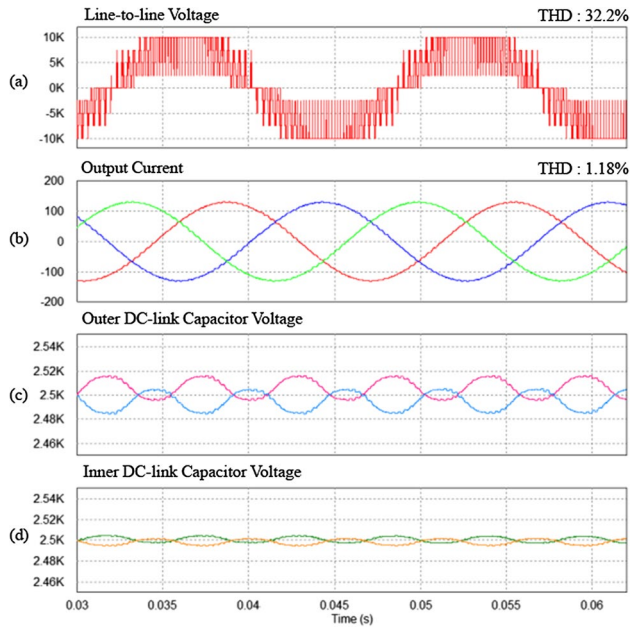

Fig. 6 Performance of 5L-HT inverter without auxiliary balancing circuit at a unity MI: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor (C_1, C_4) voltages; **d** inner DC-link capacitor (C_2, C_3) voltages

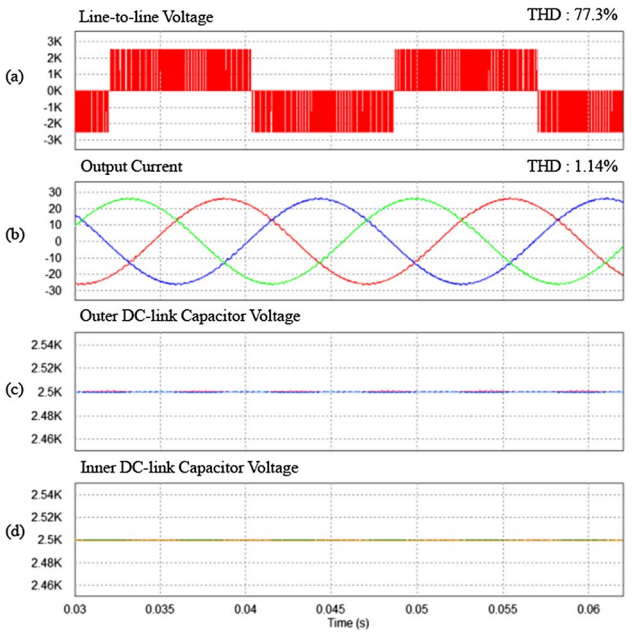

Fig. 7 Performance of 5L-HT inverter without auxiliary balancing circuit at MI = 0.2: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor (C_1, C_4) voltages; **d** inner DC-link capacitor (C_2, C_3) voltages

Figure 7 shows the simulation result at the low MI (MI = 0.2). The THD of line-to-line voltage and output current is 77% and 1.14%, respectively. The THD value is similar to that of LSPWM with the ABC. In the low modulation index region, the voltage of the four DC-link capacitors is still well regulated, and the voltage ripple is low.

Figure 8 shows the simulation result at the variable modulation index, where the amplitude modulation index and frequency modulation index vary equally ($m_a = m_f = MI$). The MI is increased by 0.2 from 0.1 to 0.9 every 0.1 s. The voltages of the four DC-link capacitors are well controlled while the amplitude and frequency of reference voltage are changed. The maximum ripple of the capacitor voltage is similar to the ripple at a unity MI. For the variable-voltage and variable-frequency operation, the balancing control ability allows the reasonable range of the voltage ripple (± 10% of the reference value). Figure 9 shows the simulation result at the load transient condition. At $t = 0.05$, the load is increased from 50 to 100% of rated power in a step. The proposed control scheme for the 5L-HT inverter is effective against the load variation. The outer capacitor voltage is controlled with the 1.8% of voltage ripple. The inner capacitor voltage ripple is 0.5%, approximately. Note that the voltage fluctuation in aforementioned conditions is still within the allowable range, which is ± 10% of the reference value.

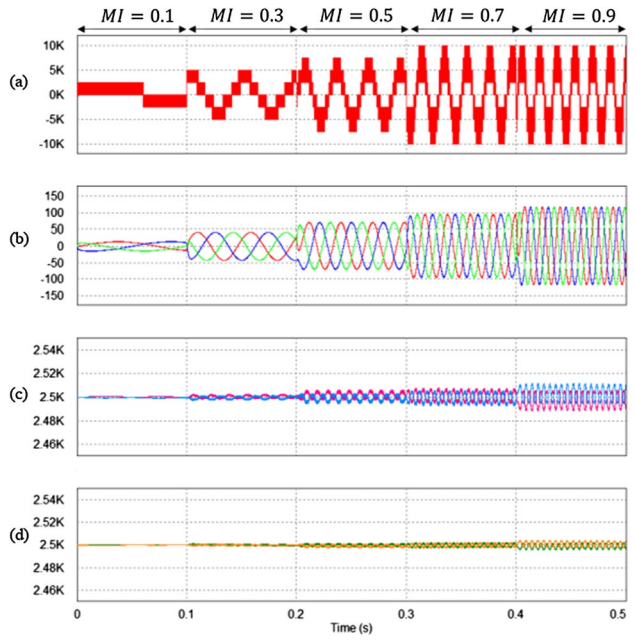

Fig. 8 Performance of 5L-HT inverter at the variable modulation index: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor (C_1, C_4) voltages; **d** inner DC-link capacitor (C_2, C_3) voltages

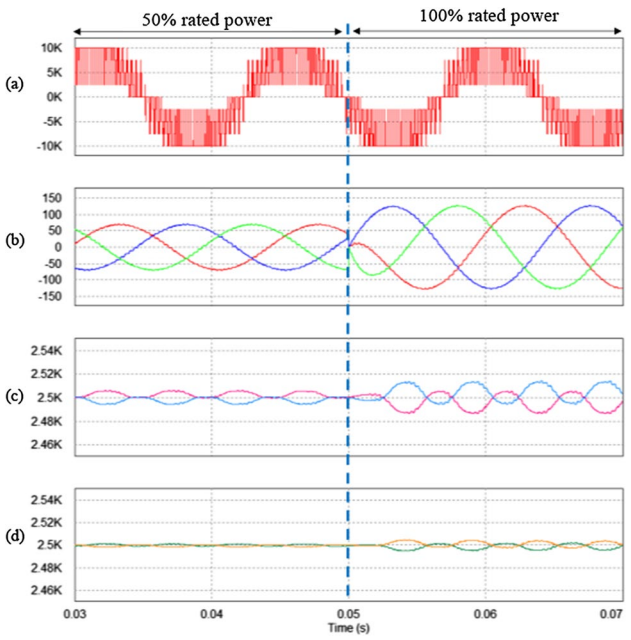

Fig. 9 Performance of 5L-HT inverter at load transient condition: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor (C_1, C_4) voltages; **d** inner DC-link capacitor (C_2, C_3) voltages

6 Experimental results

To verify the effectiveness of the capacitor voltage balancing control without the auxiliary balancing circuit, the prototype of the 5L-HT inverter has been built. A control board with DSP (TMS320F28335) and FPGA (Xilinx XC3S400) is used. The down-scaled parameters for the experiment are listed in Table 6. A photo of the hardware set-up is shown in Fig. 10.

Figure 11 shows the experimental performance at a unity MI. The line-to-line voltage and output current is illustrated in Fig. 11a and b, respectively, which show similarities to the simulation ones. The outer and inner capacitor voltages are shown in Fig. 11c and d, respectively. Each of the split DC-link capacitor voltages is well controlled at the reference value. The voltages are regulated by adjusting the duty ratio from the PI controllers. The voltage ripples of the outer and inner capacitors are around 4.8% and 4%, respectively. Figure 12 shows the experimental performance at the low MI (MI = 0.2). The line-to-line voltage and output current is shown in Fig. 12a and b, respectively, which are similar to the simulation results. At low MI, the four capacitor voltages are regulated at the reference value (50 V). The voltage ripple of four capacitors is lower than that of at a unity MI.

Figures 13 and 14 show the effectiveness of the balancing control method for the 5L-HT inverter at transient-state conditions. The experiments are conducted under the similar

Table 6 System parameters for experiment

Parameters	Value
DC-link voltage	200 V
DC-link capacitors	2200 μF
Fundamental frequency	60 Hz
Carrier frequency	3 kHz
RL-load	25 Ω, 12.5 mH

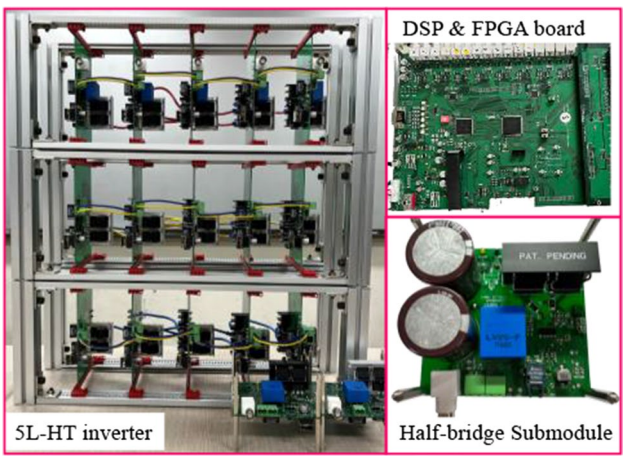

Fig. 10 Experiment hardware of the 5L-HT inverter

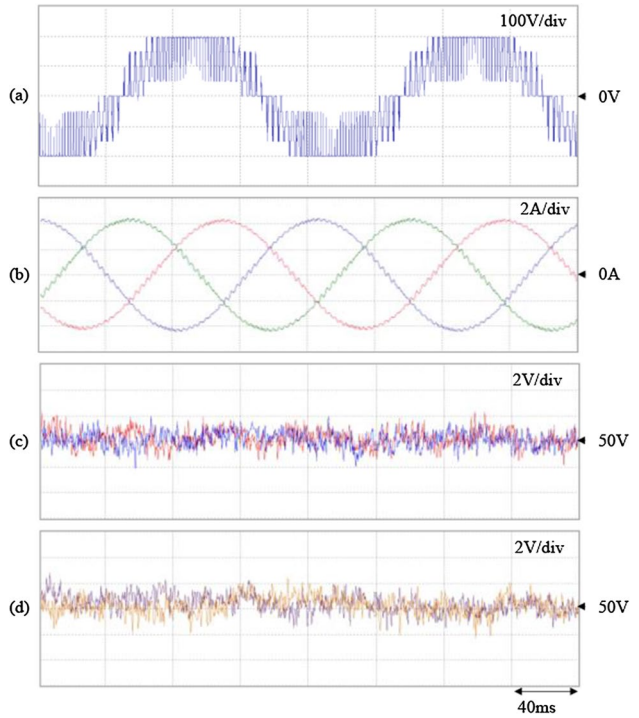

Fig. 11 Experimental result without auxiliary balancing circuit at a unity MI: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor voltages; **d** inner DC-link capacitor voltages

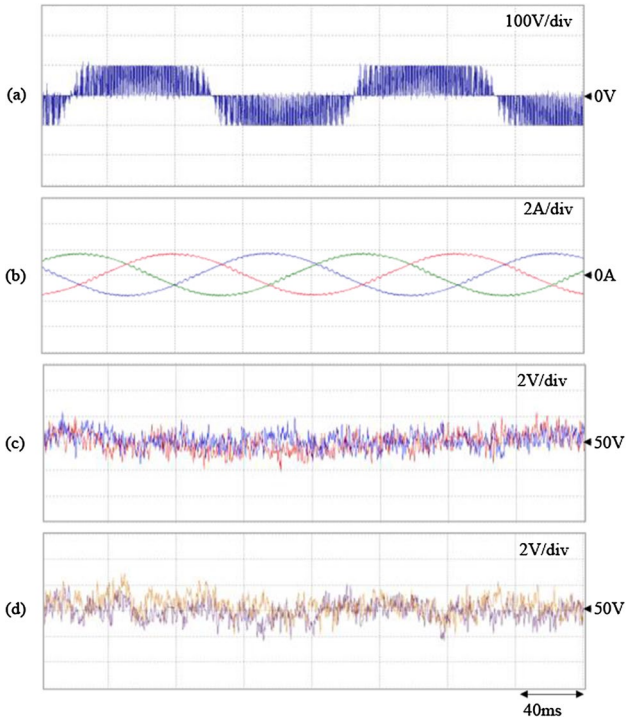

Fig. 12 Experimental result without auxiliary balancing circuit at MI = 0.2: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor voltages; **d** inner DC-link capacitor voltages

conditions with those of simulation. The outer and inner capacitor voltages are shown in Fig. 13c and d, respectively. The peak-to-peak ripple of the voltages is less than 10% of the reference value, which is lower than the allowable range. In Fig. 14, the load resistor is changed from 50 Ω to 25 Ω in a step, during which the four DC-link capacitor voltages are well controlled at the reference voltage 50 V. Also, the ripple of four voltages does not exceed 10% of the reference voltage. The balancing control method without the ABC for the 5L-HT inverter is still effective under the various operating conditions.

7 Conclusions

In this paper, the balancing control scheme of DC-link capacitor voltages for 5L-HT inverter has been proposed. The existing 5L-HT inverter requires an auxiliary balancing circuit which is bulky and expensive to control the DC-link capacitor voltage. To eliminate this circuit, the recent COPWM has been utilized. With this control algorithm, the balanced DC-link capacitor voltages have been achieved by adjusting the duty ratio of switches to control NP currents. As a result, the THD of the output voltage becomes rather higher at the medium and high modulation indices. Although

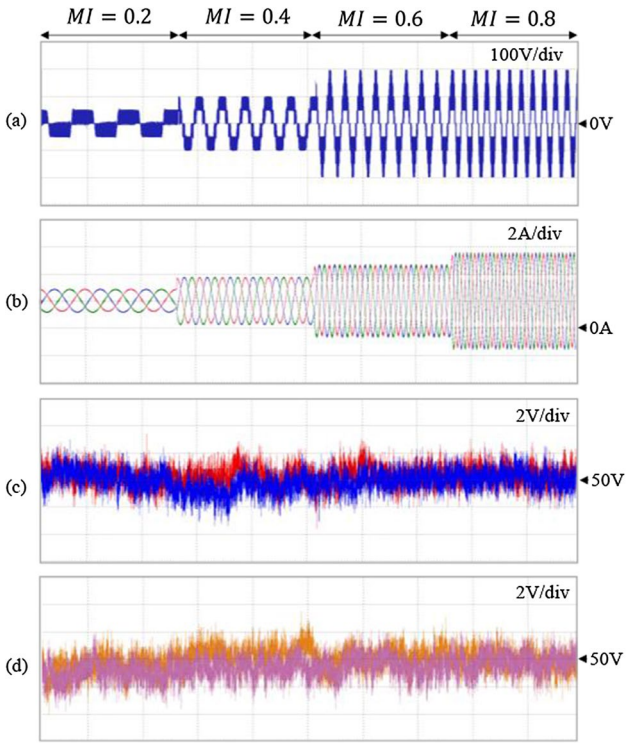

Fig. 13 Experiment result at the variable modulation index: **a** line-to-line voltage: **b** output current; **c** outer DC-link capacitor voltage; **d** inner DC-link capacitor voltage

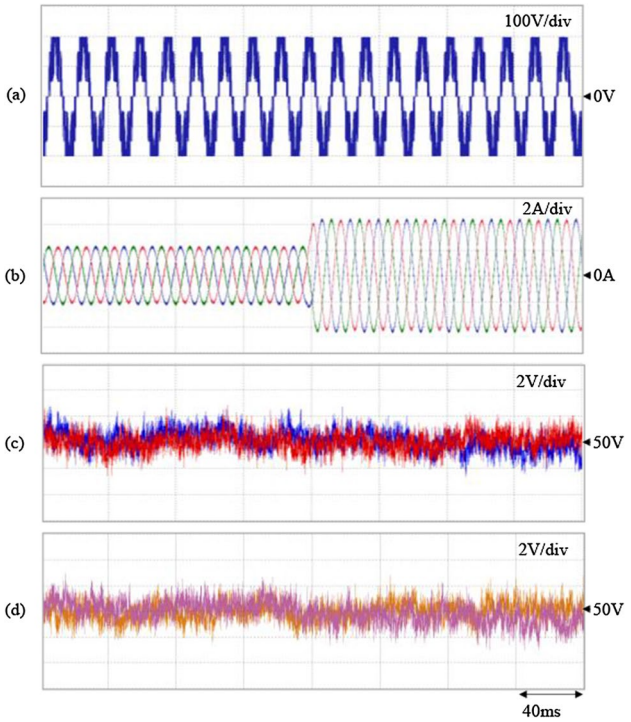

Fig. 14 Experiment result at the load transient condition: **a** line-to-line voltage; **b** output currents; **c** outer DC-link capacitor voltages; **d** inner DC-link capacitor voltages

the THD of voltage is increased, that of load currents is quite a low since the high frequency components of voltage can be easily suppressed by load inductance. Furthermore, the total cost and volume for the 1-MW/6.6-kV system can be saved by 27% and 52%, respectively. The effectiveness of the balancing control algorithm for the 5L-HT inverter has been verified through the simulation and experimental results.

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Data availability The datasets generated during and/or analysed during current study are not publicaly available but may be available from the corresponding author if the request is reasonable.

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