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ORIGINAL ARTICLE

Capacitor commutation type DC circuit breaker with fault character discrimination capability

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Abstract
Flexible direct current (DC) grids face a serious challenge in terms of rapidly isolating DC faults. A DC circuit breaker is an effective solution for DC fault isolation. To improve the fault-isolation and reclosing capability of flexible DC systems, a new high voltage direct current (HVDC) circuit breaker topology with adaptive reclosing capability is proposed in this paper. The topology of the circuit breaker is a T-shaped structure, which has the ability to break the current in both directions and effectively reduce the cost of components. Meanwhile, after the fault is cleared, the circuit breaker is controlled to inject a voltage signal into the line. Based on this, to prevent the circuit breaker reclosing in the event of a permanent fault from having an impact on the system, a method for fault identification based on Euclidean distance that uses the voltage signal to identify the fault properties is proposed. Finally, the performance of the circuit breaker is simulated and verified by PSCAD/EMTDC simulation software, and compared with the typical existing circuit breakers to verify the effectiveness of the circuit breaker and reclosing scheme.

Keywords DC grid · Hybrid DC circuit breaker · Topology · Adaptive closing · Short circuit fault

1 Introduction

A flexible DC grid has the superior qualities of high reliability and independent control of the active and reactive powers [1], which is of great significance to the development of renewable energy grid-connected technologies. However, its low damping and quick fault development make rapid fault isolation one of the main technical bottlenecks restricting its development [2, 3]. Modular multilevel converters (MMCs) based on full-bridge units can block fault currents, and DC/DC power converters [4] with fault self-clearing capability can clear faults for multi-voltage level systems. However, both methods result in short-term outages of entire multi-terminal direct current (MTDC) grids, which is unacceptable for large-scale power grids. Clearing line faults with a DC circuit breaker (DCCB) is the most promising type of method for fault clearing in DC systems because it isolates the fault while guaranteeing the normal power transmission of the non-faulty lines of the system [5].

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Capacitor-commutated DCCBs are based on traditional DC circuit breakers [6], where the insulated gate bipolar transistors (IGBTs) of the transfer branch are replaced by series capacitors and diodes [7, 8]. A novel hybrid circuit breaker was proposed in [8] that isolates line faults by generating reverse current through capacitive and inductive oscillations. However, the control of the circuit breaker is complicated. In [9], a capacitor-commutated DCCB with limited current functionality was proposed, which adopted a bridge-type capacitor-commutation unit to buffer the voltage of the device. However, this method requires a large number of IGBTs in series and parallel, which greatly increased the cost of the DCCB. In [10], a solid-state DC circuit breaker was proposed, which uses a high-temperature superconducting current limiter to limit the current to reduce the cost of the circuit breaker.

In addition, flexible DC transmission lines are mostly overhead lines, and the probability of instantaneous faults is high on overhead lines. Using a DC circuit breaker to identify the fault nature is an economic and promising solution [11–15]. A pre-charged capacitor circuit breaker was proposed in [11]. However, a reclosing strategy is not mentioned. A circuit breaker adaptive reclosing sequence strategy was proposed in [12]. However, it is still a non-selective

reclosing method. A DC solid-state circuit breaker with soft reclosing capability was proposed in [13]. However, the scheme does not consider the influence of discharge current amplitude on the system when identifying the fault nature. A soft reclosing scheme for circuit breakers, based on adding mechanical switches and resistors, was proposed in [14]. However, this method makes the IGBTs in the main circuit breaker act frequently, which is not conducive to the service life of the circuit breaker. A method for identifying fault nature through the partial sub-modules (SMs) of the DCCB was proposed in [15]. However, this scheme is susceptible to noise interference. A method for judging fault properties by injecting the characteristic signals of the half-bridge MMC and the circuit breaker was proposed in [16]. However, this method requires a high sampling frequency and is easily affected by fault impedance.

In summary, a capacitor-commutated DC circuit breaker with fault character discrimination capability (FDC-CCCB) is presented in this paper. The circuit breaker structure has bidirectional conduction and current-limiting functionality, which can greatly reduce the cost of the device. The characteristic where the capacitor voltage in the capacitor circuit breaker needs to be released through the energy release branch is used in this paper. The capacitor in the circuit breaker is controlled to discharge to the fault line. Then the nature of the fault is judged to prevent the permanent fault from having a secondary effect on the system.

2 FDA-CCCB principal and analysis

2.1 FDA-CCCB configuration

The structure of the FDA-CCCB is shown in Fig. 1. It is mainly composed of four parts: the main branch, the transfer branch, the breaking branch, and the reclosing branch.

1) When the system is under the normal operation condition, current flows through the main branch, which consists of mechanical switches $K_{1,2}$ and a diode bridge module. T_1 is a transfer switch, which is composed of a small number of IGBTs in series, and D_1-D_4 form a diode bridge.
2) The transfer branch is composed of diversion diodes ($D_{5,6}$) and current-limiting inductors ($L_{1,2}$). $L_{1,2}$ are used to limit the increase rate of the fault current. After T_1 is disconnected, the current is transferred to the breaking branch.
3) The breaking branch is composed of a mechanical switch K and breaking sub-modules (BSMs). When the system is under normal operation, K is in the disconnected state to prevent the open branch of the circuit breaker from being affected by the high voltage. Each BSM consists of three branches: the IGBT branch B_1, the capacitor branch B_2, and the arrester branch B_3. The specific structure is shown in RSM_N: $T_2 \sim T_n$ ($n=2,3\ldots$) are IGBTs, T_{CN} (where N is the number of BSMs, and $N=1,2\ldots$) are thyristors, C_N is a capacitor, R_{3N} is a bleeder resistor, and a metal-oxide varistor (MOV) is an arrester. The breaking branch is modularized to avoid a large number of IGBTs in B_2 to withstand the capacitor charging voltage in series, and to reduce the equipment withstand voltage capability requirements. T_{CN} has the functions of blocking the normal load current and preventing the capacitor from charging when the system is running stably. C_N is configured with an energy release branch, where K_{3N} is a mechanical switch and R_{3N} is an energy bleeder resistor. The energy release branch is utilized to release the voltage in the capacitor after the fault is cleared to prevent T_{CN} from being continuously subjected to the reverse voltage of the capacitor, which is not conducive to the restarting of the circuit breaker.
4) The reclosing branch is composed of a thyristor T_{re}. After the circuit breaker is opened, C_N is controlled to inject a voltage signal into the line through the reclosing branch. Then the nature of the fault is judged according to what is between the line voltage signal under the instantaneous fault and the permanent fault.

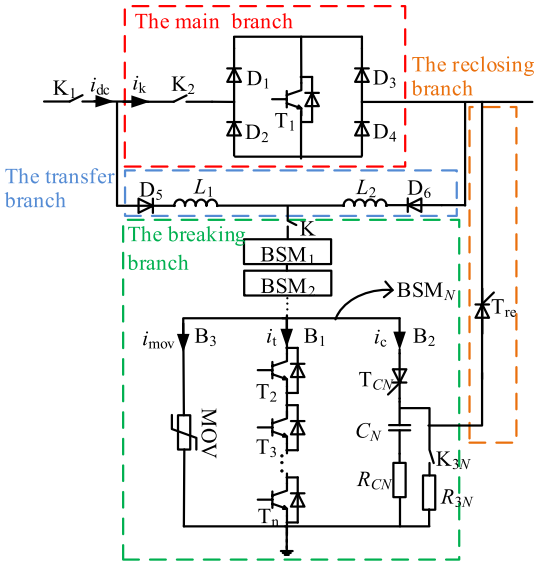

Fig. 1 Typical FDA-CCCB circuit

2.2 Working principle and theoretical analysis

Taking one breaking sub-module as an example, the current conduction paths at each stage based on Fig. 1 are shown in Fig. 2. Assuming that a short-circuit fault occurs

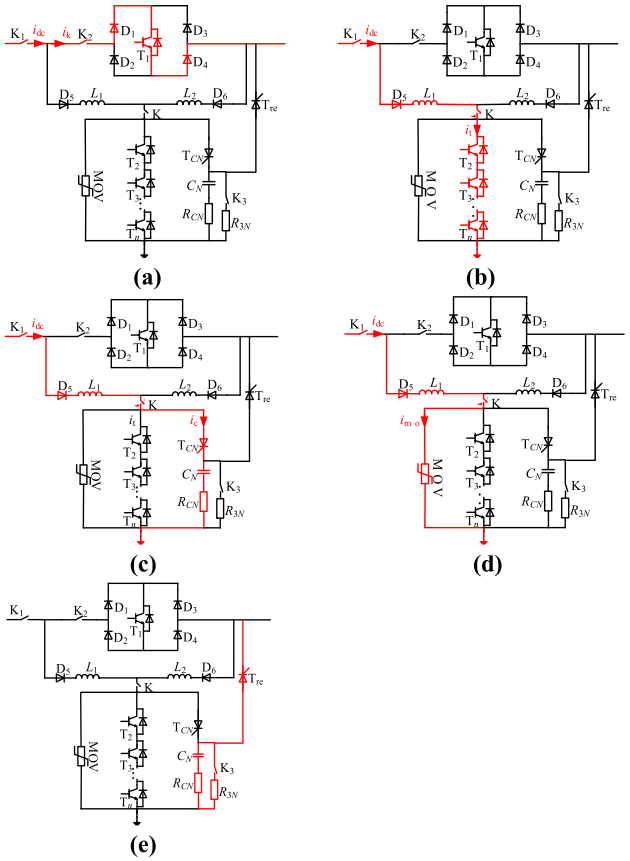

Fig. 2 Current conduction path of each stage of the FDA-CCCB: **a** stage a; **b** stage b; **c** stage c; **d** stage d; **e** stage e

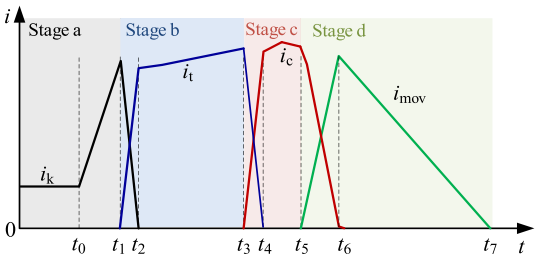

Fig. 3 Current waveform diagram of a DC circuit breaker in each stage of the fault removal process

at the right end of the circuit breaker at t_0, current waveforms of the circuit breaker in each stage are shown in Fig. 3.

Stage a ($t_0 \sim t_1$). The fault current rises at t_0. However, the circuit breaker does not receive the action signal, and the current flows through K_1 and the main branch.

Stage b ($t_1 \sim t_3$). The circuit breaker receives the action signal, $T_2 \sim T_n$ are turned on, and T_1 is turned off. The current is transferred to the B_1 branch through $D_{5,6}$ and $L_{1,2}$.

The expression for stage b is as follows:

$$U_{dc} = L' \frac{di_{dc}}{dt} + i_{dc} R_t \tag{1}$$

$$L' = L_{dc} + L_1 \tag{2}$$

where U_{dc} represents the DC voltage source voltage, R_t represents the equivalent resistance of the B_1 branch IGBTs, L' represents the equivalent inductance in the fault circuit at stage b, and L_{dc} represents the line smoothing reactor.

After T_1 is disconnected, $i_{dc}(0) = i_{dc}(t_1)$. Thus,

$$i_{dc}(t) = \frac{U_{dc}}{R_t} + \left[i_{dc}(t_1) - \frac{U_{dc}}{R_t} \right] e^{-\frac{t}{\tau}} \tag{3}$$

The time constant is calculated by the following formula:

$$\tau = \frac{L'}{R_t} \tag{4}$$

During stage b, the fault current increasing rate is mainly determined by the value of the current-limiting inductance.

Stage c ($t_3 \sim t_5$). T_{CN} is turned on. Then $T_2 \sim T_n$ are turned off. The fault current is transferred from B_1 to B_2, and the capacitor C_N is rapidly charged. When the voltage of the breaking branch increases to the rated voltage of the system, the fault current begins to decrease.

The expression for the stage c is as follows:

$$L'C \frac{d^2 UC}{dt^2} + R_C C \frac{dU_C}{dt} + U_C = U\mathrm{dc} \tag{5}$$

$$i\mathrm{dc} = C \frac{dU_C}{dt} \tag{6}$$

where C represents the capacitance in the capacitor branch, and R_C represents the resistance in the capacitor branch. At this time, the initial current of the line and the initial voltage of the capacitor are as follows:

$$\begin{cases} i_{dc}(0_+) = i_{dc}(0_-) = i_{dc}(t_4) \\ U_C(0_+) = U_C(0_-) = 0 \end{cases} \tag{7}$$

This yields $u_c(t)$ and $i_{dc}(t)$ as follows:

$$u_C(t) = U_{dc} - \frac{I_{dc}(t_4)}{\omega C} e^{-\alpha t} \sin \omega t \tag{8}$$

$$i\mathrm{dc}(t) = \frac{I_{dc}(t_4)}{\omega} e^{-\alpha t} (\alpha \sin \omega t - \cos \omega t) \tag{9}$$

where

$$\begin{cases} \alpha = \dfrac{R_C}{2L'} \\ \omega = \sqrt{\omega_0^2 - \alpha^2} \\ \omega_0 = \dfrac{1}{\sqrt{L'C}} \end{cases} \tag{10}$$

It can be known from (8)–(10) that the larger the value of C, the longer the capacitor charging time, and the longer the time for the current to transfer from the capacitor branch to the arrester branch. Although R_C increases the charging time of the capacitor, it also increases the voltage of the capacitor branch, which is conducive to the rapid operation of the arrester to absorb energy, shortens the fault clearing time, and reduces the energy absorption of the arrester and prolongs its service life.

Stage d (t_5~t_7). T_{CN} is turned off after being subjected to reverse voltage, the fault current is transferred to the arrester branch, the arrester absorbs the remaining energy in the circuit, and the fault current drops rapidly.

Stage e: After the circuit breaker is opened, the circuit experiences a deionization time of 200 ~300 ms, and then enters the stage of fault identification. T_{re} is turned on to discharge the bottom C_N of the sub-module capacitor to the line, while all K_{3N}s are turned off to release the energy in the capacitor.

When a permanent fault occurs on the line, the expression of this stage is as follows:

$$U_{CN}(t) = U_{CN}(t_6)e^{-\frac{t}{\tau_C}} \tag{11}$$

where:

$$\begin{cases} \tau_C = C_N\left(R_C + \dfrac{R_{3N}R}{R_{3N}+R}\right) \\ R = R_g + R_l \\ R_l = xr_0 \end{cases} \tag{12}$$

where R_g represents the fault impedance, x represents the distance from the measurement point to the fault point, and r_0 represents the line resistance per unit length. The capacitor discharge time is related to the values of C_N, R_C, R_{3N}, and R_g.

Taking the moment when the injected voltage signal is first detected as t_0', and Δt_s represents the sampling time, the voltage signal detected during (t_0', $t_0' + \Delta t_s$) is the electrical quantity required to identify the nature of the fault. The fault is judged by comparing the difference between the line voltage signal under the instantaneous fault and the permanent fault in the (t_0', $t_0' + \Delta t_s$). When it is determined that the line has an instantaneous fault, the circuit breaker receives the reclosing command, and K_2, K_1, and T_1 of the circuit breaker are closed at both ends of the line in turn, and the system gradually returns to normal operation.

3 Parameters design

Circuit breakers in a two-terminal flexible DC system with a rated voltage of 320 kV and a rated current of 2 kA are discussed and analyzed in this section. The circuit breaker parameters proposed in this paper are designed as follows: the fault current amplitude is limited to within 8kA, the fault detection is 2 ms, and the fault clearing time is less than 6 ms.

3.1 Parameter design of the current-limiting inductor

It can be seen from (3) that the increase rate of the fault current is mainly related to the value of L_1、 L_2. In addition, when the current is transferred to the breaking branch, the voltage of T_1 is the voltage across the current-limiting inductor. In this paper, four groups of different inductance values are selected, and the changes of the fault current and voltage across T_1 with the value of L_1 are shown in Fig. 4.

It can be seen that the larger the current-limiting inductance, the smaller the secondary increase rate of the fault current, and the lower the requirement for the breaking capacity of the circuit breaker. However, this increases the voltage of T_1, which is consistent with the above analysis results. Considering the three aspects of fault current amplitude and

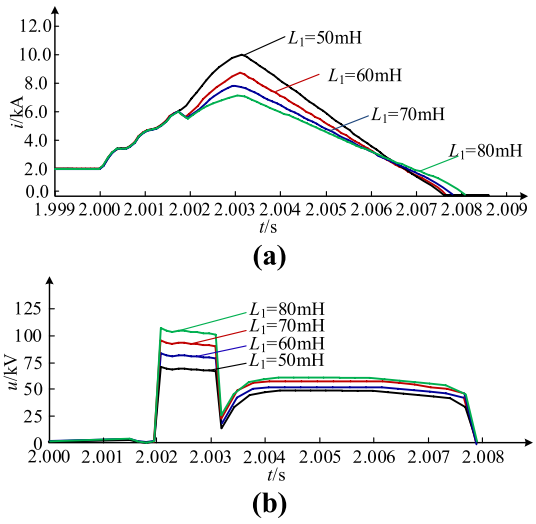

Fig. 4 Voltage and current waveforms under different inductance values: **a** waveforms of the fault current as a function of the inductance; **b** waveforms of the voltage across T1 as a function of the inductance

rate of increase, and the IGBTs withstand voltage, combined with the current-limiting requirements of the current actual project, a 70 mH current-limiting inductor is used.

3.2 Parameter design of the capacitor

After the fault current is transferred to B_2, the capacitor is charged and its voltage increases. In this stage, K_2 and T_1 share the voltage of the capacitor branch and L_1. The voltage of K_2 is U_k, and the maximum voltage that T_1 can withstand is U_{T1max}. To ensure the safe operation of the circuit breaker, the voltage across it should be lower than $U_k + U_{T1max}$, which can be expressed as:

$$u_C(t) + u_{R_C}(t) + u_{L1}(t) < U_k + U_{T1\,max}, t_3 < t < t_6 \tag{13}$$

According to (8) and (13):

$$U_{dc} - \frac{I_{dc}(t_4)}{\omega C} e^{-\alpha t} \sin\omega t + R_C i_{dc}(t) + L_1 \frac{didc}{dt} < U_k + U_{T1\,max}, t_3 < t < t_6 \tag{14}$$

The range of the total breaking branch capacitance C value can be calculated by (14). Then the capacitance C_N of each breaking sub-module is as follows:

$$C_N = NC \tag{15}$$

where N represents the number of breaking submodules.

When C_N is controlled to inject a voltage signal into the line, if a single-pole grounding fault occurs on the line, coupling occurs between the faulty line and the sound line. If the amplitude of the injected voltage is too large, the normal operation of the sound line is affected, and the power electronic device is impacted. Accordingly, the amplitude of the injected voltage signal is generally $0.1\sim0.2U_{dcN}$ [17]. Namely, the capacitor voltage in a single breaking sub-module should be less than $0.1\sim0.2U_{dcN}$.

The action time of the arrester depends on the capacitor branch voltage, and the voltage of C_N should meet the arrester action voltage as soon as possible. When the capacitor voltage is charged to the rated voltage of the system, the inductor voltage is zero, and the current begins to decrease. According to the time limit of the circuit breaker clearing fault, it should be less than 1 ms from the current drop to the time when arrester is put into operation. The appropriate capacitor value is selected according to the above constraints and the specific parameters of the system, and the value of C_N is taken as 35 μF.

3.3 Parameter design of the bleeder resistor

When the fault impedance is 0, the resistance of the discharge circuit of C_N is $R_C + R_{3N}$. When compared with R_{3N}, the value of R_C is exceedingly small. Thus, this study mainly designs the value of R_{3N}. When a fault occurs in the line, the capacitor is mainly discharged through the energy release branch (K_{3N} and R_{3N}). According to the process analysis of the circuit breaker fault identification, the capacitor discharge time should be greater than the sampling time Δt_s. In addition, to limit the C_N discharge current peak value, R_{3N} should not be too small. However, if R_{3N} is too large, it increases the discharge time of the capacitor, which is not conducive to the rapid recovery of the circuit breaker. The capacitor discharge time is usually $3\sim5RC$. Thus,

$$\Delta t_s < 5R_{3N}C_N < t_{rmax} \tag{16}$$

where t_{rmax} represents the longest recovery time of the circuit breaker, which is 10 ms. When combined with the value of C_N, R_{3N} should be less than 57 Ω. Based on the above analysis, the value of R_{3N} is 20 Ω.

4 FDA-CCCB-based fault property discrimination method

When C_N is controlled to inject a voltage signal into the line, K_1, K_2, and K are invariably disconnected, and the converter station is isolated from the fault point. Assume the fault occurs at point F. A schematic diagram of the voltage signal injected into the fault line is shown in Fig. 5.

4.1 Fault traveling wave characteristic analysis

As shown in Fig. 5, assuming that the voltage signal V_C is injected into the fault line and propagates from M to N, according to the principle of traveling wave transmission, refraction and reflection occur at the sudden change of the line wave impedance.

The refractive coefficient α and the reflection coefficient β of the impedance mutation point can be expressed as:

$$\alpha = \frac{2Z_2}{Z_1 + Z_2} \tag{17}$$

$$\beta = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{18}$$

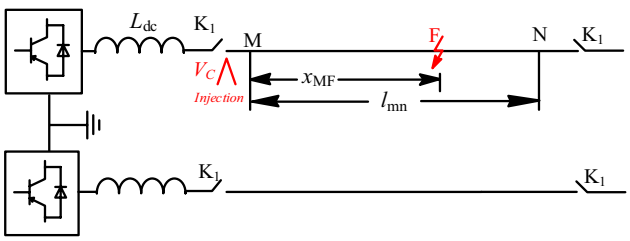

Fig. 5 Schematic diagram of signal injection

where Z_1 represents the line wave impedance, the wave impedance of the overhead line is 300 ~ 500Ω, and Z_2 represents the equivalent wave impedance of the reflection and refraction lines. In particular, when the line impedance sudden change is an open circuit, Z_2 is ∞, and the corresponding α and β are 2 and 1, respectively. Therefore, the refraction coefficients α_M and α_N and the reflection coefficients β_M and β_N at both ends of M and N are 2 and 1, respectively. The impedance mutation of the line is short-circuited, namely Z_2 is 0, and the corresponding α and β are 0 and -1, respectively.

A permanent fault occurs at F of the line. At t_0', C is controlled to inject a voltage signal with an amplitude of V_C into the line. According to the traveling wave transmission principle, it can be concluded that:

$$\begin{cases} V_{\mathrm{Fr}} = \alpha_{\mathrm{F}} V_C = \dfrac{2Z_2}{Z_2 + Z_1} V_C \\ V_{\mathrm{Ff}} = \beta_{\mathrm{F}} V_C = \dfrac{Z_2 - Z_1}{Z_2 + Z_1} V_C \end{cases} \tag{19}$$

where α_F and β_F represent the refractive coefficient and reflection coefficient of F, respectively. When a single-pole grounding fault occurs at F of the line, $Z_2 = Z_1 \| R_g$; when a pole-to-pole fault occurs at F, $Z_2 = Z_1 \| (R_g + Z_1/2)$. Therefore, $Z_2 < Z_1$, that is, $\beta_F < 0$.

At this time, the voltage at M can be expressed as:

$$u_{\mathrm{MF}}(t) = \begin{cases} u_{CN}(t) \;\; t_0 \le t < \frac{2x}{v}; \\ u_{CN}(t) + \beta_{\mathrm{F}} \alpha_{\mathrm{M}} V_C \mathrm{e}^{-2\gamma x_{\mathrm{MF}}} \;\; \frac{2x}{v} \le t < \frac{4x}{v}; \end{cases} \tag{20}$$

where γ represents the attenuation coefficient of the line, and x_{MF} represents the distance between M and F.

When the fault at F is an instantaneous fault, the voltage at M is:

$$u_{\mathrm{MF}}(t) = \begin{cases} u_{CN}(t) \;\; t_0 \le t < \frac{2l_{\mathrm{mn}}}{v}; \\ u_{CN}(t) + \beta_{\mathrm{N}} \alpha_{\mathrm{M}} V_C \mathrm{e}^{-2\gamma l_{\mathrm{mn}}} \;\; \frac{2l_{\mathrm{mn}}}{v} \le t < \frac{4l_{\mathrm{mn}}}{v}; \end{cases} \tag{21}$$

where $\beta_N = 1$, $\alpha_M = 2$.

Taking a single-pole metal ground fault at the midpoint of the line as an example, the propagation characteristics of the voltage signal in the line are shown in Fig. 6. It can be seen that when an instantaneous fault occurs in the line, the fault is cleared when the signal is injected. After the signal is injected, the first anti-travel wave measured from M is $2l_{mn}/v$, and the amplitude is larger than that of the injected voltage. When a permanent fault occurs in the line, the first voltage inverse traveling wave measured at point M is consistent with the above theoretical analysis.

The capacitors of the circuit breakers at both ends of the faulty line can be controlled to inject voltage signals. However, this scheme still has a weakness in terms of communication between the two ends. Therefore, in this paper, the capacitor of the circuit breaker on one side of the fault line is selected to inject the voltage signal, and the capacitor voltage of the circuit breaker on the other side can discharge through the energy release branch.

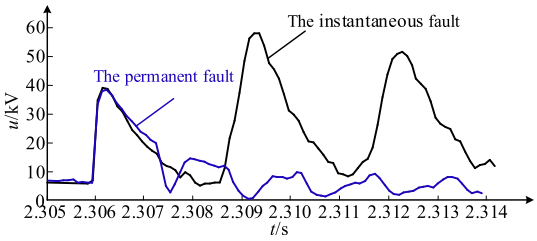

Fig. 6 Waveforms of the voltage propagation characteristics

4.2 Euclidean distance-based fault property discrimination method

After the capacitor voltage signal is injected into the line, for an instantaneous fault, the voltage measured at M is independent of the fault impedance and fault location. Meanwhile, the voltage measured at point M is significantly different from the instantaneous fault voltage when a permanent fault occurs. In this paper, a voltage waveform at point M during an instantaneous fault is used as the reference voltage, and the Euclidean distance (ED) is used to judge whether the fault has been cleared or not. Let $A = \{a_1, \ldots a_n\}$ and $B = \{a_1, \ldots a_n\}$ be two finite sets, and the ED between the point a_k in the set A and the point b_k in the set B is as follows:

$$D(a_k, b_k) = \frac{1}{n} \sqrt{\sum_{k=1}^{n} (a_k - b_k)^2} \tag{22}$$

The degree of similarity between the two sets of A and B can be expressed by the ED. The smaller $D(a_k, b_k)$ is, the higher the similarity between the two sets of A and B. When an instantaneous fault occurs in the line, taking the voltage waveform in Fig. 6a as the reference voltage wave, the voltage waveform measured at M is the measured voltage wave, and the difference between the measured wave and the reference wave is described by $D(a_k, b_k)$ in ED. An appropriate value of $D(a_k, b_k)$ is set as the threshold to distinguish the nature of the fault. According to (20) and (21), when a fault occurs at the end of the line and the fault impedance is larger, the permanent fault voltage waveform is closer to the instantaneous fault voltage waveform. Thus, to obtain the minimum value of $D(a_k, b_k)$. It is necessary to set $D(a_k, b_k)_{set}$ as:

$$D(a_k, b_k)_{set}=k_d D(a_k, b_k)_{min} \quad (23)$$

where k_d represents the reliability coefficient (0 ~ 1), which is taken as 0.7. $D(a_k, b_k)_{min}$ is the minimum ED between the measured voltage waveform and the reference waveform at M under the permanent fault.

After the voltage traveling wave is injected into the line at time t_0', the voltage traveling wave is induced at M. For the voltage wave at M, take t_0' as the starting point and take n-1 sampling points to form a sampling window of length n. The time length of the sampling window should be greater than twice the time it takes for the voltage traveling wave to propagate throughout the entire line. Therefore, the sampling window time length Δt_s is:

$$\Delta t_s = (2 + k_s) l_{mn}/v \quad (24)$$

where k_s = 0.5.

To sum up, a flow chart of the fault identification scheme is shown in Fig. 7.

5 Simulation analyses

A ± 320 kV double-ended flexible DC transmission system was built in the PSCAD/EMTDC platform as shown in Fig. 8. The FDA-CCCB and system simulation parameters are shown in Table 1 [13].

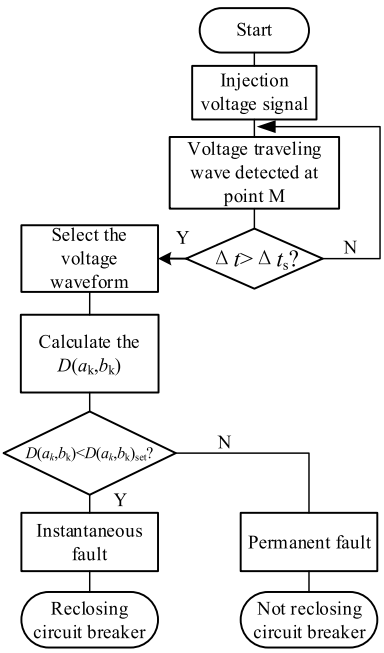

Fig. 7 Flow chart of the fault nature judgment algorithm

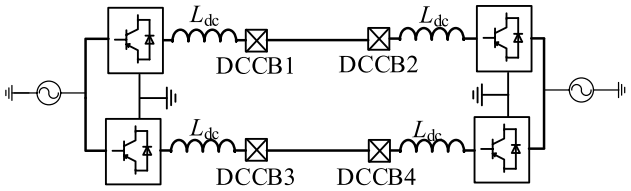

Fig. 8 Simulation diagram of the double-ended flexible DC transmission system

5.1 Fault isolation process simulation verification

The simulated short-circuit fault occurs at 2 s and the circuit breaker receives the action command in 2.002 s.

Figure 9 shows a voltage waveform of the circuit breaker. After T_1 is disconnected, the voltage at both ends of T_1 is equal to the voltage at both ends of L_1, which is 97.04 kV. When T_2–T_n is turned off, the voltage across L_1 gradually decreases. When the voltage of the breaking branch reaches the system voltage, the current begins to drop, the voltage of L_1 drops to zero and increases in the opposite direction. In addition, the capacitor branch B_2 and the peak voltage of a single breaking sub-module IGBT is about 60 kV. After the fault current drops to zero, K and K_1 are disconnected, and the voltage of T_1 and the IGBT branch B_1 drops. Figure 10 shows a current waveform of the circuit breaker. At 2.002 s, K is turned on, T_2 ~ T_n is turned on, T_1 is turned off, and the current of the main branch is reduced to 0A. The current is transferred to B_1 through the current-limiting inductor, the current of B_1 increases, and the current transfer is completed after 1 ms. Then a trigger signal is given to the thyristor T_{CN}, T_2 ~ T_n is turned off, and the B_1 current drops. At this time, the breaking current peak value is 7.35kA, and the peak value of the second rise rate is 1.35kA/ms. Then, the current is transferred to B_2, and the capacitor is charged. When the

Table 1 Simulation parameters

Components	Parameters
IGBTs	4.5 kV/3 kA
The thyristor	5 kV/4.5 kA
The rated voltage of the arrester	30 kV
The number of breaking sub-modules	6
Rated power of the system	650 MW
Line reactance	30 mH
Capacitance of MMC Neutron Module	3000 μF
Number of MMC sub-modules	38
Inductance of the bridge arm	70 mH
Line length	400 km
Δt_s	3.4 ms
The sampling frequency	10 kHz

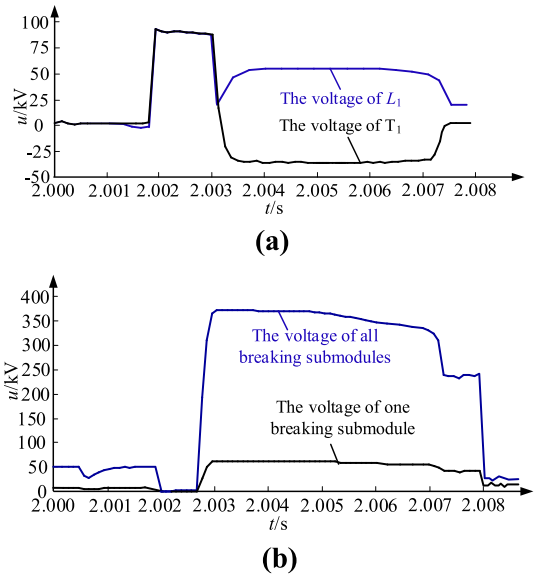

Fig. 9 Voltage simulation waveforms: **a** voltage of T_1 and L_1; **b** voltage of the breaking part

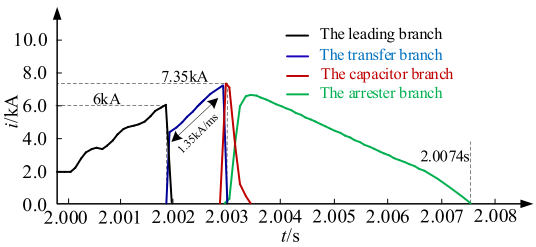

Fig. 10 Circuit breaker current simulation waveforms

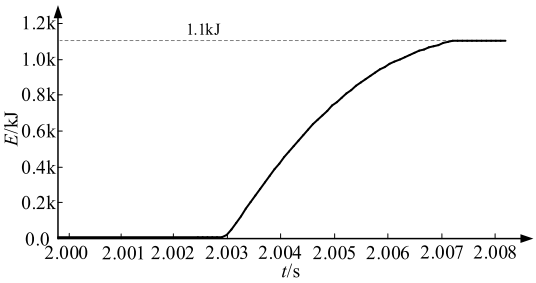

Fig. 11 Energy absorbed by the arrester

voltage of B_2 reaches the arrester operating voltage, the current begins transferring to the arrester branch B_3. The arrester absorbs the remaining energy in the circuit, and the fault current is reduced to 0A. The overall fault clearing time of the circuit breaker is 5.4 ms.

Figure 11 shows the energy absorbed by the arrester. The energy absorbed by each of the sub-module arresters is 1.1 MJ. Combined with Fig. 11, the fault current drops to 0A

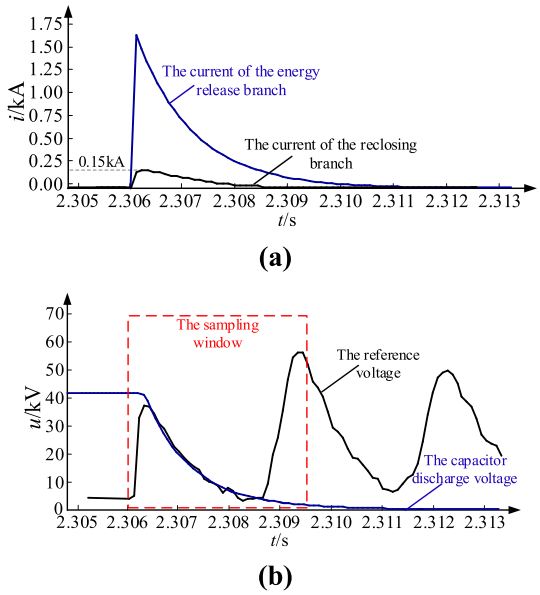

Fig. 12 Capacitor discharge voltage and current waveforms: **a** discharge current; **b** discharge voltage

at 2.0074 s, and the arrester maintains the breaking branch voltage within the clamping voltage range.

5.2 Fault nature discrimination simulation verification

At 2.206 s, the capacitor C_N discharges to the line through the reclosing branch, and at the same time closes K_3. Thus, all of the breaking sub-module capacitors discharge through the energy release branch. In this paper, $D(a_k,b_k)_{min}$ is set when the fault impedance is 500 Ω [17], $D(a_k,b_k)_{set}$ is 5.90 when a single-pole grounding fault occurs, and $D(a_k,b_k)_{set}$ is 5.26 when a pole-pole fault occurs. When an instantaneous fault occurs in the line, the voltage reverse wave amplitude measured at M is the largest. At this time, line current and voltage waveforms are shown in Fig. 12. It can be seen that when compared with the rated current of the line, the inrush current generated by C_N injecting signals into the faulty line is extremely small (0.15 kA), and that the voltage amplitude of the faulty line is less than $0.2U_{dcN}$. When a single-pole grounding fault occurs in the line, the voltage waveform measured at M is the reference voltage when there is an instantaneous fault at a distance of 60 km from point M. Simulation results of $D(a_k,b_k)$ under different fault properties are shown in Table 2. When a pole-pole fault occurs in the line, its fault impedance is generally smaller than that of a single-pole fault. Simulation results of $D(a_k,b_k)$ under different fault properties are shown in Table 3.

The ratio of $D(a_k,b_k)$ to $D(a_k,b_k)_{set}$ is used as an index to evaluate the accuracy of the fault nature discrimination method. The index can be expressed as:

$$AC = \frac{D(a_k, b_k)}{D(a_k, b_k)_{\text{set}}} \tag{25}$$

In this paper, the impact of noise on the proposed method is also analyzed. The added noise is Gaussian white noise with a signal–noise ratio (SNR) of 20 dB. Tables 4 and 5 show the AC of faults with different fault locations and fault impedances at 20 dB of white noise.

It can be seen from Tables 2, 3, 4, 5 that the simulation results verify the correctness of the theoretical derivation. Using ED can effectively identify the nature of a fault, and the method is not affected by the fault impedance, fault location, or noise.

6 Circuit breaker performance comparative analysis

An FDA-CCCB is placed in a 320 kV system at the same time as a traditional circuit breaker (scheme 1) and the circuit breaker in [9] (scheme 2), and they are compared under the same operating conditions. The circuit breaker action is

Table 2 Simulation results under single-pole grounding faults

		Fault location			
Nature of failure	Fault impedance	0 Ω	100 Ω	200 Ω	500 Ω
Instantaneous faults	60 km	0	0.15	0.21	0.27
	100 km	0.25	0.16	0.34	0.23
	200 km	0.21	0.13	0.02	0.01
	400 km	0.15	0.33	0.23	0.25
Permanent faults	60 km	16.94	12.02	10.09	9.53
	100 km	14.60	12.66	10.33	9.33
	200 km	12.75	11.11	10.35	8.85
	400 km	11.21	10.74	10.23	8.42

Table 3 Simulation results under pole-pole faults

		Fault location			
Nature of failure	Fault impedance	0 Ω	50 Ω	100 Ω	200 Ω
Instantaneous faults	60 km	0	0.13	0.17	0.24
	100 km	0.16	0.22	0.25	0.12
	200 km	0.05	0.18	0.14	0.23
	400 km	0.19	0.11	0.27	0.08
Permanent faults	60 km	14.59	12.43	11.33	9.64
	100 km	13.86	12.31	10.24	10.02
	200 km	12.52	11.29	10.26	9.67
	400 km	12.07	11.13	9.97	9.05

Table 4 AC at 20 dB white noise under single-pole grounding faults

		Fault location			
Nature of failure	Fault impedance	0 Ω	100 Ω	200 Ω	500 Ω
Instantaneous faults	60 km	0.020	0.071	0.085	0.072
	100 km	0.053	0.072	0.086	0.080
	200 km	0.081	0.069	0.092	0.080
	400 km	0.042	0.081	0.071	0.071
Permanent faults	0 km	3.151	2.423	1.726	1.715
	100 km	2.657	2.256	2.003	1.697
	200 km	2.241	1.992	1.863	1.691
	400 km	2.168	2.184	1.863	1.572

Table 5 AC at 20 dB white noise under pole-pole faults

Nature of failure	Fault impedance	Fault location			
		0 Ω	50 Ω	100 Ω	200 Ω
Instantaneous faults	60 km	0.015	0.064	0.091	0.077
	100 km	0.046	0.072	0.081	0.069
	200 km	0.089	0.073	0.092	0.076
	400 km	0.059	0.043	0.082	0.077
Permanent faults	0 km	2.905	2.563	2.316	2.062
	100 km	2.645	2.648	2.295	2.185
	200 km	2.509	2.331	2.144	2.025
	400 km	2.516	2.344	1.964	1.968

shown in Fig. 13. By comparison, the effectiveness of the FDA-CCCB in current-limiting and reducing the fault clearing time is verified.

Figure 14 shows a comparison of three circuit breakers. In addition, Table 6 shows the differences in the breaking currents, operating times, device withstand voltages, arrester energy absorptions, and number of components

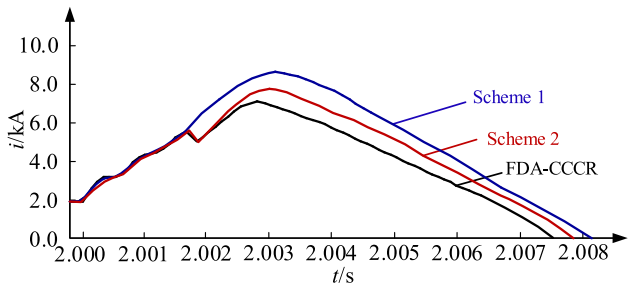

Fig. 13 Performance comparison of three circuit breakers

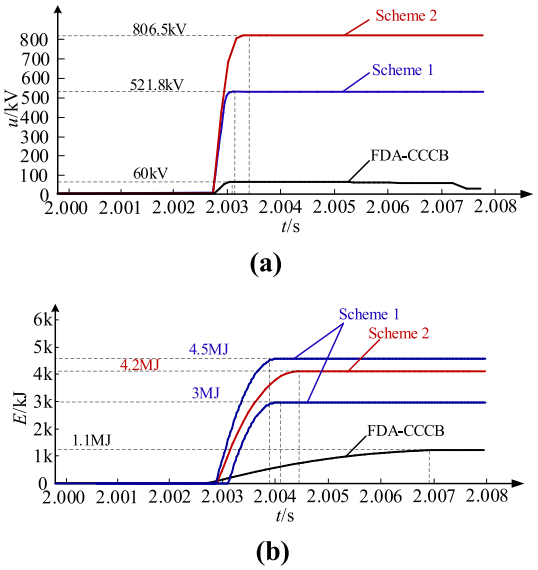

Fig. 14 Comparison of different circuit breakers: **a** IGBT voltage of the breaking branches; **b** energy absorption

Table 6 Comparison of different circuit breakers

Scheme	Scheme 1	Scheme 2	FDA-CCCB
Current peak	9 kA	7.56 kA	7.35 kA
Operation time	6.1 ms	5.7 ms	5.4 ms
IGBT voltage	521.8 kV	806.5 kV	60 kV
Dissipated energy	7.5 MJ	8.4 MJ	6.6 MJ
Number of IGBTs	714	672	245
Number of thyristors	0	172	257

for the different circuit breaker schemes. It can be seen that the first scheme adopts a stepping input arrester, which reduces the energy absorption of a single arrester to a certain extent. In addition, the total absorbed energy is 7.5 MJ. There are two capacitor commutation units in scheme 2, where each unit is equipped with a surge arrester, the energy absorbed by the two surge arresters is the same, and the total energy consumption is 8.4 MJ. The FDA-CCCB adopts capacitor commutation, sets the RCN to limit the current flowing into the arrester, reduces the energy absorption requirements of the arrester, and the total energy consumption is 6.6 MJ. In terms of cost, the FDA-CCCB adopts a bridge structure in the main branch, the transfer branch realizes bidirectional breaking, and the current amplitude is the smallest. Thus, the number of IGBTs is greatly reduced, and only 245 IGBTs are required. In the scheme proposed in this paper, thyristors are used in the capacitor branch to prevent the capacitor charging from increasing the fault current during normal operation. In addition, thyristors are used in the closing branch to control capacitor discharge. The number of series–parallel thyristors needs to be considered, and the total number of thyristors used is 257. Although more thyristors are used, when compared with IGBTs, thyristors are cheap and widely used.

In summary, the circuit breaker scheme proposed in this paper meets the requirements of fast interruption while ensuring a low cost.

7 Conclusion

A capacitor-commutated DC circuit breaker with fault character discrimination capability was presented in this paper. Taking a 320 kV double-terminal flexible DC system as background, the circuit breaker model was built by PSCAD for simulation verification. The following conclusions can be drawn:

1) The FDA-CCCB adopted a T-shaped structure, which greatly reduced the number of components and reduced the cost of circuit breakers. The breaking branch of this topology adopted a modular structure to reduce the voltage of the capacitor branch, which effectively reduced the voltage equalization problem of the IGBTs. In addition, the control of this topology is simple. Based on this topology, the parameter design principles and methods of the capacitors, the current-limiting inductors, and the other devices were analyzed. It was found that the current-limiting inductance in the circuit breaker could effectively limit the fault current amplitude to 7.35 kA, which reduced the current stress of the circuit breaker. Finally, the breaking speed of the circuit breaker is comparable to other circuit breakers that do not have current-limiting capability.
2) To avoid the non-selective reclosing of the circuit breaker, this paper proposed the addition of a reclosing branch in the circuit breaker. The voltage of the capacitor was discharged to the fault line, and the injected voltage signal amplitude fluctuation range was between 0.1 and 0.2 times the rated value. Thus, it did not affect the system or health line. According to the refractive reflection characteristics of the injected voltage wave, Euclidean distance was introduced to distinguish between instantaneous and permanent faults. Through simulation verification, it was found that the method proposed in this paper has no dead space, and requires a low sampling rate, has a simple principle, is easy to implement, and possesses good capability in terms of fault impedance and noise interference.

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Data availability All data, models generated or used during the study appear in the manuscript.

Declarations

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

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