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ORIGINAL ARTICLE

Evaluation of DPWM schemes for Si/SiC three-level hybrid active NPC inverters

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Abstract
The hybrid utilization of SiC and Si devices can achieve a trade-off between the efficiency and cost of three-level active neutral-point-clamped (3L-ANPC) inverters. This paper studies a three-phase 2-SiC 3L-hybrid ANPC (3L-HANPC) inverter with different discontinuous pulse width modulation (DPWM) schemes. The principles of these DPWM schemes are analyzed in detail, and carrier-based algorithm for two of the DPWM schemes are given. Finally, a 6 kW three-phase 2-SiC 3L-HANPC inverter prototype was built to compare these two modulation schemes. Experimental results show that DPWM1 with its peak voltage-clamped can achieve a higher efficiency than DPWM2 with its zero-crossing clamped. However, the DPWM2 scheme has a lower THD than the DPWM1 scheme. Since the THD improvement contributed by the DPWM2 scheme is relatively small, the DPWM1 scheme is the preferred DPWM scheme.

Keywords Three-phase 3L-ANPC inverter · Discontinuous pulse width modulation · Si/SiC hybrid

1 Introduction

Compared with Si semiconductor materials, wide bandgap (WBG) semiconductor materials represented by silicon carbide (SiC) have a higher breakdown voltage, better thermal stability, higher saturation drift velocity of the carrier, and higher thermal conductivity [1]. Therefore, SiC devices can operate with a higher switching frequency and a higher efficiency [2, 3]. As a result, SiC devices have attracted a great deal of attention in emerging industries such as electric vehicle (EV) chargers and energy storage systems. However, in high-capacity applications, such as motor drivers and photovoltaic (PV) inverters, SiC devices are too expensive to be widely used, while traditional Si IGBT devices are still the mainstream [4]. Therefore, converters with a combination of SiC and Si devices are cost-effective [5, 6].

A performance comparison of a Si-based soft-switching inverter and a SiC-based hard switching inverter was presented in [7]. Results showed that at a high switching frequency, the cost of the SiC-based inverter was 60% lower than that of the soft-switching inverter, while higher efficiency was achieved. In [8], a Si/SiC hybrid converter was designed to drive a high-speed motor. Based on the hybrid utilization of Si and SiC devices, a high switching frequency, small overall power loss, and output current ripple were realized at a low cost. In [9], a three-phase Si/SiC three-level hybrid active neutral-point-clamped (3L-HANPC) converter for medium voltage high-speed drive systems was proposed, and a corresponding optimized space vector pulse width modulation (SVPWM) was presented. While the voltage balance of the upper and lower capacitors on the DC side was ensured, the switching loss was concentrated in the SiC MOSFETs to realize a high efficiency and low cost.

However, when WBG devices are applied to enhance the switching frequency and power density, the switching loss inevitably increases. Thus, discontinuous pulse width modulation (DPWM) instead of continuous pulse width modulation (CPWM) is a better solution for converters with a high switching frequency [10–15]. In addition, considering that a high switching frequency reduces the interrupt cycle of digital control, the calculation of DPWM based on the space vector synthesis method is complicated [13]. Thus, DPWM modulation based on the carrier-based method has been used to lower the calculation burden of digital processors [16, 17].

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A DPWM scheme for use in a grid-tied three-level neutral point-clamped (3L-NPC) converter was presented in [14]. In this way, the targets of reducing losses and increasing efficiency were realized. The DPWM scheme applied to a three-level (3L) inverter was optimized in [18]. In addition, the peak clamped DPWM and the carrier-based zero-crossing clamped DPWM methods were presented.

To date, there have been many comparative evaluations of Si/SiC hybrid inverters based on SVPWM schemes. However, the comparative analysis of DPWM schemes, especially for three-phase Si/SiC 3L-HANPC converters, still needs to be explored. Therefore, based on the three-phase Si/SiC 3L-HANPC inverter, two DPWM schemes, peak clamped DPWM and zero-crossing clamped DPWM, are compared with respect to efficiency and total harmonic distortion.

The remainder of this paper is organized as follows. First, the topology of a 3L-ANPC inverter with the combination of Si IGBTs and SiC MOSFETs is presented, and the conventional SVPWM scheme is introduced. The principle of peak clamped DPWM and zero-crossing clamped DPWM is discussed. Then, a power loss model is built to theoretically evaluate the efficiency performance of these two DPWM schemes. Then, a THD performance comparison is conducted by simulation. In Sect. 4, an experimental comparison of the efficiency and THD performance is demonstrated. Finally, Sect. 5 concludes the paper.

2 Three-phase Si/SiC 3L-HANPC inverter

2.1 Three-phase 2-SiC 3L-HANPC inverter topology

The ANPC converter is the only three-level topology that can decouple circuits into high-frequency and low-frequency parts, which easily implements the hybrid application of SiC MOSFETs [9]. Thus, the SiC MOSFETs operate at high frequency and have the switching loss centrally, while the Si IGBTs operate at the fundamental frequency, which reduces the cost while keeping the efficiency comparable to that of the full SiC inverter [19–21]. The topology of the three-phase 2-SiC 3L-HANPC inverter proposed in [9] is depicted in Fig. 1. The two switches S_{x5} and S_{x6} (x = a, b, c) of each phase are replaced with SiC MOSFETs as high switching frequency switches. They act complementarily at high switching frequencies, marked as dark yellow. The rest of the devices are Si IGBTs.

There are four switching states by employing the SVPWM scheme for an ANPC inverter, as given in Table 1. In this table, 1 and 0 represent the ON and OFF states of the switches, respectively. Phase A is taken as an example to clearly illustrate the switching states. The

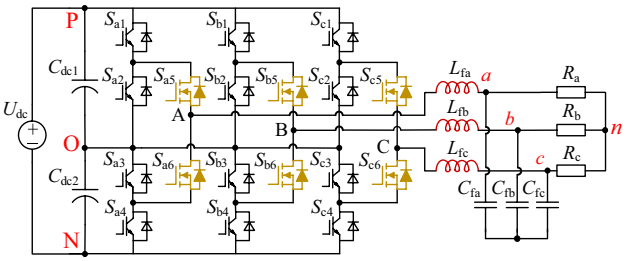

Fig. 1 Three-phase 2-SiC 3L-HANPC inverter topology

commutation process of the switching states during the positive half cycle is depicted in Fig. 2.

2.2 Principle of the SVPWM Scheme

There are 64 three-phase switching states in the SVPWM scheme of this hybrid inverter. They are generated by combining the above four switching states "P," "U," "L," and "N." The distribution of the corresponding voltage vectors in the three-level vector space is shown in Fig. 3, where "O" stands for "U" or "L." These voltage vectors are distributed in six large sectors from I to VI, and each of the large sectors can be divided into six small regions from 1 to 6.

According to Fig. 3, taking the reference voltage vector $\boldsymbol{V}_{\mathrm{ref}}$ located in sector I regions 3 as an example for analysis, the switching states process can be obtained based on the principle of "nearest three vectors" (NTV), as shown in Fig. 4. It is clear that the modulating signals are never clamped during the switching cycle in the conventional SVPWM.

3 Principle of the peak clamped DPWM and zero-crossing clamped DPWM schemes

In SVPWM, the bridge-leg voltage level of each phase is varied in every switching cycle, and the switching loss increases with the increase in the switching frequency. By discarding the redundant vector, DPWM clamps the bridge-leg voltage of one phase in a switching cycle. As a result, the switching times for each of the switching cycles are reduced to 2/3 of the continuous modulation, which ultimately reduces the switching loss at high switching frequencies [18]. This section introduces two common DPWM schemes for three-phase inverters: peak clamped DPWM1 and zero-crossing clamped DPWM2.

Table 1 3L-ANPC Switching States

Switching states	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	Voltage level
P	1	0	1	0	1	0	$0.5U_{dc}$
L	1	0	1	0	0	1	0
U	0	1	0	1	1	0	0
N	0	1	0	1	0	1	$-0.5U_{dc}$

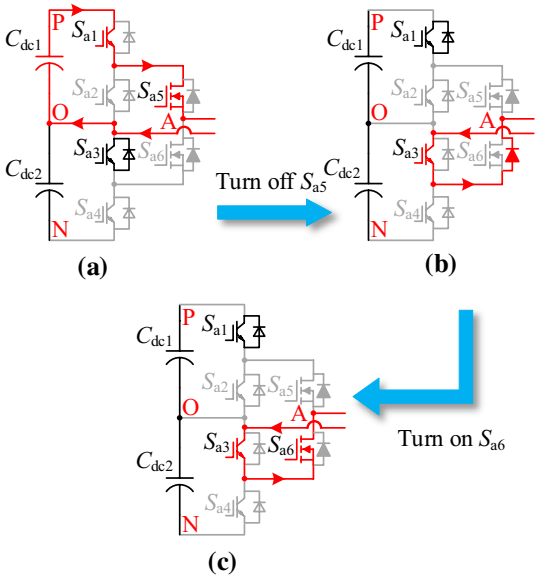

Fig. 2 Demonstration of the commutation process during the positive half cycle: **a** P state; **b** dead-time; **c** L state

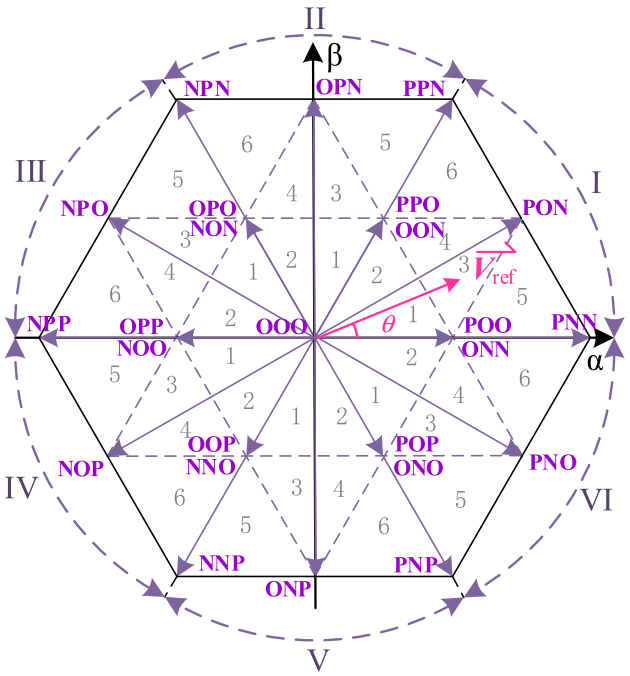

Fig. 3 Vector distribution and sector division

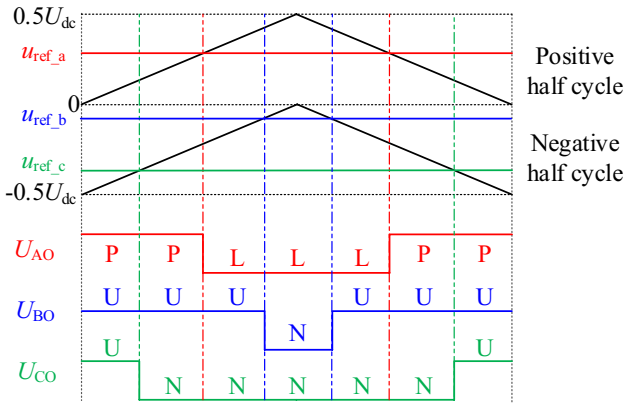

Fig. 4 Seven-segment sequence in sector I-3 with the reference voltage for each phase and the switching states for each segment

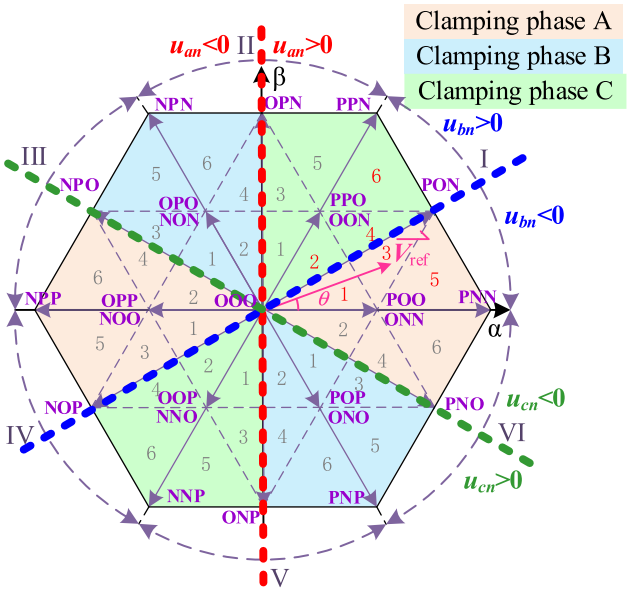

Fig. 5 Clamping modes of DPWM1 scheme

3.1 Principle of the peak clamped DPWM1 scheme

The clamping mode of peak clamped DPWM1 is shown in Fig. 5. From this figure, it can be seen that the vector

clamping area is mainly adjacent to the peak value of the output voltage.

Moreover, the DPWM scheme can be implemented by injecting a zero-sequence component into three-phase sinusoidal modulation waves. The referenced three-phase sinusoidal modulation waves are expressed as:

$$\begin{cases} u_{\mathrm{Ma}} = M\cos(2\pi f_{\mathrm{g}} t) \\ u_{\mathrm{Mb}} = M\cos(2\pi f_{\mathrm{g}} t - 2\pi/3) \\ u_{\mathrm{Mc}} = M\cos(2\pi f_{\mathrm{g}} t + 2\pi/3) \end{cases}, \tag{1}$$

where f_{g} is the fundamental frequency of the utility grid, and M represents the normalized modulation amplitude value, which also represents the modulation index, and is calculated as follows:

$$M = \frac{\sqrt{6}U\mathrm{ac}}{U\mathrm{dc}}, \tag{2}$$

where U_{ac} is the RMS value of the utility grid phase voltage, and U_{dc} is the DC bus voltage.

The injected zero-sequence component can be acquired as follows:

$$u_{\mathrm{z1}} = \begin{cases} 1 - u_{\max} | u_{\max} | \geq | u_{\min} | \\ -1 - u_{\min} | u_{\max} | < | u_{\min} | \end{cases}, \tag{3}$$

where $u_{\max}$ and $u_{\min}$ are the maximum and minimum of the three-phase sinusoidal modulation wave at certain times.

The three-phase modulation wave $u_{\mathrm{ref\_}x}$ (x = a, b, c) of DPWM1 can be obtained by injecting (3) into (1), which is expressed as:

$$u_{\mathrm{ref\_}x} = u_{\mathrm{M}x} + u_{\mathrm{z1}}, x = \mathrm{a, b, c}. \tag{4}$$

Taking phase A as an example, modulation waves of DPWM1 and the injected zero-sequence component under different modulation indices are presented in Fig. 6. It is clearly shown that DPWM1 is always clamped near the peak area of the modulation wave, which corresponds to the clamping areas in Fig. 5.

The position of the reference vector $\boldsymbol{V}_{\mathrm{ref}}$ is shown in Fig. 5. Meanwhile, the modulation waves of DPWM1, the voltage level of the bridge leg, and the corresponding switching states in a single switching cycle are illustrated in Fig. 7. When the modulation signal is greater than 0, the bridge leg voltage level of the unclamped phase is changed between the "P" and "L" states. Meanwhile, that of the clamped phase is forced to the "P" state. When the modulation signal is less than 0, the bridge leg voltage level of the unclamped phase switches is changed between the "U" and "N" states, and that of the clamped phase is forced to the "N" state. As shown in Fig. 7, the voltage level of phase A is clamped to P at this time.

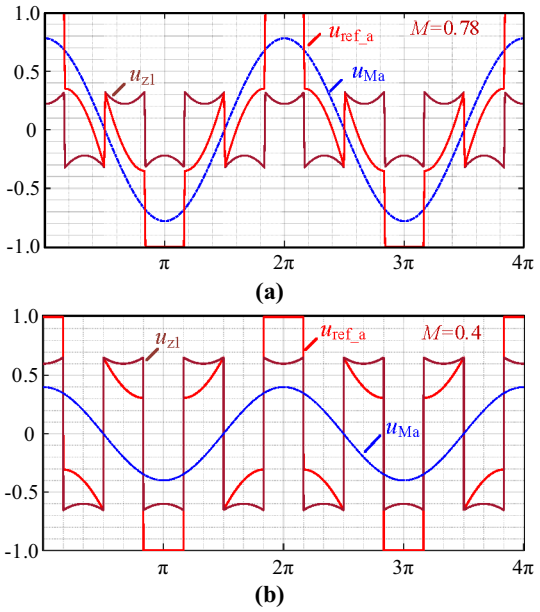

Fig. 6 Waveforms of the modulation wave and the zero-sequence components of DPWM1: **a** M=0.78; **b** M=0.4

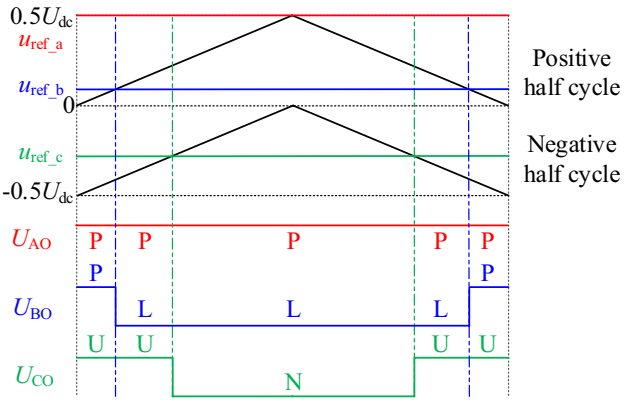

Fig. 7 Switching-state sequence in sector I region 3 of the DPWM1 scheme

3.2 Principle of the zero-crossing clamped DPWM2 scheme

The clamping mode of the zero-crossing clamped DPWM2 is shown in Fig. 8. The vector clamping area is mainly adjacent to the zero-crossing point and peak point of the output voltage, which can improve the zero-crossing distortion.

The carrier-based implementation method of DPWM2 was presented in [14]. The zero-sequence component can be calculated as follows:

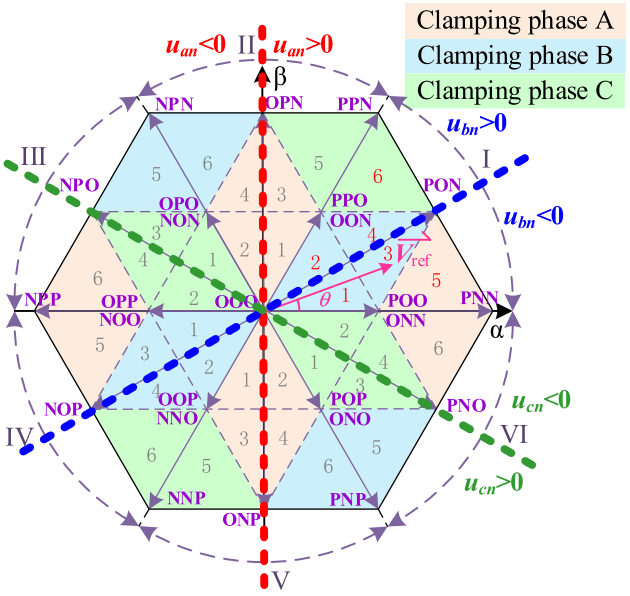

Fig. 8 Clamping modes of the DPWM2 scheme

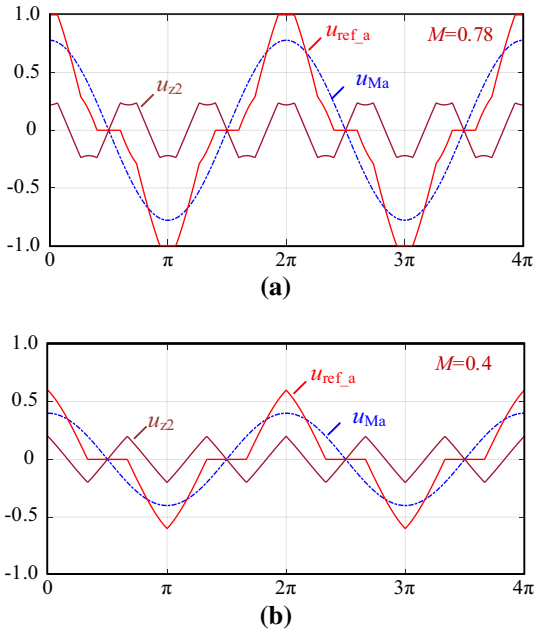

Fig. 9 Waveforms of the modulation wave and the zero-sequence components of DPWM2: **a** $M=0.78$; **b** $M=0.4$

$$u_{z2}=\begin{cases}-u_{\mathrm{mid}} & |u_{\max}|\geq|u_{\min}|,u_{z1}>-u_{\mathrm{mid}}\\ 1-u_{\max} & |u_{\max}|\geq|u_{\min}|,u_{z1}<-u_{\mathrm{mid}}\\ -u_{\mathrm{mid}} & |u_{\max}|<|u_{\min}|,u_{z1}<-u_{\mathrm{mid}}\\ -1-u_{\min} & |u_{\max}|<|u_{\min}|,u_{z1}>-u_{\mathrm{mid}}\end{cases}, \tag{5}$$

where $u_{\max}$, $u_{\min}$, and u_{mid} stand for the maximum, minimum, and intermediate values of a three-phase sinusoidal modulation wave at a certain time. The intermediate variable required for judgment u_{z1} can be calculated by (3).

Similarly, a three-phase modulation wave of DPWM2 can be calculated by substituting (5) into (1). When the modulation index is higher than 0.577, the modulation wave is clamped at the zero-crossing and peak points. However, when the modulation index is less than 0.577, the clamping area of the modulation wave is adjacent to the zero-crossing point.

Figure 9 illustrates modulation waves of DPWM2 and its injected zero-sequence component under different modulation indices for phase A. It corresponds to the clamping areas shown in Fig. 8. The relationships among the modulation wave of DPWM2, the voltage level of the bridge leg, and the corresponding switching states are demonstrated in Fig. 10. When the reference vector is located in sector I region 3, as shown in Fig. 8, it is clear that the voltage level of phase B is clamped to the "U" level.

3.3 Power loss and THD performance analyses

A power loss model was built to quantitatively analyze the efficiency performance of these two DPWM schemes [22, 23]. By employing the 3L-HANPC converter topology and the two DPWM schemes, the SiC MOSFETs operate at a high switching frequency, while the Si IGBTs operate at the fundamental switching frequency. Therefore, the switching loss of the Si IGBTs can be ignored. The conduction loss of IGBTs can be expressed as:

$$P_{\text{on - loss\_IGBT}}=12\times\sum_{i=1}^{\mathrm{M_f}}V_{\mathrm{CE(on)}}I_{\mathrm{D}}(i), \tag{6}$$

where $V_{\mathrm{CE(on)}}$ is the ON-state voltage drop of the IGBT, and $I_{\mathrm{D}}(i)$ represents the ON-state collector-emitter current in the i-th switching period. The total switching time $\mathrm{M_f}$ in a fundamental cycle can be obtained by (7), where f_{g} and

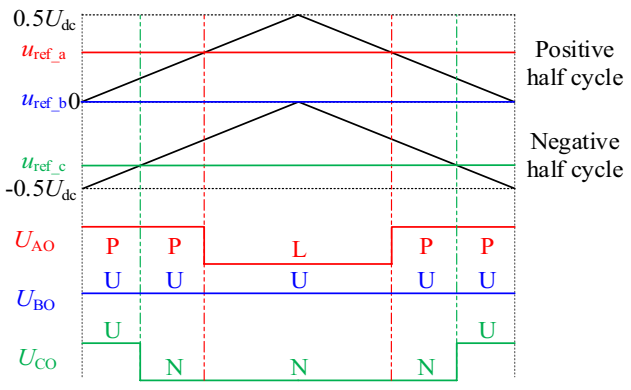

Fig. 10 Switching-state sequence in sector I region 3 of the DPWM2 scheme

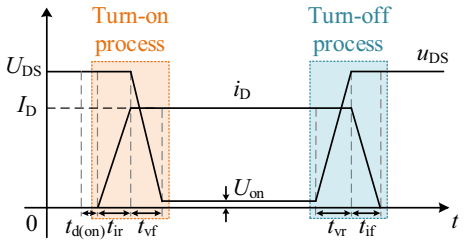

Fig. 11 Switching process of a SiC MOSFET

f_s represent the fundamental frequency and the switching frequency, respectively.

$$M_f = \frac{f_s}{f_g}. \tag{7}$$

A switching process model of a SiC MOSFET was built, as shown in Fig. 11, where U_{DS} is the OFF-state drain-source voltage, and I_D is the ON-state drain current. When the MOSFET is turned ON, the ON-state resistance between the drain and the source is $R_{DS\ (on)}$ [22]. At this time, the drain-source voltage is U_{on}. t_{ir} and t_{vr} represent the rise times of the drain current and the drain-source voltage, respectively. t_{if} and t_{vf} are the fall times of the drain current and the drain-source voltage, respectively. $t_{d(on)}$ represents the turn-ON delay time of the MOSFET. All of the above data can be extracted from the SiC MOSFET datasheet.

Taking one switching cycle as an example, the switching loss of the SiC MOSFETs is zero when the bridge-leg voltage is clamped. Otherwise, the switching loss of the SiC MOSFETs during the i-th switching cycle is calculated as follows:

$$P_{\text{switching - loss}}(i)=\frac{1}{T_s}\int_0^{T_s} u_{DS}i_D dt = \frac{1}{2T_s}U_{DS}(i)I_D(i)(t_{ir}+t_{if}+t_{vr}+t_{vf}) \tag{8}$$

where $U_{DS}(i)$ and $I_D(i)$ are the drain-source voltage in the OFF state of the MOSFET, and the drain current in the ON state during the i-th switching cycle. Therefore, the switching loss of the three-phase 2-SiC 3L-HANPC inverter can be expressed as:

$$P_{\text{switching - loss}} = 6\times\sum_{i=1}^{M_f} P_{\text{switching - loss}}(i) \tag{9}$$

The conduction power loss of the SiC MOSFETs can be expressed as:

$$P_{\text{on - loss\_MOSFFET}} = 6\times\sum_{i=1}^{M_f}\frac{I_D^2(i)R_{DS(on)}(dT_s - t_{d(on)} - t_{ir})}{T_s}. \tag{10}$$

where d represents the duty cycle, and T_s represents the switching period. The total power loss of the Si IGBTs and the SiC MOSFETs can be calculated as:

$$P_{\text{loss}} = P_{\text{on - loss\_IGBT}} + P_{\text{on - loss\_MOSFFET}} + P_{\text{switching - loss}}. \tag{11}$$

The power loss calculation results of a three-phase 2-SiC 3L-HANPC inverter with different loads and modulation indices while using the two DPWM schemes are depicted in Fig. 12. As can be seen, the power loss of the DPWM1 scheme is always less than that of the DPWM2 scheme. Thus, since the clamping areas of the DPWM1 scheme are near the peak of the AC voltage and that of the output current, it can reduce more switching loss than the DPWM2 scheme, which leads to higher efficiency.

Simulation waveform of the two DPWM schemes and the harmonic spectrums of u_{An} are presented in Fig. 13. The

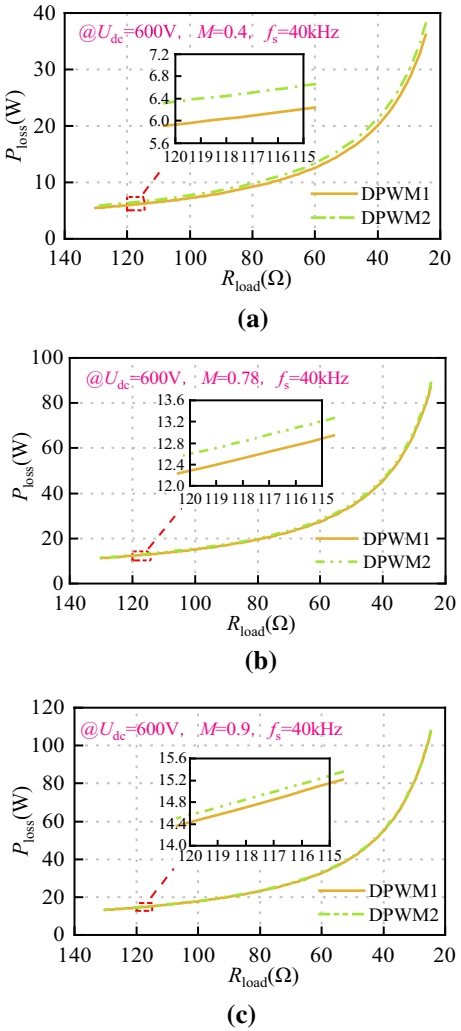

Fig. 12 Calculated loss of a three-phase 2-SiC 3L-HANPC inverter with different modulation indices under different DPWM schemes: **a** $M=0.4$; **b** $M=0.78$; **c** $M=0.9$

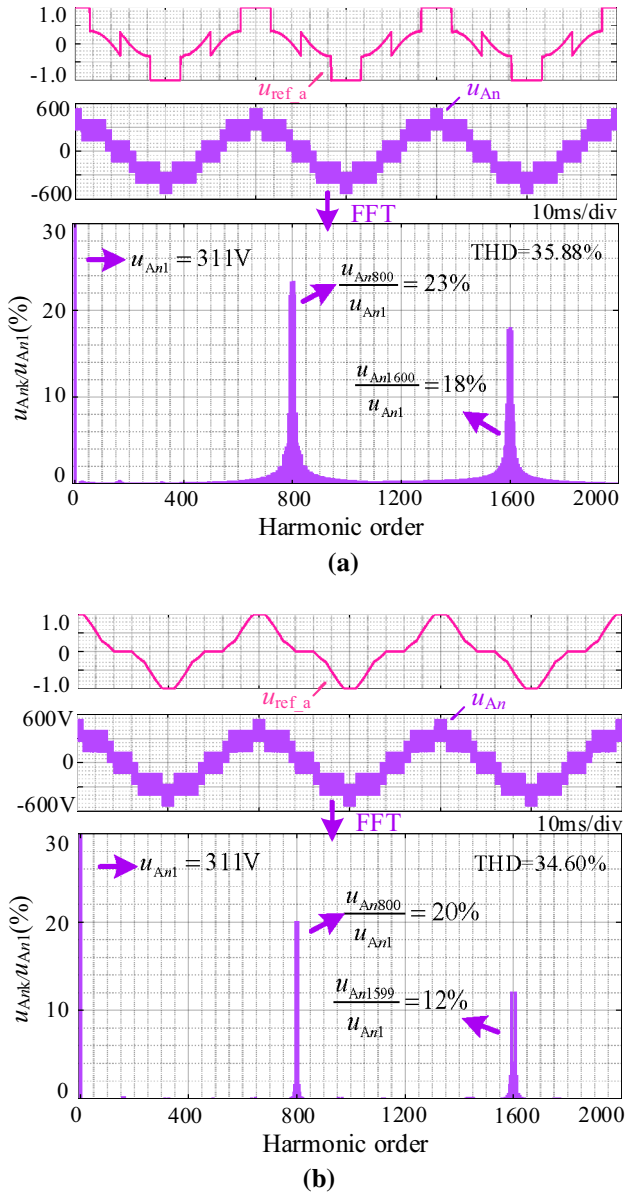

Fig. 13 Simulation waveforms and harmonic analysis results of different DPWM schemes: **a** DPWM1; **b** DPWM2

simulation conditions are consistent with the experimental conditions shown in Table 2. u_{An} represents the differential-mode voltage between terminal A and terminal n, as shown in Fig. 1. u_{ref_A} is the modulation signal. As shown in Fig. 13, since the DPWM1 scheme has more harmonics near the switching frequency, DPWM2 has better harmonic performance than DPWM1.

Table 2 3L-HANPC inverter prototype specifications

Parameter	Value
Rated output power	6 kW
DC bus voltage	600–800 V
Output voltage and frequency	220 V and 50 Hz
Switching frequency	40 kHz
Filter inductance L_f	1.4 mH
Filter capacitance C_f	4.7 μF
SiC MOSFET	SCT3080AL
Si IGBT	IKW30N60H3
Main controller	TMS320F28335

4 Comparison of two modulation schemes

For an experimental comparison of the two different DPWM schemes, a three-phase 2-SiC 3L-HANPC inverter prototype was built in the laboratory.

The parameters of the 3L-HANPC inverter prototype are listed in Table 2. A TMS320F28335 and an EPM-570T100I5N are used as the digital controller of this prototype. A picture of the prototype is shown in Fig. 14,.

Steady-state waveforms of the phase A driving signals while employing DPWM1 and DPWM2 are given in Figs. 15 and 16, respectively. Where u_{gs1}, u_{gs2}, u_{gs5}, and u_{gs6} represent the driving signals of S_{a1}, S_{a2}, S_{a5}, and S_{a6}, while the modulation index is 0.78. From Fig. 15, it is clear that the driving signal of DPWM1 is only clamped near the peak point of the AC voltage. The driving signal of DPWM2 is clamped at both the zero-crossing and

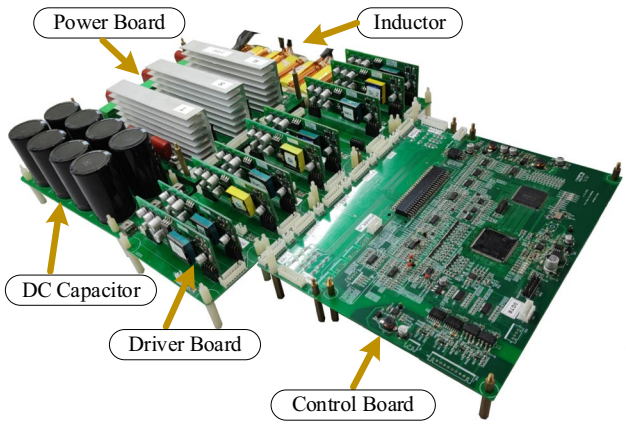

Fig. 14 Three-phase 2-SiC 3L-HANPC inverter prototype

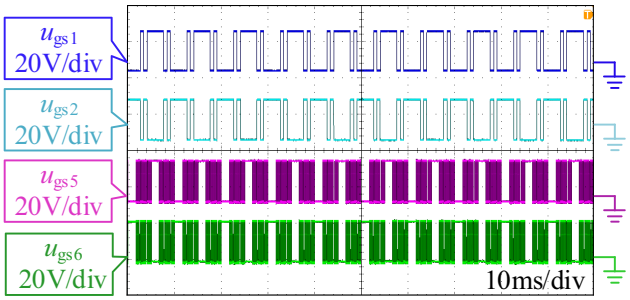

Fig. 15 Driving signals of DPWM1 modulation

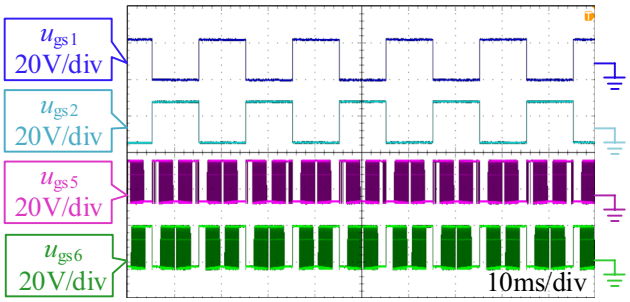

Fig. 16 Driving signals of DPWM2 modulation

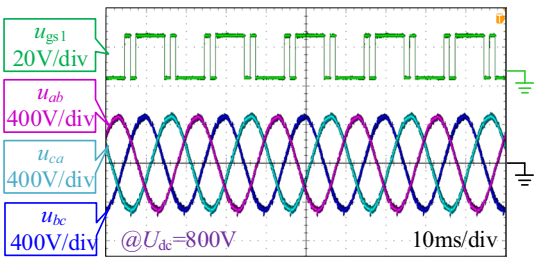

Fig. 17 Three-phase line voltage and driving signal waveforms of the DPWM1 scheme

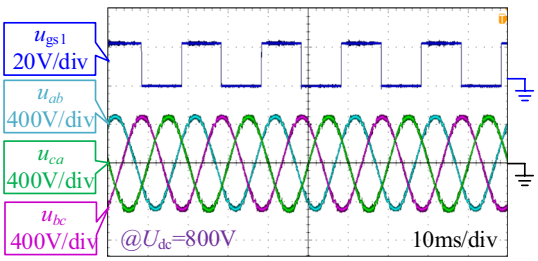

Fig. 18 Three-phase line voltage and driving signal waveforms of the DPWM2 scheme

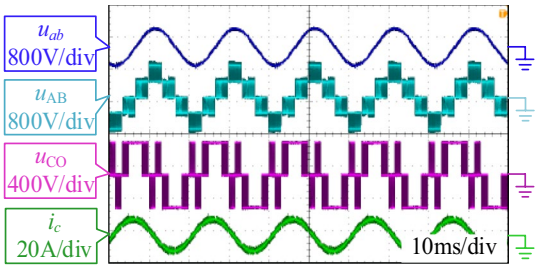

Fig. 19 Steady state waveforms of DPWM1 modulation

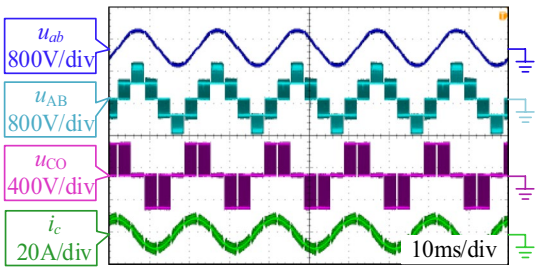

Fig. 20 Steady state waveforms of DPWM2 modulation

peak points of the AC voltage, which is consistent with the analysis in Sect. 3. Steady-state line voltage waveforms of the 2-SiC 3L-HANPC inverter while using DPWM1 and DPWM2 are shown in Figs. 17 and 18, respectively. u_{ab}, u_{bc}, and u_{ca} represent line voltages. The output power is 3 kW, and the DC bus voltage is 800 V. It can be seen that the quality of the output voltage is good.

Steady-state waveforms of DPWM1 and DPWM2 with 5 kW of output power are presented in Figs. 19 and 20, where u_{AB} and u_{ab} represent the line voltage before and after filtering, respectively. u_{CO} and i_c are the bridge leg voltage and current of phase C. This indicates that DPWM1 generates a voltage jump near the zero-crossing point, while the voltage level is clamped at the zero-crossing point to improve the voltage quality under DPWM2. However, the clamping area near the peak point of DPWM2 is much smaller than that of DPWM1. Therefore, DPWM1 can reduce more switching loss than the DPWM2 scheme, which is consistent with the above analysis.

A WT-1800 power analyzer is used to measure the efficiencies and THDs of the two modulation schemes. The measured efficiencies are shown in Fig. 21. It can be found that the efficiency of DPWM1 is always higher than that of DPWM2. In addition, this advantage is more significant under low modulation index conditions. This is due to the

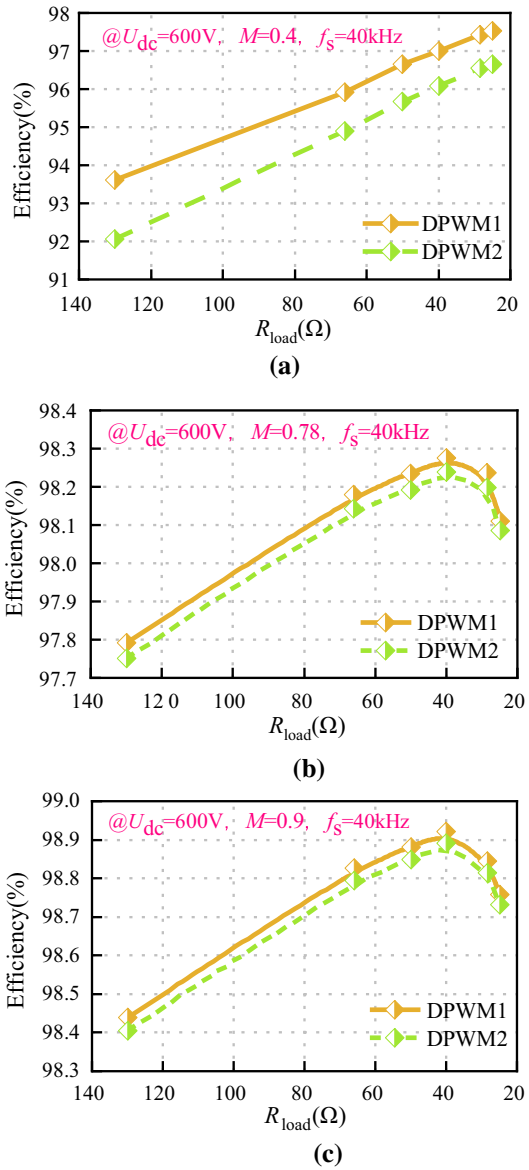

Fig. 21 Measured efficiency curves of two schemes under different conditions: **a** $M=0.4$; **b** $M=0.78$; **c** $M=0.9$

fact that the clamping area of the DPWM1 scheme is near the peak value point of the output voltage and that of the output current. Furthermore, experimental results show that the peak efficiency of DPWM1 is about 98.9%, with $M=0.9$.

The measured voltage THDs of the two schemes with different loads and modulation indices are shown in Fig. 22. From this figure, it can be found that the THD value of the DPWM2 scheme is lower than that of the DPWM1 scheme. Thus, although the DPWM2 scheme has a lower efficiency, its THD performance is better than that of the DPWM1 scheme.

According to the efficiency and THD comparison results, the THD value difference between the two DPWM

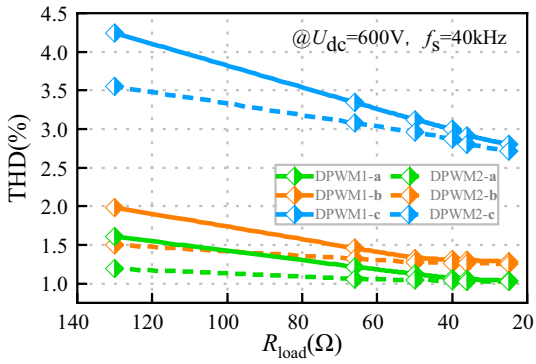

Fig. 22 Measured THDs of two schemes under different conditions: **a** $M=0.4$; **b** $M=0.78$; **c** $M=0.9$

schemes is relatively small. However, the efficiency of the DPWM1 scheme is higher than that of the DPWM2 scheme, especially with low modulation indices. Therefore, DPWM1 is the preferred DPWM scheme for 2-SiC 3L-HANPC inverters.

5 Conclusion

Based on a three-phase 2-SiC 3L-HANPC inverter prototype platform, a performance comparison between two common DPWM schemes for three-phase inverters: peak clamped DPWM1 and zero-crossing clamped DPWM2 was conducted. The analysis and experimental results show a number of things.

(1) The DPWM1 scheme with its peak voltage clamped can achieve a higher efficiency than DPWM2 with its zero-crossing clamped when applied to the three-phase 2-SiC 3L-HANPC inverter.
(2) However, the DPWM2 scheme has better THD performance than that of the DPWM1 scheme.

Since the THD improvement contributed by the DPWM2 scheme is relatively small, the DPWM1 scheme is a preferred solution for improving the efficiency of three-phase 2-SiC 3L-HANPC inverters.

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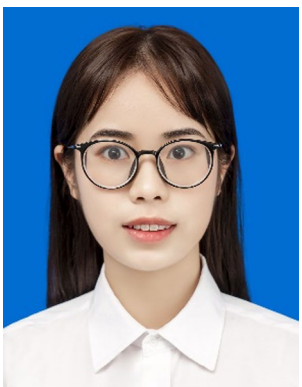

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