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ORIGINAL ARTICLE

Generalized switched-capacitor multilevel inverter topology with self-balancing capacitors

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Abstract
This paper presents a switched-capacitor topology with fewer switching components and reduced voltage stresses. The circuit contains eight switches and two capacitors to generate a five-level voltage waveform. This paper provides in-depth descriptions of the structural design, operation, and loss analysis. Inherently self-balanced capacitors are utilized in the proposed topology, which eliminates the need for additional charge balancing circuits and sensors. The control action was implemented using a simple logic-based multicarrier pulse width modulation (PWM) strategy. A brief comparative analysis with state-of-the-art topologies has been presented to demonstrate the merits of the developed topology. Finally, the feasibility and efficacy of the suggested topology have been evaluated using simulation and experimental testing to ensure that it is both feasible and effective.

Keywords Cost function · Multilevel inverter · Pulse width modulation · Switched capacitor

1 Introduction

Renewable and sustainable energy sources, such as solar and wind farms, have gained considerable attention from researchers and industry in recent years due to their reduced environmental effect and increasing economic benefits. Due to the rapid improvements in power electronics equipment technology, numerous power converter topologies for new energy/power systems have been developed. Multilevel inverters (MLIs) are the most popular of these topologies. This is to the reduced dv/dt stress on the switch, high power quality, reduced filter size, greater efficiency, reduced EMI, etc. [1, 2].

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Standard multilevel inverters are generally classified as diode clamped, flying capacitor (FC), and cascading H-bridge (CHB) inverters. These traditional inverters have several advantages over two-level inverters. These advantages include lower switching and conduction power losses, better efficiency, and a significantly improved power quality. On the other hand, these topologies have several drawbacks. Diode clamped and flying capacitor inverters having issues with capacitor voltage balancing and requiring more clamping diodes to achieve higher voltage levels [3]. Requiring several isolated DC sources for an increased number of voltage levels constitutes the main constraint of CHB inverters [4]. The voltage gain of all of the modules listed above is limited to one, which is a common limitation among classical multilevel inverters. These difficulties may make these converters unsuitable for industrial uses. Achieving the maximum voltage level from a DC source is advocated in [5]. In addition, there is a lack of voltage boosting capacity in modified structural designs.

As a result, there is a rising trend towards designing novel switched-capacitor (SC) inverter topologies with integrated voltage boosting, self-balancing of capacitor voltage self, and a reduced number of device components. SC configurations can be classified into two categories: single-stage and two-stage structures. Single-stage configurations have

several advantages over two-stage configurations, especially the absence of a rear-end H-Bridge. The rear-end H-bridge provides switches with high voltage stress [6, 7]. As a result, high voltage applications are restricted since the backside H-bridge requires switches with a rated voltage that is equal to the peak output voltage. In [8], a single-stage five-level topology was proposed with lower voltage stress and a reduced component count when compared to previous designs. The authors of [9–13] presented multiple cases of five-level topologies. However, these topologies have a limited ability to boost input voltage. Similarly, in [14–17], 5-level topologies employed an increased number of switching components to achieve a voltage gain of two. In [18, 19], a five-level architecture was presented that is deficient in terms of its boosting capability. The authors of [20], proposed a nine-tier topology that used 11 switches and two capacitors to achieve a voltage gain of two. In addition, the topology in [21] can enhance the gain. However, generalized SC structures require more switching components. The authors of [22, 23] proposed a five-level flying capacitor topology that consists of ten switches and four capacitors. In practice, this is less attractive since it has more switching elements. The authors of [24, 25] presented the simplest topology with the smallest number of power components. However, it needs to use two separate dc sources, which severely restricts its application. The configurations in [26–28] allow multilevel inversion while having a high step-up voltage level and a compact design, which is largely due to the switched-diode capacitor cell. However, additional capacitors and diodes were required, and their modulation schemes were complex.

The abovementioned deficiencies were the main reason for developing new single-stage SCMLI architecture with the following unique features.

(a) 2×boosting capability.

(b) The use of a single dc source.

(c) A reduction in the number of switching components.

(d) The capacitor voltage is automatically balanced to ensure proper operation.

(e) Twenty-five percent of the switches are conducting for any generating level other than zero.

(f) It is well suited for low and medium-voltage applications.

2 Proposed topology

2.1 Circuit description

Figure 1 shows the structural design of the five-level SC topology. In the proposed topology, the requirements of the power switches are such that out of eight switches (S_1–S_8), two switches (S_1, S_5) need to be unidirectional-conducting-unidirectional-blocking (*UCUB*), while the remaining switches need to be bidirectional-conducting-unidirectional-blocking (*BCUB*). Five voltage levels ($\pm 2V_{DC}, \pm 1V_{DC}, 0$) are generated by single dc source and two capacitors. Table 1 shows the proper switching pattern at various voltage levels. In this table '0' and '1' symbolize switch OFF and switch ON. The charging and discharging of capacitors are identified by "Δ" and "∇ε, respectively. Capacitors charge in the direction of the red-dotted line, while the blue dotted line represents the path taken to synthesize the voltage level. The terminals *x* and *y* are depicted as the load terminals.$v_{xy}(t)$ shows the load voltage. In Fig. 1, the terminals labeled *x* and *y* are the load terminals.

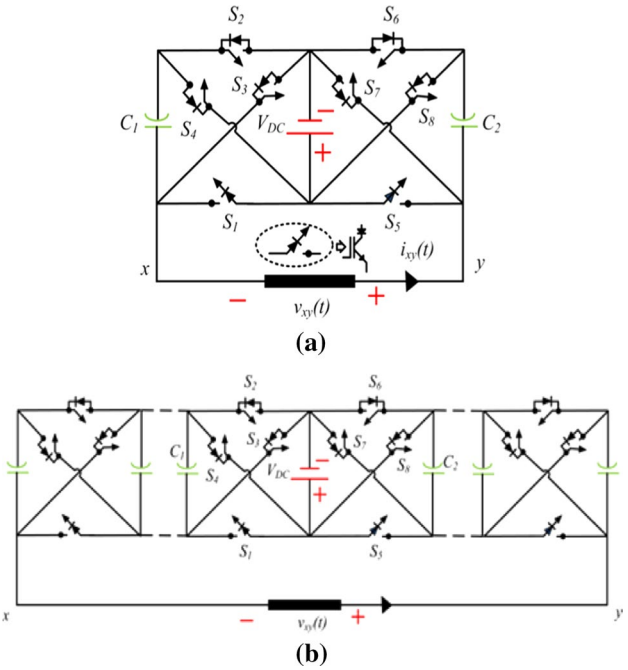


Fig. 1 Structural design of: **a** proposed topology; **b** generalized circuit diagram

2.2 Circuit operation

For better understanding, the equivalent circuits illustrated in Fig. 2a–f are used to describe the operating principle of the proposed topology.

(a) **Level 1** $\boldsymbol{v_{xy}(t) = 0}$
The switches S_1, S_3, S_5, and S_7 can simultaneously turn on to reach this level. Both of the capacitances C_1 and C_2 are charged to V_{DC}. Figure 2a, b depict the direction of the load current as well as the charging route of the capacitors.

(b) **Level 2** $\boldsymbol{v_{xy}(t) = +1V_{DC}}$

Table 1 Valid switching pattern for different voltage levels

L	Active switches								$v_{xy}(t)$	E	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8		C_1	C_2
1	1	1	0	0	1	1	0	0	0	Δ	Δ
2	0	0	1	0	1	1	0	0	$+1V_{DC}$	Δ	Δ
3	0	0	1	0	0	0	0	1	$+2V_{DC}$	–	∇
4	1	1	0	0	0	0	1	0	$-1V_{DC}$	Δ	Δ
5	0	0	0	1	0	0	1	0	$-2V_{DC}$	∇	–

L Level, *E* Effect of capacitor

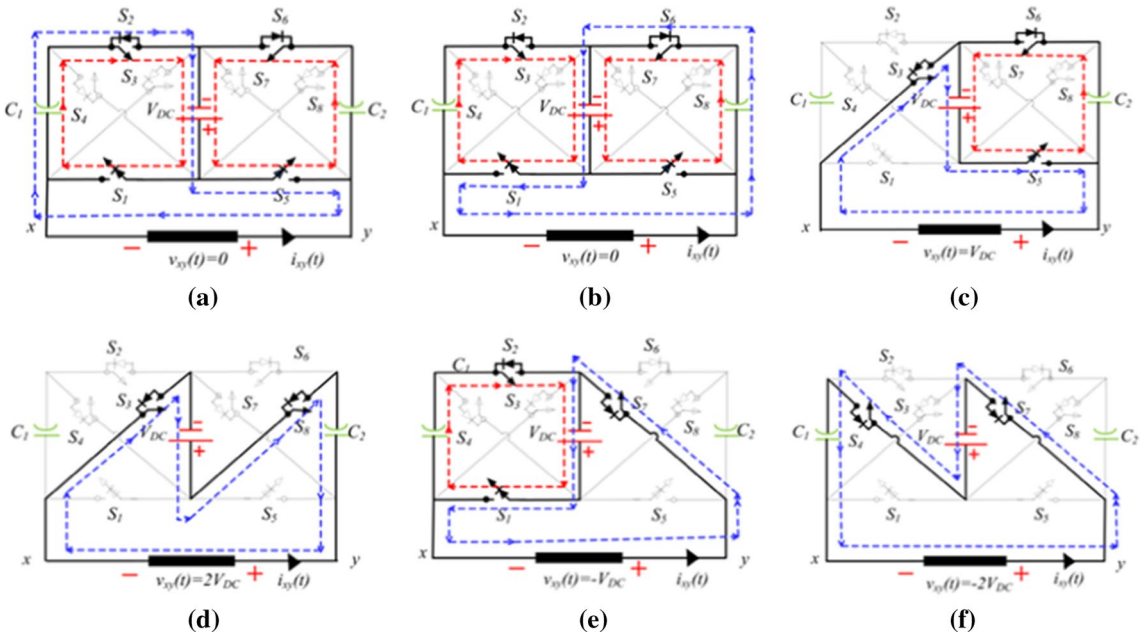


Fig. 2 Different voltage levels of the proposed topology: **a**, **b** $v_{xy}(t) = 0$; **c** $v_{xy}(t) = +1V_{DC}$; **d** $v_{xy}(t) = +2V_{DC}$; **e** $v_{xy}(t) = -1V_{DC}$; **f** $v_{xy}(t) = -2V_{DC}$

To reach this level, make sure the switches S_3, S_5, and S_6 all turn on simultaneously. At this level, the capacitor C_2 is charged to V_{DC}. Figure 2c depicts the direction of the load current and the charging route of the capacitors.

(c) **Level 3 $v_{xy}(t) = +2V_{DC}$**

To reach this level, turn the switches S_3, and S_8 on. The stored energy of the capacitor is transferred to the load along with the voltage V_{DC}. This circuit is represented using the equivalent circuit diagram in Fig. 2d.

(d) **Level 4 $v_{xy}(t) = -1V_{DC}$**

It is possible to attain this level by turning switches S_1, S_2, and S_7 on simultaneously. C_1 is charged to the voltage V_{DC}. An equivalent circuit diagram for this level is shown in Fig. 2e.

(e) **Level 5 $v_{xy}(t) = -2V_{DC}$**

The switches S_4 and S_7 are turned on concurrently for this level. Together with V_{DC}, the capacitor C_1 releases the energy to the load. Figure 2f depicts the equivalent circuit for this particular level.

2.3 Acceptable capacitance design standards

Capacitance has a significant impact on the cost, size, and efficiency of DC/AC converters. In this case, the capacitance needs to be optimized. The capacitance value is calculated using the following parameters. The length of time the capacitor must be discharged before the next charge, the maximum load current, and the tolerable voltage ripple. Thus, capacitors should be chosen to satisfy the following criterion:

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} \tag{1}$$

According to the proposed topology, the discharging amount of the capacitor C_2 can be represented as in [6] so that:

$$\Delta Q_{C2} = \int_{t_1}^{t_2} i_0(\sin 2\pi ft - \varnothing)\mathrm{d}t \tag{2}$$

Considering the modulation index unity, the values of t_1, t_2, t_3, and t_4 can be obtained from the staircase output voltage of the inverter.

$$t_1 = \frac{\sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{3}$$

$$t_2 = \frac{\pi - \sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{4}$$

$$t_3 = \frac{\pi + \sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{5}$$

$$t_4 = \frac{2\pi - \sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{6}$$

where 'f' and 'i_0' represents the fundamental frequency and peak inverter output current respectively. In addition, $\varnothing$ is the power factor angle of the load. Therefore, the required capacitance value can be estimated with a maximum permissible voltage ripple of 10% of the maximum capacitor voltage as:

$$C_2 \geq \frac{\Delta Q_{C2}}{\Delta V_{C2}} \geq \frac{\Delta Q_{C2} = \int_{t_1}^{t_2} i_0(\sin 2\pi ft - \varnothing)\mathrm{d}t}{0.1V_{DC}} \tag{7}$$

The value of C_1 can be assessed in a similar fashion.

2.4 Self-balancing mechanism of capacitors

The switching Table 1 and the voltage levels are shown in Fig. 2a–f demonstrate that the capacitors C_1 and C_2 are charging and discharging as a result of the series/parallel approach [20]. The capacitor C_1 and C_2 are charged to V_{DC} during the level of zero and $\pm 1V_{\mathrm{DC}}$. C_1 dissipates energy during the negative half of the cycle, while C_2 dissipates energy during the positive half of the cycle. This results in an output voltage that is twice the supply voltage. Due to these charging and discharging processes, the capacitors are naturally self-balanced. As a result, the need for a separate circuit to assist the circuit in self-balancing is eliminated.

3 Control strategy

Inverter switching pulses are generated using a variety of control techniques. There are two types of control techniques: low switching frequency and high switching frequency [21]. A universal multicarrier pulse width modulation (PWM) method, as shown in Fig. 3a, has been implemented and tested in this study. Four carrier frequencies ($f_{c1} \sim f_{c4}$) with magnitudes of 2 kHz are constantly compared with the modulating signal of the frequency (f_r) of 50 Hz. Their outputs are combined to produce an aggregated signal $a(t)$. According to Fig. 3a, the aggregated signal is compared with constant using mapped values. Figure 6b depicts the reference signal, the carrier signal, and the output voltage.

4 Power losses analysis

The following section provides information on the switching losses, conduction losses, and capacitor ripple losses associated with the proposed topology. The total power losses (P_T) can be expressed as:

$$P_T = P_{sw} + P_c + P_r \tag{8}$$

4.1 Switching losses (P_{sw})

Switching losses occur when switches are turned on and off. The switching power losses can be expressed mathematically as [21]:

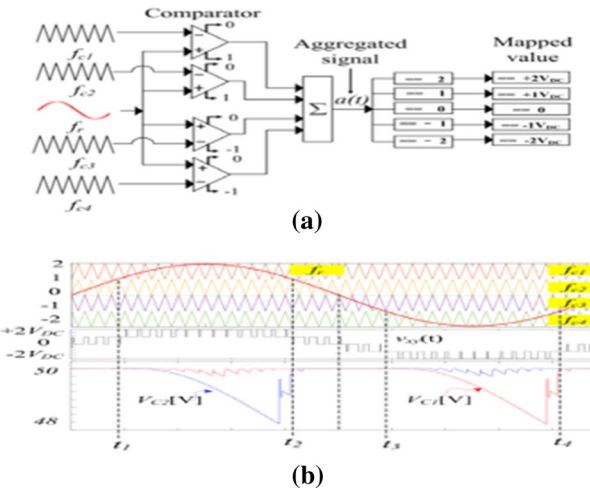


Fig. 3 Diagrams showing: **a** multicarrier PWM control scheme; **b** waveforms of the reference, carrier, output voltage, and capacitors voltage

$$P_{\text{sw}} = P_{\text{sw,on}} + P_{\text{sw,off}} \tag{9}$$

$$P_{\text{sw,on},i} = \frac{1}{6} f V_{\text{on},i} I_{\text{on},i} t_{\text{on}} \tag{10}$$

$$P_{\text{sw,off},i} = \frac{1}{6} f V_{\text{off},i} I_{\text{off},i} t_{\text{off}} \tag{11}$$

$$P_{sw} = \sum_{l=1}^{5} \sum_{i=1}^{8} \left(P_{\text{sw,on},i} + P_{\text{sw,off},i} \right) \tag{12}$$

where $V_{\text{on}}, V_{\text{off}}$ are the voltages across the switches before and after they are turn-on. $I_{\text{on}}, I_{\text{off}}$ are the currents flowing through the switches after turn-on and before the turn off respectively.t_{on}, t_{off} are the turn-on and turn-off time of the switch. f denotes the fundamental frequency.

4.2 Conduction losses (P_c)

The internal resistance of the power switches (R_s) and the diode (R_d) dissipates power when they are in the conduction mode, which results in conduction losses. The losses associated with the power switches and diodes can be expressed as follows [21]:

$$P_{\text{c,sw}} == V_{\text{s,on}} I_{\text{s,avg}} + I_{\text{s,rms}}^2 R_{\text{s,on}} \tag{13}$$

$$P_{\text{c,d}} = V_{\text{d,on}} I_{\text{d,avg}} + I_{\text{d,rms}}^2 R_{\text{d,on}} \tag{14}$$

where $V_{\text{s,on}}$,$V_{\text{d.on}}$ are the on-state voltages of switch and diode, respectively. $I_{\text{s,avg}}, I_{\text{d,avg}}, I_{\text{s,rms}}, I_{\text{d,rms}}$ Specify the average and rms currents of the switch and diode, respectively. As a result, the total conduction losses associated with the proposed topology are:

$$P_{\text{c}} = \sum_{i=1}^{n} \left(\sum_{k=1}^{n} \left(P_{c,sw,i} + P_{\text{c,d},i} \right) \right) \tag{15}$$

where i is the number of switches/diodes, and k is the number of the conduction path.

4.3 Ripple losses (P_R)

The potential difference between the power source and the capacitor during the charging/discharging intervals causes ripple losses in SC inverters. The voltage ripple (ΔV_c) of each capacitor can be expressed as follows [5]:

$$\Delta V_C = \frac{1}{C} \int_{t_a}^{t_b} i_C(t) \mathrm{d}t \tag{16}$$

where $i_C(t)$ is the current flowing through the capacitor during the discharge interval (t_a, t_b). (t_1, t_2) and (t_3, t_4) are the longest discharge intervals of C_2 and C_1 for the proposed inverter. It is then possible to compute the ripple loss associated with a fundamental cycle of the output voltage as:

$$\text{Ripple losses } (P_R) = \frac{f}{2} \sum_{n=1}^{2} \left(C_n \Delta V_{Cn}^2 \right) \tag{17}$$

Consequently, the overall efficiency of the proposed five-level inverter can be represented as:

$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{out}} + P_T} \tag{18}$$

P_{out} is the output power of the proposed inverter.

5 Simulation and experimental results

To ensure the theoretical validity and usability of the suggested topology, it has been tested on both the MATLAB/Simulink program and a hardware configuration. Table 2 presents the simulation and environmental parameters that have been used.

5.1 Simulation outcomes

The proposed topology has been examined theoretically in MATLAB/Simulink under transient conditions. Figure 4a–c show the output voltage, output current, and capacitors voltage under transient conditions. It has been observed that the peak value of the load voltage is two times the supply voltage (i.e., $v_{xy}(t)$ $100V$), and the capacitors maintained their self-balancing effect in all of the cases. Moreover, Fig. 4a shows that the load voltage remains unchanged during a step change in load conditions. Figure 4b shows a change in the switching frequency from 100 Hz to 2 kHz. Figure 4c shows output voltage changes according to the modulation index (0.95–0.5 and 0.5–0.2) and rapidly reached the new state. To determine the switching and conduction losses associated with the proposed model, simulations were performed using PLECS software with a 30Ω pure resistive load.

5.2 Experimental outcomes

With a resistive load of 30Ω, the FFT analysis of $v_{xy}(t)$ results in a rms output voltage of 67.54 V, with a total harmonic distortion (THD) of 11.6%. Similarly, the FFT analysis of $i_{xy}(t)$ reveals a rms current of 2.214 A, with a 5.2% THD. 152, 5.845, 3.465, and 0.4 W represent the total output power, switching losses, conduction losses, and ripple

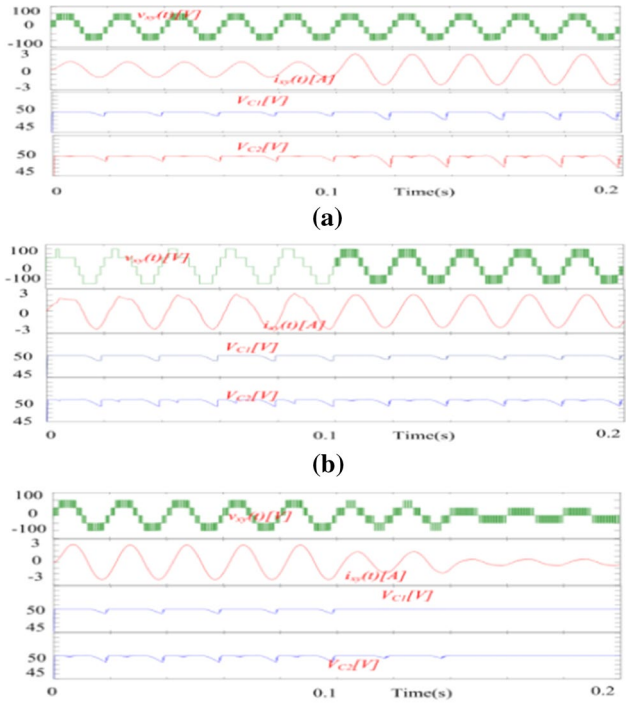


Fig. 4 Simulation results: **a** step change in the load; **b** change in the switching frequency (100 Hz to 2 kHz); **c** change in the modulation index (0.95–0.5, 0.5–0.2)

Fig. 5 Photograph of the experimental setup

losses, respectively. In this case, the efficiency of the inverter is 93%.

A laboratory prototype has been developed to experimentally evaluate the effects and practicality of the proposed five-level SC architecture. The UCUB configuration for the switches S_1 and S_5 is implemented with MOSFETs (IRF640NPBF) with series-connected diodes (MBR30100CT). In this experimental work, for the 8 power switches (S_1–S_8) a total of 8 gate-driver ICs (TLP250) soldered at the back of the PCB with a multi-output (multi-winding) transformer was also employed for electrically isolated supplies. Figure 5 shows the experimental setup designed with the parameters given in Table 2.

(i) *Steady-state analysis* Figure 6a shows the results of experiments in the absence of a load and under steady state conditions. In the absence of a load, it generates a voltage of five levels, and has a maximum value of 100 V. Moreover, a steady-state study was performed for a R–L load (30Ω, 50 mH). Figure 6a shows that the suggested architecture provides five-level voltages with 50 V in each of the steps. The capacitors are self-balanced, and the voltage ripples are minimal.

(ii) *Dynamic response analysis* Dynamic conditions such as a step-change in the load, a change in the switching frequency, and a change in the modulation index are used to assess the performance of the inverter. Results of these dynamic conditions are depicted in Fig. 6b–d. Figure 6b shows a step-change in the loading condition. It can be seen that, despite the abrupt change in load, the voltage level of the system stays unchanged, and the voltage of the capacitors is completely self-balanced. Figure 6c shows that the changes in the switching frequency affect the output voltage and current i.e., when the switching frequency was changed from 100 Hz to 2 kHz, it shows that the output voltage and current quickly respond to the sudden change. The modulation index changing from 0.95 to 0.5 and then back to 0.5 to 0.2 is shown in Fig. 6d. This shows that the inverter completes its transient processes quickly.

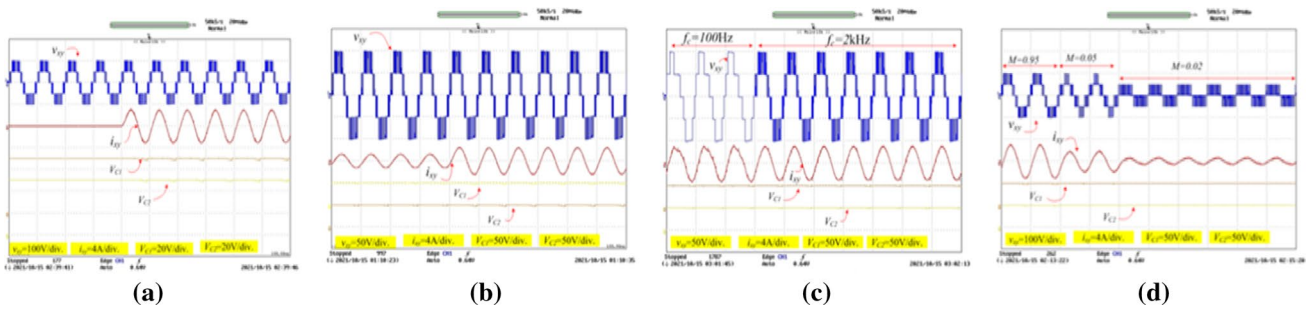
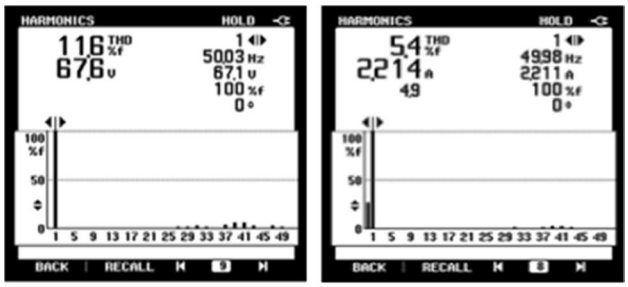


Fig. 6 Experimental results: **a** no load and steady state conditions; **b** step change in the load condition; **c** change in the switching frequency (100 Hz to 2 kHz); **d** change in the modulation index ($M = 0.95$–0.5, 0.5–0.2); **e** voltage stress across a few switches

Table 2 Simulation and experimental parameters

Parameter	Specification
Input voltage V_{DC}	50 V (Keysight N8952A) (0–200 V/0–210A)
Fundamental frequency f_0	50 Hz
Switching frequency	100 Hz, 2 kHz
Capacitor ($C_1 = C_2$)	2000 µF
R–L Load	15Ω, 50 mH, 30Ω, 50 mH,
dSPACE DS 1104	–
MOSFETs	IRF640NPBF 200 V 18A
Diode	MBR30100CT, 100 V 30A
Driver	TLP250



(a) (b)

Fig. 7 FFT analysis of: **a** output voltage; **b** output current

Experimental results of the FFT analysis are displayed in Fig. 7a, b. The efficiency obtained from the experimental setup by a power quality analyzer (fluke 43B) is 92.86%. The obtained efficiency is slightly lower than the findings from the simulation. The test findings coincide with the modeling result, which demonstrates the viability of the proposed structure.

6 Comparative analyses

The merits of the proposed SC topology have been compared with the conventional and prior state-of-the-art topologies in terms of the number of switching components per level factor, total standing voltage, DC source requirements, boosting capability, and cost function. Table 3 includes a comprehensive comparison of several aspects of various designs.

6.1 DC sources

Table 3 shows that the CHB architecture and the architecture in [19] necessitate several dc supply inputs to generate five voltage levels. This ultimately increases the cost and complexity of the circuit by including many input sources. Since the proposed topology needs only one DC source, the circuit design is inexpensive and simple.

Table 3 Comparative analysis with recent SC topologies

Ref	N_l	N_s	N_{sw}	N_c	N_d	N_{dri}	(TSV + PIV) (∗ V_{DC})	Gain	$F_{c/l}$	CF	A
NPC	5	1	8	4	6	8	8	1	5.4	6.8	NO
FC	5	1	8	10	–	8	8	1	5.4	6.8	NO
CHB	5	2	8	2	–	8	8	1	5.6	10.4	NO
[10]	5	1	6	2	2	6	12	2	3.4	5.6	YES
[11]	5	1	6	2	1	6	6	1	3.2	4.2	NO
[12]	5	1	7	3	1	7	13	1	3.8	4.8	NO
[13]	5	1	8	1	2	5	10	1	3.4	5.2	NO
[14]	5	1	8	4	–	8	12	2	4.2	6.4	NO
[15]	5	1	7	2	4	7	9	2	4.2	5.8	YES
[16]	5	1	10	1	1	8	14	2	4.2	6.8	YES
[17]	5	1	8	2	2	7	10	2	4	5.8	YES
[19]	5	2	8	–	–	7	12	1	3.4	10.8	YES
[22]	5	1	12	4	–	12	20	4	5.8	9.6	YES
[26]	5	1	6	2	3	6	9	1	3.6	5.2	YES
[27]	5	1	6	2	2	6	14	2	3.4	6.2	YES
[31]	5	1	8	2	2	8	9	1	4.2	5.8	YES
[P]	5	1	8	2	2	8	12	2	4	6.4	YES

N_l No. of level, N_s No. of source, N_{sw} No. of switches, N_c No. of the capacitor, N_d No. of the diode, N_d No. of the driver unit, *TSV* total standing voltage, *PIV* Peak inverse voltage, $F_{C/L}$ Component count per level, *A* Boosting ability, *P* Proposed topology

6.2 Switching components per level factor

The switching components per level factor $F_{c/l}$ is defined as the relationship between the total number of switching components and the total number of possible voltage levels. This factor can be mathematically expressed as:

$$F_{c/l} = \frac{N_s + N_{sw} + N_c + N_d + N_{dri}}{N_l} \tag{19}$$

This is a proportional factor since it is proportionate to the topologies total cost and overall size. The suggested topology has the benefit of low switching components per level factor when compared to the CHB, NPC, FC, and the topologies in [10–13, 17, 22]. The topology in [11] has the least components per level factor. However, its gain is limited.

6.3 Total standing voltage (TSV)

Total standing voltage is defined as the sum of the blocking voltages of all individual switches. For the creation of the novel multilevel inverter architecture, this is extremely important. The topologies in [22, 27] have higher values of TSV + PIV. When compared to the proposed topology, the topologies [9–11, 13, 15, 17, 26, 32] have a comparatively low total standing voltage. However, other factors such as the absence of boosting capability and the high component count per level factor make them less attractive and economical.

6.4 Voltage boosting capability

The quality of the power is determined by the THD. It also serves the needs of various interconnection systems such as renewable grid systems, electric vehicles, and so on. In Table 3, it can be seen that the traditional topology and the topologies in [9–14, 19, 26, 32] are unable to increase the input voltage. Therefore, electric cars cannot use these topologies.

6.5 Cost function

This section is crucial for evaluating the overall cost since it allows for the assessment of the overall cost. The switching components and the total standing voltage ($TSV + PIV$) are closely related to the cost function and are expressed as (20):

$$\mathrm{CF} = \frac{(N_{sw} + N_c + N_d + N_{dri} + \propto (TSV + PIV)}{N_l} \times N_s \tag{20}$$

When the TSV and switching components are given equal significance, the value of $\propto$ is one, and when the switching components are given more priority, the value of $\propto$ is larger than one, and vice versa. For the proposed topology $\propto$ is treated as a single entity. Except for [10–13, 15, 26, 27], it is clear from Table 3 that the total cost of the proposed structural design is projected to be modest.

7 Discussions of findings and applicability

As demonstrated by the simulation and experimental results for the proposed architecture, a five-level waveform with twice the voltage gain is generated. The chosen values ensure that the capacitors operate satisfactorily in terms of voltage ripples at a full load. The power loss distribution in the switches indicates that the proposed topology is more efficient. In terms of possible applications for the suggested topology, the following have been found based on a review of the literature on SCMLIs.

7.1 High-frequency ac distribution

The high-frequency alternating current (HFAC) power distribution system (PDS) has become increasingly popular in high-power density applications such as telecommunication, spacecraft, and computer systems due to its significant reduction in the number of power conversion stages [28], transformer size, and filter size. The use of a HFAC PDS in small-scale networks such as micro grids, buildings [29], and electric vehicles [24] is another new application for this technology. Due to the capacitor voltage imbalance difficulties in these applications, standard multilevel topologies with more than five levels are less feasible [30]. Thus, SCMLIs have become a preferred choice for HFAC applications [8]. SCMLI topologies reduce the need for magnetic circuits or dc-dc boost converters at low voltage sites.

7.2 Photovoltaic (PV) based power generation systems and electric vehicle (EV) traction system

The power available through renewable energy, such as photovoltaic systems, is relatively low. Voltage boosting is achieved either by cascading PV modules, using a dc-dc boost inverter, or using a step-up transformer. All of these technique increases the number of components, costs, volume, and power losses [31]. However, the use of SCMLIs provides a good voltage gain, capacitor self-balancing, high-resolution waveforms for grid compatibility, and decreased filtering requirements [32].

8 Conclusion

A new innovative SC multilevel inverter with five voltage levels and a lower device count was presented in this article. In-depth descriptions of the topological design, operation, and power losses were provided. A simple logic-based PWM technique was implemented to provide a smooth control approach. The proposed architecture can include a small number of switching components, a self-balancing capacitor voltage, and a low-cost function. The advantages of the proposed topology over prior state-of-the-art topologies were shown via comparative investigations. Proofs of the concept were given with experimental results that show good agreement with MATLAB/Simulink findings, which indicates the efficacy and practicality of the proposed topology.

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