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ORIGINAL ARTICLE

Comparison of junction temperature variations of IGBT modules under DC and PWM power cycling test conditions

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Abstract
This paper presents an experimental investigation and a finite element (FE) analysis study on the thermal and mechanical behaviors of insulated-gate bipolar transistor (IGBT) power modules under various operating conditions. The power cycling test conditions are provided by two test benches, a direct current (DC) test bench and a pulse width modulation (PWM) test bench. Infrared (IR) camera acquisition methods are suggested as an approach for transient temperature measurements to estimate the effects of operating conditions and switching frequency on the thermal performance of an IGBT module. An electrical–thermal–mechanical FE model of an IGBT module is employed to determine the stress in the interconnections of an IGBT module induced by junction temperature fluctuations. Results indicate that the operating conditions significantly impact the maximum junction temperature, the junction temperature increase rate, and the junction temperature distribution of an IGBT chip and the thermally induced stress in the interconnections. The switching frequency strongly impacts the junction temperature of an IGBT chip, and the maximum junction temperature increases when the switching frequency increases due to the increasing switching loss. Furthermore, the junction temperature variation induced by the instantaneous switching loss is estimated by the proposed IR camera measurement method.

Keywords IGBT module · Power cycling test · Infrared (IR) camera measurement · Junction temperature

1 Introduction

Power semiconductor devices, such as insulated gate bipolar transistors (IGBTs) and power VDMOS transistors, are core elements of the electric drive systems used in electric vehicles, railway traction systems, as well as aerospace and renewable energy applications [1, 2]. Thus, it is worth paying attention to their reliability [3]. For high-power IGBT modules, the junction temperature (T_j) is a key parameter that impacts the reliability performance and critically affects the lifetime of IGBT modules [4, 5]. Some studies [6, 7] have shown that approximately 60% of the failures of power semiconductor devices are temperature-induced. Therefore, knowledge about junction temperature variation during IGBT module operation is of great interest.

The temperature measurement methods employed to estimate the junction temperatures of IGBT modules can be broadly divided into three general categories: physical contact, electrical, and optical measurement methods [8]. The physical contact measurement method requires direct contact with the surface of the power chip, and can only provide a local temperature [9]. The electrical method applies temperature-sensitive electrical parameters (TSEPs), such as the on-state collector-emitter voltage ($V_{CE\text{-}ON}$) under a low current [10], the gate-emitter voltage ($V_{GE,I}$) [11], the saturation current (I_{sat}) [12], and the peak gate current ($I_{G,peak}$) [13], to evaluate the junction temperatures of IGBT modules. TSEP-based measurements are currently the only way to achieve rapid measurements in periods of less than a hundred microseconds. However, this method only provides an average junction temperature for a power device. The optical method requires mechanical access to the power chip. Thus, it cannot be performed without modification to the structure of the power module. The main optical temperature

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indicators are optical fibers [14], local infrared (IR) sensors [15], IR microscopes [16], and IR cameras [13].

IR camera measurements have been widely used to obtain the junction temperature distribution and the maximum junction temperature of IGBT chips under power cycling conditions. The authors of [13] used an IR camera to assess the accuracy of a TSEP-based method for IGBT junction temperature measurements. Gao et al. [17] applied an IR camera to evaluate the changes in the temperature gradient of IGBT chips under direct current (DC) power cycling conditions. Czerny et al. [18] measured the junction temperature of an IGBT module under pulse width modulation (PWM) power cycling conditions, and found that a high operation frequency can induce periodic junction temperature fluctuations on an IGBT chip.

One disadvantage of IR cameras is that the measurement time cannot be lower than 1 ms due to limits imposed by the instrumentation response time and the response time of optical phenomena to changes in temperature. Thus, if the frequency of the temperature change is faster than the sampling frequency of the IR camera, it is nearly impossible to determine the temperature fluctuation. In some applications, such as electric vehicles, a real IGBT inverter generally works under PWM operating conditions, and the operation frequency usually ranges from 1 to 300 Hz. Furthermore, the pulse frequency of the current that flows over an IGBT module under switching conditions can range from 5 to 30 kHz. The current induces short heating and cooling periods, which results in periodic junction temperature variations on an IGBT chip. This variation in the junction temperature is a source of thermomechanical stress in the interconnects within IGBT modules and can eventually lead to fatigue failures and malfunctions in power modules [19]. Thus, it is necessary to improve the IR camera measurement method to obtain a junction temperature map of an IGBT chip under fast switching conditions, and to clarify the factors that influence thermomechanical stress.

In this paper, both DC and PWM power cycling test benches are introduced. Then details of the IR camera measurement methodology, which can record the junction temperature data of IGBT chips under various operating conditions, are provided. Based on the proposed IR camera measurement approach, the effect of the switching frequency on the junction temperature of IGBT chips can be examined, and a quantified correlation between the switching loss and junction temperature variation of an IGBT chip is determined.

2 Test bench and methods

2.1 Tested IGBT modules

The typical electrical ratings of the considered IGBT module are 1200 V/450 A [20]. Figure 1a shows a photograph of the tested IGBT module with the chips labelled in consecutive order. The IGBT module consists of two identical sections, an upper and a lower half bridge, and each section has three IGBT chips and three diodes. In each half bridge, the chips are connected in parallel. The IGBT module was manufactured utilizes the most current assembly technology. It uses a direct copper bonded (DCB) substrate to function as an electrical insulator, current channels, and a thermal conductor. In addition, it uses bond wires to achieve interconnections between chips, the DCB substrate, and terminals, as shown in Fig. 1b.

To directly monitor the junction temperature with an IR camera, an IGBT module without silicone gel was customized by the manufacturer. In addition, to obtain homogenous emissivity across the surface of the chip, both the bond wires and chips were painted with black paint.

2.2 Power cycling tests

Figure 2 shows the power cycling test bench, which included a power supply system, a control and synchronization system, a drive system, a data acquisition system, a data storage and analysis system, and an infrared thermal image acquisition system [21]. Both constant DC and PWM load experiments can be performed on this bench. Circuit diagrams of the DC and PWM power cycling test are presented in Fig. 3.

(1) DC test bench

Figure 3 shows the test circuit with one module and one rectifier-filter circuit in series. A DC waveform is applied to the gate of the device under test (DUT) to maintain the DUT conditions. The DC test bench conditions are indicated in

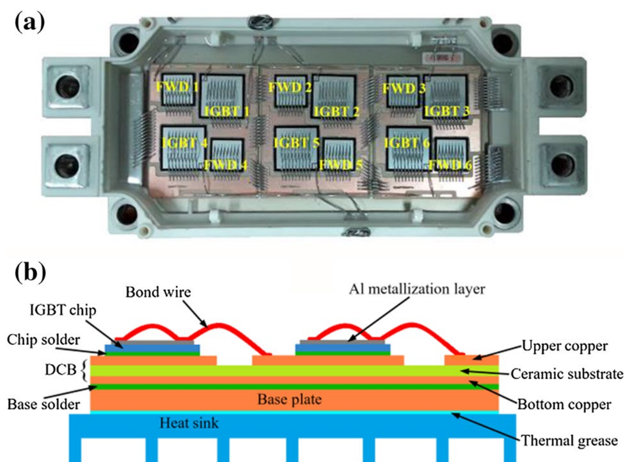

Fig. 1 IGBT module under investigation: **a** view of an IGBT module; **b** cross-sectional schematic of an IGBT module

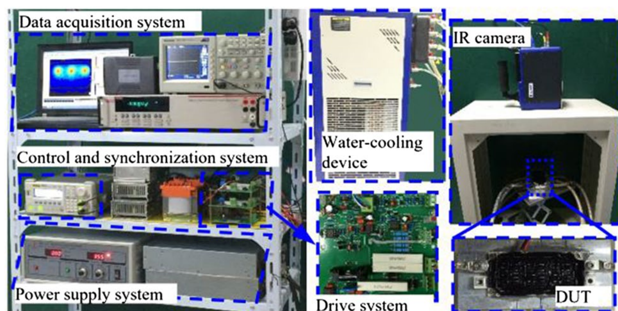

Fig. 2 Prototype test bench

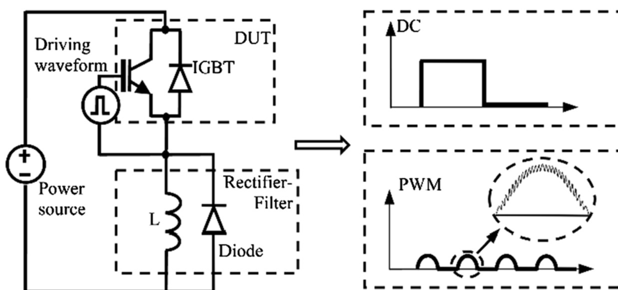

Fig. 3 Configuration of power cycling test

Table 1. The collector current (I_C) for the tests is set to 140 A. The cycle periods are 8 s, 0.05 s, and 2×10^{-4} s.

(2) **PWM test bench**

As shown in Fig. 3, for each specific PWM test, the IGBT switching frequency is certain, and a periodic change in the duty cycle is applied to the gate, which can generate a loading current in the shape of a 40 Hz positive sinewave. To obtain results comparable to those from the DC test bench, the peak of the sine current is set to 200 A, which makes the rms current equal to 140 A. The PWM test bench conditions with different IGBT switching frequencies are also indicated in Table 1.

(3) **Measurements**

Two common parameters, the collector current (I_C) and the temperature of the base plate bottom (T_c), are captured by a data acquisition system and transmitted to a computer for storage and further analysis for both DC and PWM tests. In addition, $V_{CE\text{-}ON}$ is monitored by imposing a constant current of 100 mA on the DUTs during t_{off}.

Table 1 Test conditions of power cycling tests

Condition	Waveform of the loading current	DC current (A)	f_{sw} (Hz)[a]	$\delta = t_{on}/(t_{on}+t_{off})$[b]	t_{on} (s)[c]	t_{off} (s)[d]
DC-I	I_C; $1/f_{sw}$; t_{on}; t_{off}; $I_{C,max}$; $\delta = t_{on}/t_{off}$; t	140	0.125	0.5	4	4
DC-II		140	20	0.5	0.025	0.025
DC-III		140	5 k	0.5	1×10^{-4}	1×10^{-4}
Condition	Waveform of the loading current	Max/RMS current (A)	f_{sw} (Hz)	f_{op} (Hz)[e]	t_{on} (s)	t_{off} (s)
PWM-I	I_C; t_{on}; t_{off}; $I_{C,max}$; $1/f_{op}$; t; I_C; t_{on} t_{off}; $1/f_{sw}$; $I_{C,max}$; t	200/140	10 k	40	4	4
PWM-II		200/140	5 k	40	0.025	0.025
PWM-III		200/140	10 k	40	0.025	0.025

[a]Switching frequency
[b]Duty cycle
[c]Power-on duration
[d]Power-off duration
[e]Operation frequency

2.3 IR camera measurements

The IR camera used here is a FLIR SC7300M [13]. All of the infrared measurements were performed at a sampling frequency of 200 Hz with a resolution of 320 × 240 pixels.

(1) Triggering and synchronization

The maximum junction temperature ($T_{j,max}$) is the most important parameter from a reliability point of view [22]. To capture the maximum value of the junction temperature of an IGBT module under power cycling, the measurement should be carried out at the exact power-off moment. However, the time interval between the time when the loading current stops and the time when the IR camera takes a measurement introduces an error to the acquired junction temperature results since the generated heat can diffuse away in a few milliseconds [23].

A synchronous trigger system is used in this study to overcome this time interval problem. A function/arbitrary waveform generator is applied to independently provide outputs to two pulse channels. One triggering signal is sent to the IR camera, and the other switching signal is used to control the switch of the tested IGBT module. These two signals are completely synchronized. A timing diagram of the two signals is shown in Fig. 4.

The trigger system provides effective matching between the time of the thermal transient event and the image acquisition. This means that it is possible to identify the transient junction temperature of the IGBT chip at any moment during the power cycling tests.

(2) Multiple time-delayed acquisition

An IGBT module is heated by pulsed currents. Thus, the junction temperature is periodically repeated. Here, a multiple time-delayed acquisition method is applied to provide full frame measurements of the replicable junction temperature [24]. Figure 5 presents the timing sequence. Meanwhile, Fig. 5a gives the replicable junction temperature profile, injected loading current, and image acquisition timing, while Fig. 5b presents the reconstructed junction temperature profile. The operation frequency of the PWM power cycling tests is f_{op}. Thus, the temporal duration of one heating cycle is $D = 1/f_{op}$, and the sampling frequency of the IR camera is f_{sam}. N images are acquired during one heating cycle:

$$N = D \cdot f_{sam}. \tag{1}$$

During the test, the synchronous trigger system starts image acquisition and synchronously turns on the IGBT module. Thus, the junction temperature T_1 at time t_1, the junction temperature T_2 at time t_2, …, and the junction temperature T_N at time t_N can be obtained during the first heating cycle. Then a time delay Δt is introduced into the timing sequence of the triggering signals during the next heating cycle.

The relationship between the required equivalent sampling frequency (f_{eq}) and the time delay Δt can be expressed as:

$$\Delta t = \frac{1}{f_{eq}}. \tag{2}$$

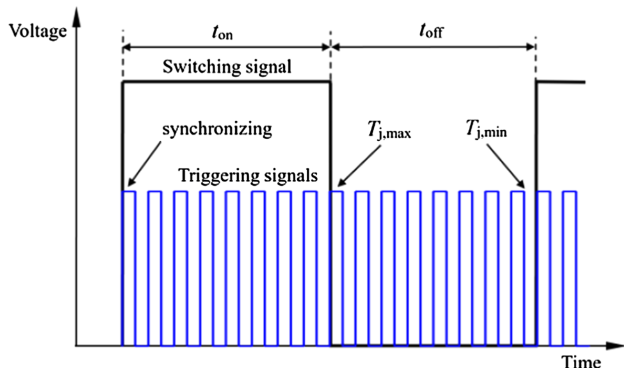

Fig. 4 Timing diagram of the triggering signal and the switching signal

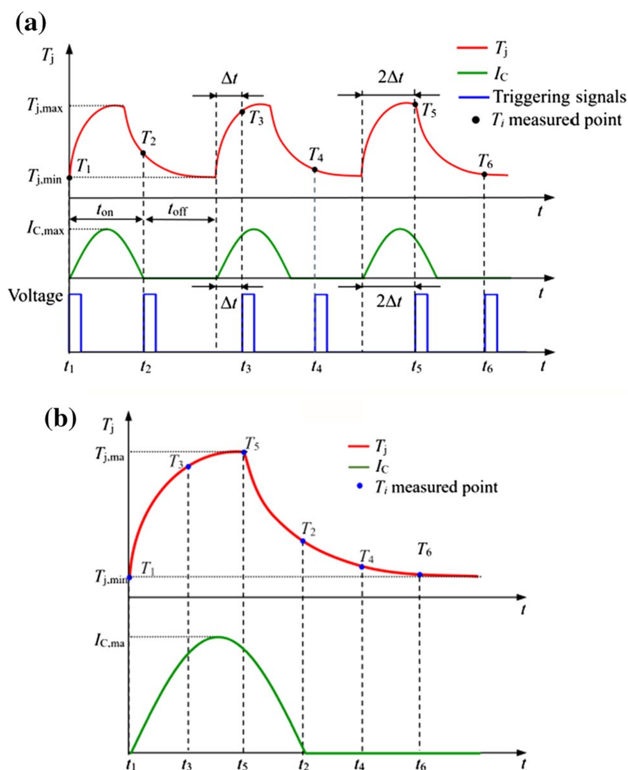

Fig. 5 Multiple time-delayed acquisition method: **a** replicable junction temperature profile, injected loading current, and image acquisition timing; **b** reconstructed junction temperature profile

Furthermore, the number of iterations, M, can be represented as:

$$M = \frac{f_{eq}}{f_{sam}} \text{ or } M = \frac{1}{f_{sam} \cdot \Delta t}. \tag{3}$$

If Δt shifts for each iteration, the junction temperature must be replicated M times to complete the profile reconstruction. At the end of the measurement process, all of the acquired time-delayed frames are used to reconstruct the time-domain infrared sequence, as shown in Fig. 5b.

(3) Integration time controlling

The minimum period required to create an image is equal to the integration time (IT) and the amount of time required to build the image (post-processing). The range of the integration time should be chosen to match the temperature of the scene to be imaged. Here, the junction temperature range of the IGBT module to be measured is approximately 20–150 °C during power cycling tests. Thus, the integration time can be set between 800 and 2000 μs in increments of 1 μs. The maximum sampling frequency ($f_{sam,max}$) for acquiring images is limited by the integration time of the IR camera.

$$f_{sam,max} = \frac{1}{\text{IT} + \text{Post - processing}}. \tag{4}$$

The IR camera cannot directly acquire the temperature variation if the temporal duration of the thermal transient is smaller than the IR camera integration time. To investigate the junction temperature fluctuations of the IGBT module during one switching cycle, a method is proposed that adjusts the integration time of the IR camera, which allows the temperature variation measurement to occur within a temporal duration that is smaller than the integration time, as shown in Fig. 6.

The switching frequency of the IGBT module is 5 kHz, and the temporal duration of one switching cycle is 200 μs. First, an integration time of 800 μs is used, and the flow of photons within four switching cycles is received by the camera. Then an integration time of 1000 μs is used, and the IR camera can record photons over five switching cycles. The junction temperature increments during one switching cycle can be obtained by the difference between the two measured junction temperatures.

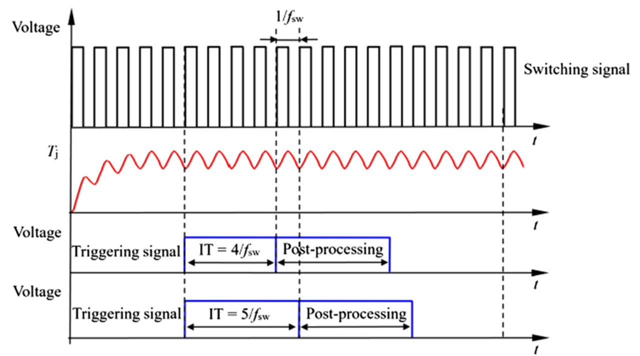

Fig. 6 Time period diagram of the IR camera

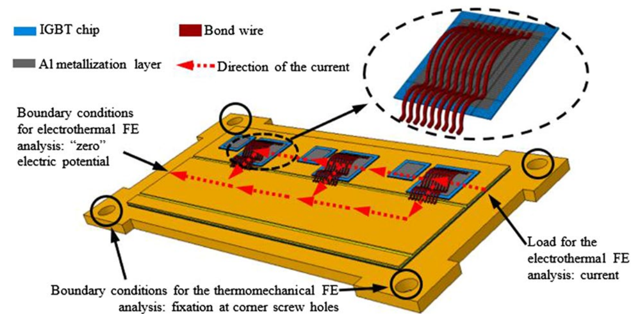

Fig. 7 3D FE model of an IGBT module

3 Finite element modeling process

3.1 Finite element model

Figure 7 illustrates a 3D FE model established based on the test sample, and the model consists of three IGBT chips, three diode chips, an Al metallization layer, chip solder, a DCB substrate, base solder, a base plate, and bond wires. Nine bond wires for each of the IGBT chips are connected to the Al metallization layer and the upper copper layer of the DCB. The dimensions of the model are the same as those of the test sample, which are listed in Table 2. A fine mesh is defined using 8-node linear brick elements, and the model included 562,995 elements and 660,531 nodes.

3.2 Electrothermal finite element analysis

First, an electrothermal FE analysis is performed to obtain the junction temperature distribution of the IGBT module. Here, eight-node linear coupled thermal–electrical elements (DC3D8E-type) are used in the simulation. Table 3 lists the material properties applied in the electrothermal FE analysis. The electrical resistivity of the IGBT chip is temperature dependent, as shown in Fig. 8. The other material properties, including thermal conduction, electrical resistivity, density, and specific heat, are set as constants.

For the electrothermal FE analysis, electrical current is injected in the loading region. The current flows through the upper copper layer, the chip solder, the IGBT chip, the Al metallization layer, and the bond wires and into the output zero potential region, as shown in Fig. 7. Heat is generated at the IGBT chips. Then it dissipates throughout

Table 2 FE model geometry parameters

	Length (mm)	Width (mm)	Thickness (mm)
IGBT chip	13	13	0.20
Diode chip	8	8	0.20
IGBT chip Al metallization layer	11	11	0.004
Diode chip Al metallization layer	6	6	0.004
IGBT chip solder	13	13	0.15
Diode chip solder	8	8	0.15
Upper copper layer	–	–	0.30
Ceramic substrate	98	44	0.38
Bottom copper layer	98	44	0.30
Base solder	98	44	0.15
Copper base plate	120	60	3.00

Table 3 Material properties in the electrothermal FE analysis

Materials	Thermal conduction (mW/mm K)	Electrical resistivity (mΩ mm)	Density (kg/m^3)	Specific heat (J/kg K)
Aluminum	237	2.65×10^{-2}	2.70×10^{3}	900
Silicon (IGBT)	148	Temperature-dependent	2.33×10^{3}	700
Solder (SAC305)	57	1.04×10^{-1}	7.30×10^{3}	230
Al_2O_3	20	1×10^{18}	3.96×10^{3}	753
Copper	400	1.68×10^{-2}	8.92×10^{3}	380

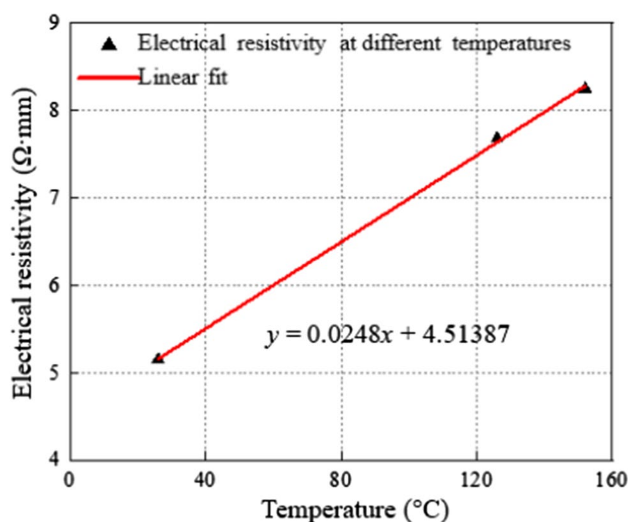

Fig. 8 Electrical resistivity vs. temperature for the IGBT chip

the entire IGBT module. The effect of the cooling system is taken into account in the FE simulation by forcing convection boundary conditions on the bottom face of the model. A convection coefficient of 40 W/(m^2 °C) is used on all of the other external faces to simulate natural heating loss due to convection with ambient air. Both the ambient temperature and the stress-free temperature of the model are set to 23 °C.

3.3 Thermomechanical finite element analysis

A thermomechanical FE analysis is numerically performed. Eight-node linear brick elements with reduced integration (C3D8R-type in ABAQUS) are used in the simulation. The linear elastic material properties, Young's modulus E, Poisson's ratio ν, and CTE α, of the materials used in the finite element model are listed in Table 4.

During the thermomechanical FE analysis, the thermal results obtained from the analysis are imported as the load in the thermomechanical simulation. All of the nodes at the screw holes of the IGBT module are fixed for all degrees of freedom since the boundary conditions should represent those used in the power cycling test. Here, the stress is completely thermally induced since the IGBT module is not subjected to any mechanical loading.

4 Results and discussion

4.1 Comparison of the junction temperatures obtained using $VCE_{\text{-ON}}$, an IR camera, and FE analysis

$V_{\text{CE-ON}}$ has generally been used for many decades as a TSEP to measure the junction temperature of IGBT modules [25, 26]. For junction temperature measurements based on

Table 4 Material properties in the thermomechanical FE analysis

Material	*E* (GPa)	*ν*	*α* (ppm/°C)
Aluminum	70.6	0.33	21
Silicon (IGBT)	112	0.22	2.5
$Sn_{3.0}An_{0.5}Cu$ (solder)	10.6	0.35	22.4
Al_2O_3 (substrate)	300	0.22	6.4
Copper	100	0.34	16.4

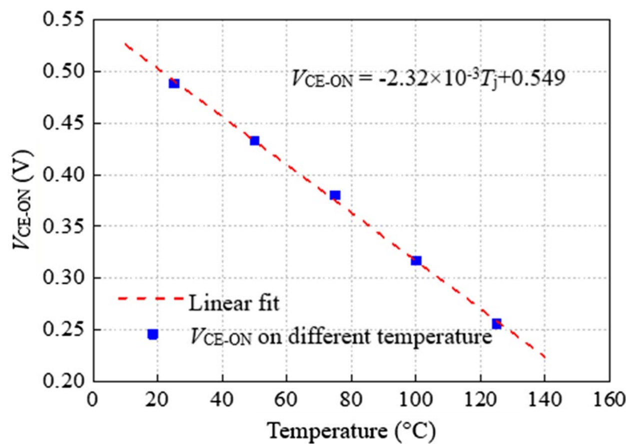

Fig. 9 Calibration curve of $V_{CE\text{-}ON}$ and T_j for the IGBT module

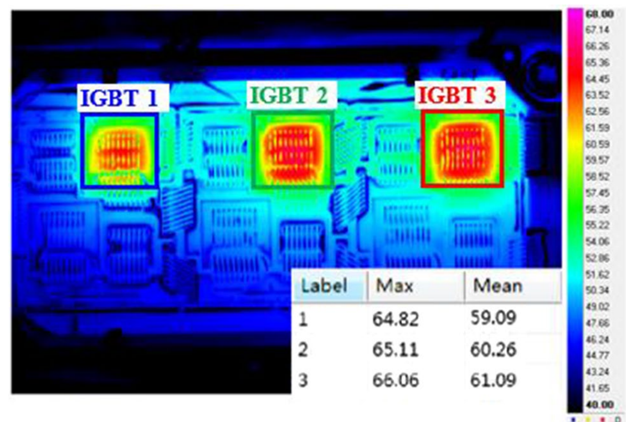

Fig. 10 IR imaging of the IGBT module at the power-off moment under the DC-I test condition

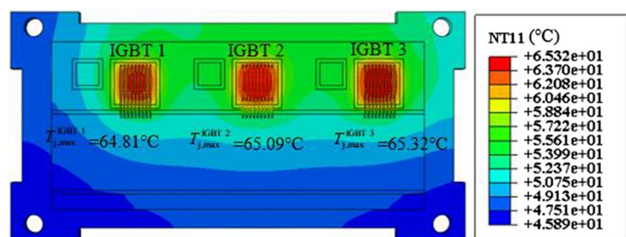

Fig. 11 Predicted temperature distribution of the IGBT module at the power-off moment under the DC test condition using FE analysis

$V_{CE\text{-}ON}$, a preliminary calibration is essential to obtain the dependence of the junction temperature on the voltage. As can be seen in the characterization curve of the IGBT module shown in Fig. 9, $V_{CE\text{-}ON}$ displays a nearly linear relationship with the junction temperature, and the temperature sensitivity is approximately − 2.32 mV/°C.

Figure 10 presents an infrared image acquired at the power-off moment under the DC-I test condition. The entire IGBT module with three operating IGBT chips is recorded in one image, and the individual IGBT chips can be clearly recognized. The maximum junction temperatures reached during the power cycle for IGBT 1, IGBT 2, and IGBT 3 are 64.82 °C, 65.11 °C, and 66.06 °C, respectively. Then, processing software is used to average the temperatures measured over the individual IGBT chips. The mean junction temperatures for the three chips are 59.09 °C, 60.26 °C, and 61.09 °C, respectively. The junction temperature distribution on the surface of the IGBT chip is not uniform. The junction temperature in the central region of the IGBT chip is clearly higher than that in the peripheral region. Thus, the measured average junction temperature across the IGBT chip surface is slightly lower than the spot junction temperature in the central region of the IGBT chip.

Using the established FE model, an electrothermal FE analysis was initially performed. Figure 11 gives the junction temperature distribution of the IGBT module based on the electrothermal FE analysis under the DC test condition. The junction temperature distribution in the IGBT chips predicted by the FE analysis corresponds to that obtained from the IR camera measurement. At power-off, the maximum junction temperature is located in the center of the IGBT chip, and the values for IGBT 1, IGBT 2, and IGBT 3 are 64.81 °C, 65.09 °C, and 65.32 °C, respectively.

Table 5 gives junction temperature results estimated by TSEP measurement, IR camera measurement, and FE analysis. The junction temperature value given by the TSEP-based measurement (T_j^{TSEP}) is in good agreement with the mean junction temperature obtained with the IR camera measurement ($T_{j,mean}^{IR}$). The differences between the T_j^{TSEP} and $T_{j,mean}^{IR}$ values for each of the IGBT chips are less than 2 °C. In addition, the T_j^{TSEP} value is very representative of the mean junction temperature of the three IGBT chips, with errors lower than 1 °C. These results are in accordance with several previous studies [13], which suggests that the TSEP-based method can provide an adequate assessment of the mean junction temperature of IGBT chips in a parallel. However, a comparison of T_j^{TSEP} in relation to the peak value obtained by the IR camera measurement ($T_{j,max}^{IR}$) for each of the IGBT chips shows that T_j^{TSEP} clearly underestimates the maximum junction tempera-

Table 5 Junction temperature measurement results

	T_j^{TSEP}(°C)	$T_{j,mean}^{IR}$(°C)	Error $T_{j,mean}^{IR}$ -T_j^{TSEP} (°C)	$T_{j,max}^{IR}$(°C)	Error $T_{j,max}^{IR}$ -T_j^{TSEP} (°C)	$T_{j,max}^{FE}$(°C)	Error $T_{j,max}^{IR}$ -$T_{j,max}^{FE}$ (°C)
IGBT 1	59.58	59.09	− 0.49	64.82	5.24	64.81	0.01
IGBT 2		60.26	0.68	65.11	5.53	65.09	0.02
IGBT 3		61.09	1.51	66.06	6.48	65.32	0.74
Average		60.15	0.57	–	–	–	–

ture of the IGBT chips, and gives results with the largest errors, i.e., more than 5 °C. The error percentage for the maximum junction temperature obtained from the FE analysis ($T_{j,max}^{FE}$) relative to that obtained from the IR camera measurement is less than 1.12%. The small differences between the results confirm that the convection coefficients and external temperatures are well defined in the FE analysis.

These results suggest that TSEP measurements based on $V_{CE\text{-}ON}$ can only provide a mean junction temperature for IGBT chips and cannot provide the peak junction temperature. The maximum junction temperature can be obtained by an IR camera or FE analysis.

Figure 12 compares the junction temperatures in the central region of IGBT 2 chip obtained from FE analysis and IR camera measurement under the DC-I test condition. The simulation results are in good agreement with the IR camera measurement results, and the results differ by 2–8% during the power cycle. The junction temperature difference between the FE analysis and the IR camera measurement results may be caused by the inadequate heat dissipation capacity of the cooling system used in the power cycling test.

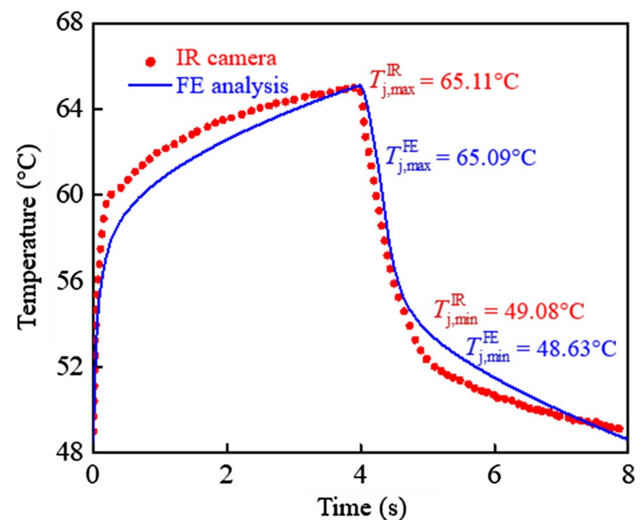

Fig. 12 Comparison of the temperatures from IR camera measurements and FE analysis for the central region of the IGBT 2 chip under the DC test condition

4.2 Effect of test conditions (DC vs. PWM) on the junction temperature of an IGBT Chip

To compare the junction temperature results for different operating conditions, two power cycling tests were conducted under DC-I and PWM-I test conditions. The difference between the two test conditions is that a half sine current with a 40 Hz operation frequency and a 10 kHz switching frequency is applied in the PWM-I test.

Figures 13 and 14 display the junction temperature evolution of IGBT 2 chip in one power cycle, when the steady state is achieved, under the DC-I test condition and under the PWM-I test condition, respectively. The time evolution of the junction temperature at different test positions under the DC-I test condition is shown in Fig. 13a, i.e., A—the central point of the IGBT chip, B—the point near the bond wire heel, and C—the corner point of the IGBT chip. The time evolution of the junction temperature at the different test positions under the PWM-I test condition is acquired, as shown in Fig. 14a, i.e., D—the central point of the IGBT chip, E—the point near the bond wire heel, and F—the corner point of the IGBT chip.

The trend of the junction temperature profile under the PWM-I test condition is quite similar to that observed under the DC-I test condition. Figures 13a and 14a show that in the initial heating phase (0–0.1 s), the junction temperature increases significantly at all of the test positions. During the next heating phase (0.1–4 s), the junction temperature for all of the test positions increases until it reaches its peak value. The rate of increase is approximately the same at the three positions. However, the rate is apparently lower than that observed in the initial heating phase. The maximum junction temperatures occur at the central point of the IGBT chip. After $t = 4$ s, i.e., when the power is disconnected, the junction temperature of the IGBT module decreases due to the cooling system.

Nevertheless, some obvious differences in the junction temperature results for the two test conditions can be observed. First, the maximum junction temperature that can be reached under the PWM-I test condition is far from that achieved under the DC-I test condition. In the PWM-I test, the maximum junction temperatures for the three test positions are 90.30 °C at test point *D*, 82.38 °C at test point *E*, and 73.85 °C at test point *F*. The mean and maximum junction temperatures of the IGBT chip in the PWM-I test are

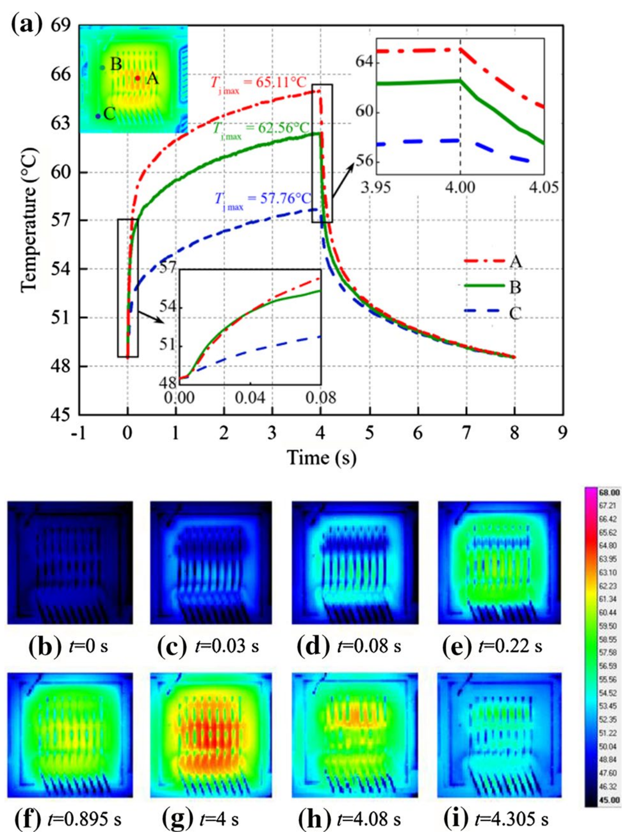

Fig. 13 Temperature evolution in the IGBT 2 chip over time under the DC-I test condition: **a** temperature evolution at different test positions of the IGBT chip. Temperature distribution of the IGBT chip at: **b** $t=0$ s; **c** $t=0.03$ s; **d** $t=0.08$ s; **e** $t=0.22$ s; **f** $t=0.895$ s; **g** $t=4$ s; **h** $t=4.08$ s; **i** $t=4.305$ s

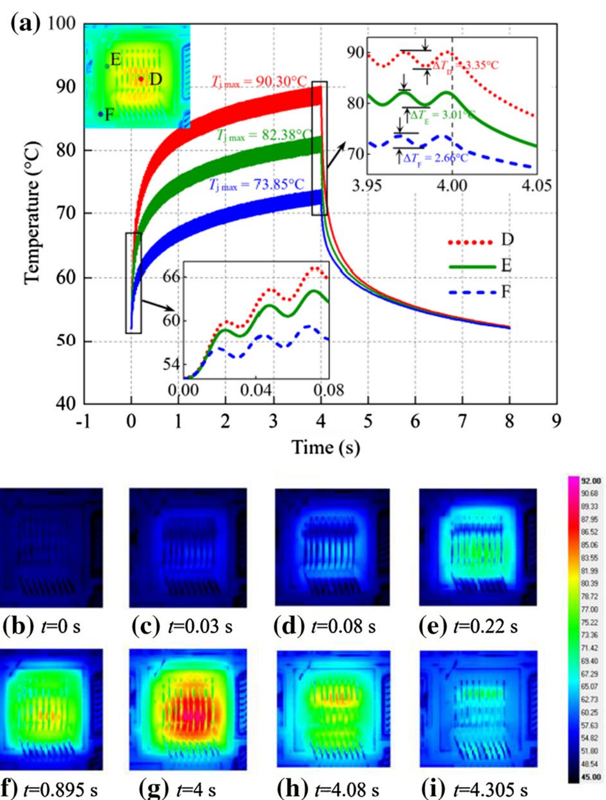

Fig. 14 Temperature evolution in the IGBT 2 chip over time under the PWM-I test condition: **a** temperature evolution at different test positions of the IGBT chip. Temperature distribution on the IGBT chip at: **b** $t=0$ s; **c** $t=0.03$ s; **d** $t=0.08$ s; **e** $t=0.22$ s; **f** $t=0.895$ s; **g** $t=4$ s; **h** $t=4.08$ s; **i** $t=4.305$ s

approximately 15–25 °C higher than those of the IGBT chip in the DC-I test. Since the rms current in the PWM-I test is fixed at 140 A, which is equal to that in the DC-I test, this junction temperature difference is clearly due to switching power loss.

Second, the junction temperature evolution over time under the PWM-I test condition, shown in Fig. 14a, does not monotonically increase like that under the DC-I test condition, as shown in Fig. 13a. Under the PWM operating conditions, the current flowing over the IGBT module approximates a sinewave. This sinusoidal current can induce periodic junction temperature fluctuations within the IGBT module. As shown in Fig. 14a, the junction temperature does not monotonously increase. Instead, it increases with fluctuations. These periodic junction temperature fluctuations are directly related to the operation frequency. In addition, the junction temperature variations of the three test positions during one period of operation are not the same. The variations are 3.35 °C at test point *D*, 3.01 °C at test point *E*, and 2.66 °C at test point *F*. It can be seen that the junction temperature fluctuations in the central region of the IGBT chip were greater than those in other regions.

In addition, the junction temperature rates of increase at different test positions in the initial heating phase are different under the DC and PWM test conditions. In the DC-I test shown in Fig. 13a, the junction temperature rate of increase in the region near the bond wire heel (test point *B*) is approximately as high as that in the central region (test point *A*) at the very beginning of the heating duration. Conversely, Fig. 14a shows that under the PWM-I test condition, the junction temperature rate of increase in the central region of the IGBT chip (test point *D*) is clearly higher than that in the other regions during the entire heating duration.

When current flows from the Al metallization layer into the bond wires, the dramatic reduction in the area of the current flow causes current crowding near the bonding area. This current crowding can increase the local junction temperature due to the joule heating effect. The current rate of increase under the DC-I test condition is clearly higher than that under the PWM-I test condition at the very beginning of the heating duration. Thus, severe current crowding occurs around the bonding area in the DC-I test after

the high current injection begins, which causes the junction temperature in this region to dramatically increase. In the PWM-I test, the current increases relatively slowly when compared with that in the DC-I test. Thus, a severe current concentration does not occur in the bonding area. As a result, the junction temperature rate of increase around this region is not as high as that observed in the DC-I test. Furthermore, the junction temperature rate of increase around the bond wire heel (test point *B*) slows down after 0.04 s in the DC-I test, since the current concentration is mitigated when the current is stabilized.

Figures 13b through i and 14b through i show selected infrared images of the IGBT 2 chip at different times during one power cycle under the DC-I test condition and under the PWM-I test condition, respectively. The junction temperature distribution of the IGBT chip over time in the PWM-I test is basically the same as that in the DC-I test. During the power-off phase, the junction temperature of the IGBT chip decreases to the cooling temperature, which is approximately 45 °C, as shown in Figs. 13b and 14b. When current flows into the IGBT chip, heat is generated around the bond wires, as can be seen in Figs. 13c and 14c. Then the heat spreads to the other regions of the IGBT chip. The heat flux spreads across the entire surface of the IGBT chip at approximately $t=0.895$ s, as can be seen in Figs. 13f and 14f. Eventually, the hottest region is located in the center of the IGBT chip, as can be seen in Figs. 13g and 14g. The control switch is turned off at time $t=4$ s, and an uneven temperature distribution can be observed during the cooling duration.

Still, some obvious differences in the junction temperature distributions of the IGBT chips can be observed. The central region of the IGBT chip experiences a comparatively higher temperature than the other regions during the entire heating duration. The junction temperature distributions at $t=0.08$ s, as can be seen in Figs. 13d and 14d, show that the temperature around the bond wire heels under the PWM-I test condition is not as high as that under the DC-I test since a severe current concentration does not occur under the PWM-I test condition. Furthermore, the temperature in the region under the bond wires is lower than that in the other regions due to the low current density in this region.

Figure 15 shows the junction temperature distributions over the IGBT chips and the projections at $t=3.895$ s under the DC-I and PWM-I test conditions obtained by IR camera measurements. The junction temperature distribution is relatively uniform across the surface of the IGBT chip under the DC-I test condition, while the temperature gradient under the PWM-I test condition is clearly greater than that observed under the DC-I test condition. These results indicate that the temperature gradient varies under different operating conditions, which indicates that a larger power loss results in a larger temperature gradient.

4.3 Thermal stress induced by junction temperature fluctuations

One last difference caused by different operating conditions is thermally induced stress. Under the PWM test conditions, the fluctuations in the junction temperature can induce periodic stress in the interconnections of the IGBT module. To further investigate the effect of junction temperature fluctuations on the stress state of the IGBT module, an FE analysis is applied here.

A comparison of the stress results for the DC-I and PWM-I test conditions is given in Figs. 16 and 17. Under both test conditions, the compressive stresses in the 1-direction and 2-direction concentrate at the interfaces of the bond wires and the Al metallization layer due to the large CTE mismatch among the bond wires (22 ppm/K), the Al metallization layer (21 ppm/K), and the IGBT chip (2.5 ppm/K). The maximum compressive stress occurs at the corner of the interface between the bond wires and the Al metallization layer. The maximum S11 stresses are − 6.89 MPa in the DC-I test and − 22.69 MPa in the PWM-I test. Meanwhile, the maximum S22 stresses are − 6.98 MPa in the DC-I test and − 23.28 MPa in the PWM-I test. This difference in maximum stress is due to the different maximum junction temperatures that can be reached under the two test conditions.

Periodic thermal stress can be observed under the PWM-I test condition. This periodic thermal stress is induced by the

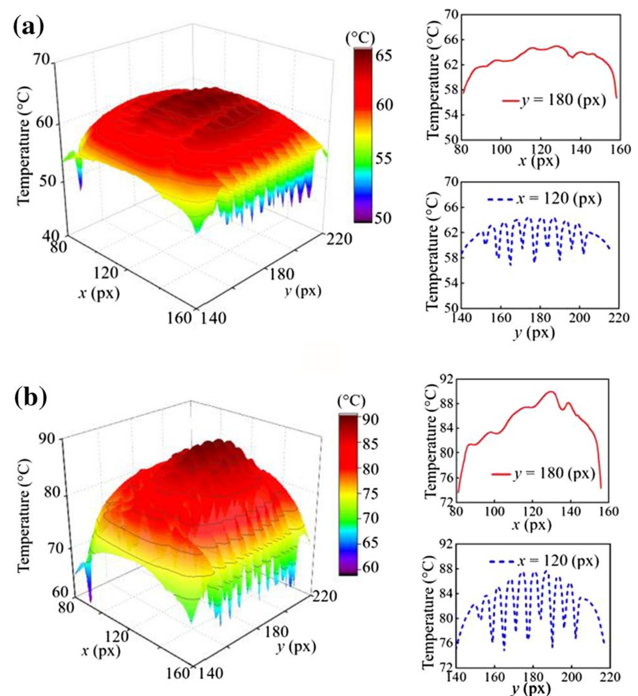

Fig. 15 Temperature distributions of the IGBT chip at $t=3.895$ s under different test conditions: **a** DC-I; **b** PWM-I

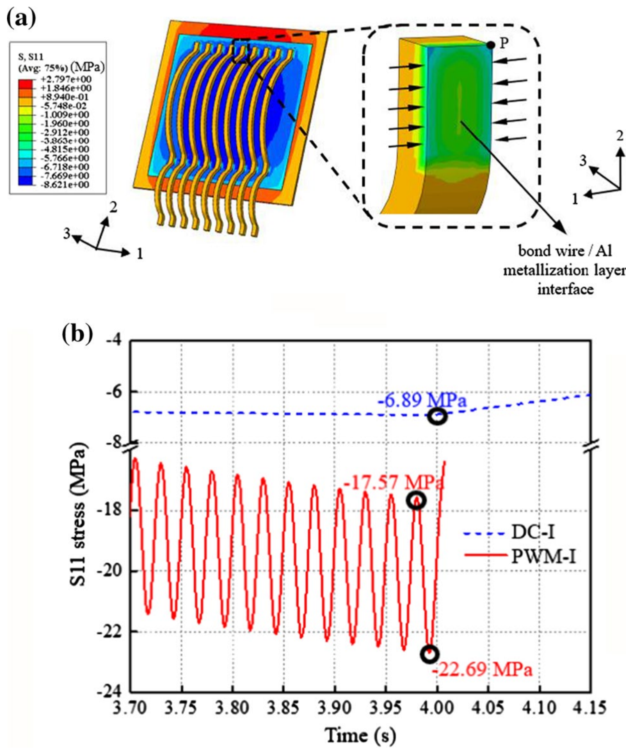

Fig. 16 Comparison of S11 stresses under different test conditions: **a** stress distribution under the DC-I test condition; **b** S11 stress history of point *P* under different test conditions

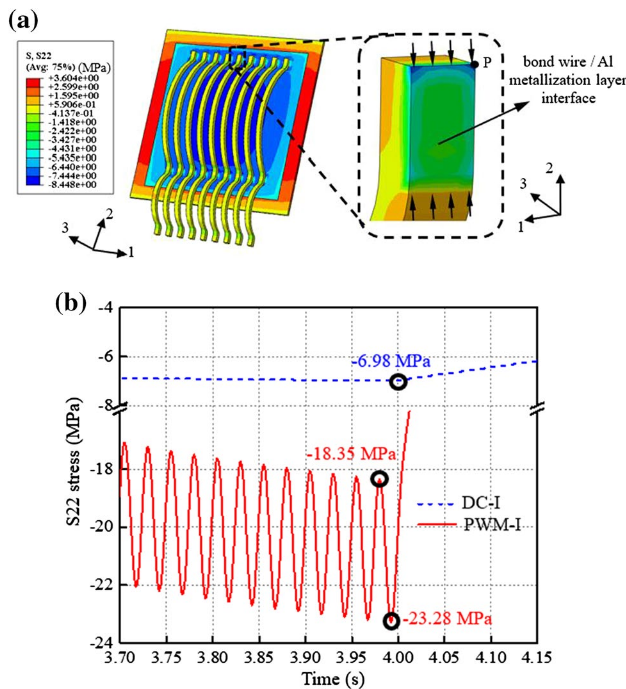

Fig. 17 Comparison of S22 stresses under different test conditions: **a** stress distribution under the DC-I test condition; **b** S22 stress history of point *P* under different test conditions

junction temperature fluctuations due to the periodic sinusoidal current under the PWM-I test condition. Thus, this stress corresponds to the operational frequency. The variations in the stress reach 5.12 MPa in the 1-direction, and 4.93 MPa in the 2-direction. The maximum stress is only approximately 4–5 times the value of the periodic stress variation in both directions, which indicates that the stress variation accounts for a large fraction of the total stress. This repeated stress variation in the interface between the bond wires and the Al metallization layer can lead to fatigue failure of the bond wires. The failure of a single bond wire can result in a current redistribution in the IGBT module, which accelerates the failure of the remaining bond wires. Eventually, this stress may cause the IGBT module to malfunction and significantly shorten the life of IGBT modules.

4.4 Effect of the switching frequency on the junction temperature of an IGBT Chip

To further investigate the effect of the switching frequency on the junction temperature of the IGBT chip, power cycling tests are conducted under the DC-II, PWM-II, and PWM-III test conditions. For the DC-II test, $t_{on}=0.025$ s and $t_{off}=0.025$ s are selected, and the total cycling period is 0.05 s, which indicates $f_{sw}=20$ Hz. The operational cycling period of the PWM-II and PWM-III tests is 0.05 s, which is the same as that in the DC-II test. However, the switching frequencies of the PWM-II and PWM-III tests are 5 kHz and 10 kHz, respectively. These values are much higher than that in the DC-II test.

Here, the multiple time-delayed acquisition method is applied to acquire more frames within one operation period, and the junction temperature evolutions in the central region of the IGBT 2 chip under the three test conditions are shown in Fig. 18. The lowest junction temperature is observed under the DC-II test condition since there is no switching loss in the IGBT module, and the junction temperature increase of the IGBT chip is only induced by conduction loss. The maximum junction temperature is approximately 63.81 °C in the PWM-II test with $f_{sw}=5$ kHz. In addition, the temperature reaches approximately 73.57 °C when $f_{sw}=10$ kHz in the PWM-III test. When the switching frequency increases, the junction temperature of the IGBT chip clearly increases due to the increasing switching loss. These results indicate that the switching frequency has a strong influence on the junction temperature of the IGBT chip since the switching loss is mostly influenced by the switching frequency.

It is worth noting that in the DC-II test, the junction temperature of the IGBT chip reaches its maximum value at $t=0.025$ s, i.e., when the power is turned off. It is worth noting that in the PWM-II and PWM-III tests, the maximum junction temperature does not occur at the power-off moment. Instead, the peak value of the junction temperature is reached before the applied power is disconnected. A

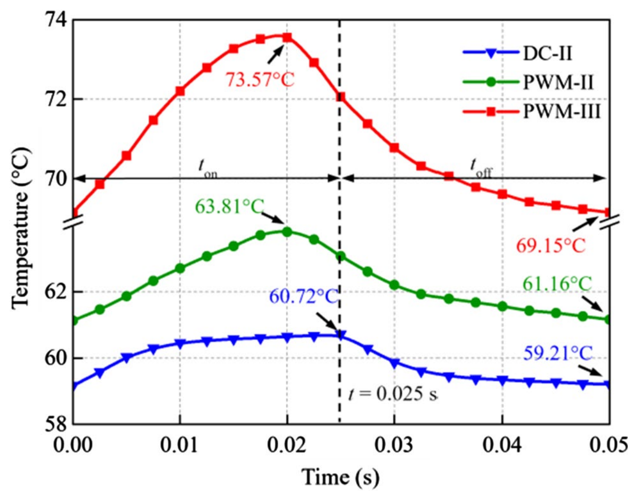

Fig. 18 Temperature profiles measured by an IR camera under different test conditions

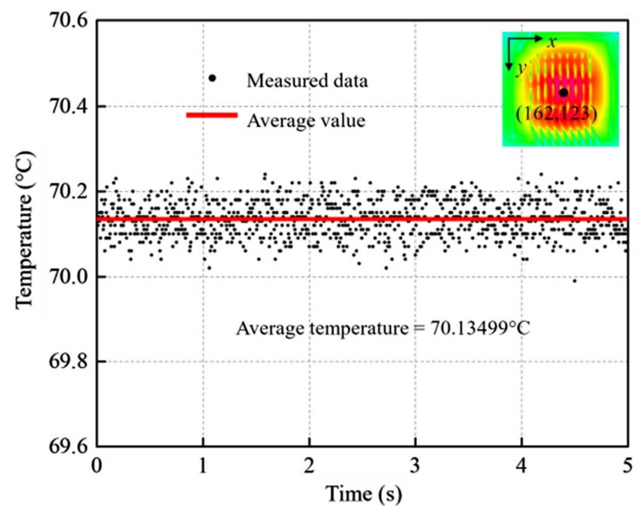

Fig. 19 Measured temperatures obtained by an IR camera with an integration time of 800 μs

reasonable assumption is that the different waveforms of the loading currents in the DC and PWM test conditions cause the highest junction temperatures to occur at different times.

In the DC-II test, a constant current is injected into the IGBT module until it is turned off. The IGBT module is continually heated by the current load. Thus, the maximum junction temperature in the DC-II test occurs at the power-off moment. In the PWM-II and PWM-III tests, since a sinusoidal current is applied, the current begins to decrease before the power is turned off at $t=0.025$ s, i.e., at $t=0.0125$ s. The junction temperature of the IGBT chip decreases when the generated heat is less than the dissipated heat. Therefore, the peak values of the junction temperature under the PWM-II and PWM-III test conditions are obtained before the power-off moment.

4.5 Junction temperature variation during one switching duration

The maximum sampling frequency of an IR camera measurement is limited by the integration time used for acquiring infrared images. Here, the switching frequency of the IGBT module is 5 kHz, which indicates that the temporal duration of one switching cycle is 200 μm. Meanwhile, the integration time is set between 800 and 2000 μm. Thus, the temporal duration of one switching cycle of the IGBT module is shorter than the integration time. As a result, the IR camera measurement cannot reveal the periodic junction temperature variation dependence on the switching frequency. To overcome this problem, the junction temperature variation of the IGBT chip within one switching cycle is investigated by changing the IR camera integration time.

A power cycling test under the DC-III test condition is conducted. The switching frequency of the IGBT module in this test is 5 kHz, which means the temporal duration of one switching cycle is 200 μs. An integration time of 800 μs was used for the first IR camera measurement to record the flow of photons within four switching cycles. To address the issue of uncertainties, the junction temperature measurement is performed 1000 times after the steady state is reached. Then a statistical data analysis is performed between the average value of the junction temperature and the measured data, as shown in Figs. 19 and 20. For IR camera measurements with an 800 μs integration time, the average value of the measured data is 70.13499 °C with a standard deviation of 0.041794735 °C.

Then IR camera measurements are performed by applying integration times of 1000 μs and 1200 μs, and the IR camera records the photos within five switching cycles and six switching cycles, respectively. The average junction temperature values obtained with the integration times of 1000 μs and 1200 μs are 70.16973 °C and 70.20359 °C, respectively. Thus, the junction temperature variation during one switching cycle can be obtained by subtracting the two junction temperatures obtained with integration times of 1000 μs and 800 μs or integration times of 1200 μs and 1000 μs, and the resulting junction temperature variations are 0.03474 °C and 0.03386 °C, respectively. The proposed approach allows the high-speed thermal transient in an IGBT chip to be captured and the switching loss-induced junction temperature variation to be assessed by adjusting the IR camera.

5 Conclusion

This paper aimed at providing an IR camera acquisition method for transient temperature measurements of power modules. This approach allows for effective matching of the

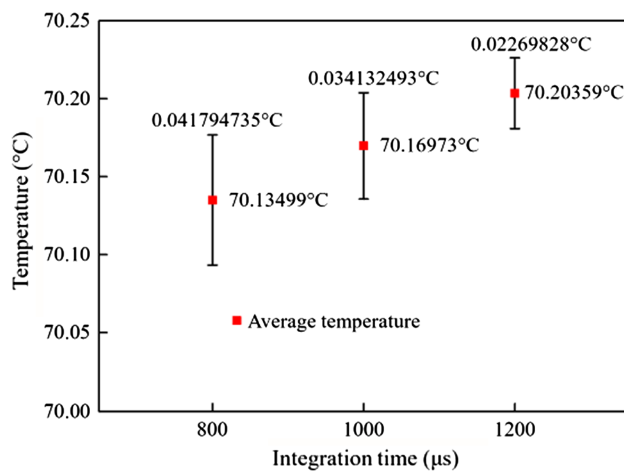

Fig. 20 Average junction temperatures and standard deviations at different integration times

timing of a thermal transient event and image acquisition to provide full frame measurements of a replicable junction temperature. It also allows the junction temperature variation induced by the instantaneous loss of the power module to be obtained.

The proposed method was employed on an IGBT module. Six power cycling tests were conducted under DC and PWM operating conditions. Junction temperature estimation methods (TSEP measurement, IR camera measurement, and FE analysis) were performed, and the results were compared. The obtained results indicate that TSEP measurement can only provide a mean junction temperature for an IGBT chip. Meanwhile, the maximum junction temperature can be obtained by IR camera measurement or FE analysis. The effects of the operating conditions (DC vs. PWM) on the thermal and mechanical results of an IGBT module were investigated. The maximum junction temperature of the IGBT chip under the PWM test conditions was clearly higher than that under the DC test conditions due to the switching power loss. In addition, a larger power loss resulted in a larger temperature gradient. Under the DC operating conditions, the junction temperature of the IGBT chip monotonously increased. Meanwhile, under the PWM operating conditions, the temperature increased with fluctuations. The current rate of increase around the wire bonding area in the DC test was clearly higher than that in the PWM test at the very beginning of power cycling since current crowding occurs under the DC test conditions. Furthermore, the thermally induced stresses under the DC and PWM test conditions were determined using FE analysis. The operating conditions also affected the thermally induced stresses of the IGBT module. The periodical sinusoidal current under the PWM operating conditions resulted in periodic stress in the interconnects of the IGBT module, and this stress variation accounted for a large fraction of the total stress. This repeated stress variation in the interfaces can lead to a fatigue failure of an IGBT module.

The effect of the switching frequency on the junction temperature results of an IGBT module was also investigated. The switching frequency had a strong influence on the junction temperature of the IGBT chip. When the switching frequency increased, the junction temperature of the IGBT chip clearly increased due to increasing switching loss. These results indicated that the maximum junction temperature in the PWM test did not occur at the power-off moment, as in the DC test, since the sinusoidal current began to decrease before the IGBT module was turned off, and the junction temperature of the IGBT chip decreased when the generated heat was less than the dissipated heat.

Finally, the junction temperature variation induced by the instantaneous switching loss was assessed by the proposed IR camera measurement approach. The obtained results revealed a quantifiable correlation between the switching loss and the junction temperature variation of the IGBT module. This correlation should benefit further investigations on the performance of semiconductor power losses. It should also enable optimization of the efficiency of power devices.

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