



# Hardware implementation for hybrid active NPC converters using FPGA-based dual pulse width modulation

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## Abstract

Recent developments in power electronics technologies have resulted in a need for fast responses and dynamic control. However, existing control schemes are still limited to the available digital signal processors (DSPs) and their associated high prices. The field-programmable gate array (FPGA) offers fast performance and high control flexibility by providing a reconfigurable computing speed. However, it has some implementation limitations in standalone systems. In this regard, this paper presents a hardware setup for a three-level hybrid active neutral point inverter (HANPC) using a FPGA and a DSP. A unique method using digital and analog modulation is designed in this study using Vivado software. The proposed method depends on receiving analog reference signals from the DSP and then performing all the required processes using the FPGA. Direct pulse width modulation is generated to control the HANPC without changing the hardware configuration of the main topology. The implemented hardware is based on a 15 kW HANPC topology that is mainly controlled by a Digilent Zybo-Z7-20 FPGA. The effectiveness of the proposed system was verified by experimental results.

**Keywords** Converters · HANPC · Hardware · FPGA · Multilevel inverters

## 1 Introduction

Large-scale power converters are regarded as the dominant part used in the renewable energy field. In recent decades, various developments have been made on different power converter topologies to satisfy the excess energy demand. Standalone, hybrid, and grid-connected systems are the main types of renewable energy systems [1]. In all types of renewable energy systems, the power conversion system is the most significant. Solar energy is the preferred source of energy due to its wide availability and ease of use [2, 3]. Consequently, improvements in control systems have moved toward the use of microprocessors, such as digital signal processors (DSPs), for controlling power converters [4, 5]. Nevertheless, such microprocessors suffer from speed limitations, limited output control, and high price. Conversely, field-programmable gate arrays (FPGAs) offer an alternative platform for implementing digital systems due to their capability in terms of high-speed processing and parallel

hardware designs with lower cost, as well as their high flexibility in the simultaneous control of multiple outputs [6, 7]. These features lead to multi-operation, which reduces the computing time and achieves optimum operational performance. This can be contrasted with similar controllers made up of analog components. [8–10]. The key point of using such tools is distinguishing between the programming part and the architecture part. Meanwhile, the reconstruction of the experimental part has higher flexibility [11–13]. According to [12], some of the main drawbacks of microprocessors can be solved by recent developments in FPGAs.

Several studies have focused on the application of FPGAs in multilevel converters, especially for high-speed control systems [14–16]. For instance, the authors of [15] proposed the control of multilevel inverters based on an experimental evaluation. The main interest was in the implementation of an FPGA to control the system. On the other hand, no attention was paid to the enhancement of the harmonic content of the output waveforms. Similar analyses were performed in [17–19] for different applications. However, the possible benefits of enhancing the overall harmonic distortion have not been thoroughly verified.

This paper presents the hardware implementation of hybrid neutral point clamped converters (HANPCs) using

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an FPGA for carrying out the numerous modulation process of a system. In this study, an improvement of the existing design, which consists of DSP boards, is being considered. The advantages of an FPGA in terms of greater flexibility and a wider range of output control overcome the DSP sampling and computation time limitations [20]. It also helps in avoiding the complex constructions of standalone FPGA handling issues. The implementation of additional hardware to improve the quality of existing systems is being demonstrated for different applications as explained in [21–23]. In this regard, this paper presents a hardware implementation for hybrid neutral point clamped converters (HANPCs) using an FPGA for carrying out the modulation of a system. An FPGA possesses fast performance and high control flexibility by providing a reconfigurable computing speed. Meanwhile, HANPC converters are operated at two different levels of switching frequencies: low (50–60 Hz) and high frequencies (30–40 kHz). In addition, a large number of switching devices (18 devices) needs to be controlled at the same time. Therefore, the FPGA offers the best choice for carrying out the necessary modulations at different frequencies. The proposed method uses analog reference signals from the DSP and then processes the signals using the FPGA to efficiently control the pulse width modulation (PWM) signals of the HANPC.

The remainder of this paper is organized as follows. The basic working performance of the HANPC is presented in Sect. 2. The basic implementation of the FPGA and DSP within the system is discussed in Sect. 3. Simulation results, experimental verification, and discussions are presented in Sect. 4. Finally, some conclusions are presented in Sect. 5.

## 2 Physical model of HANPC inverters

The main circuit diagram of an HANPC converter is shown in Fig. 1. The HANPC converter was originally developed from the natural point clamped (NPC) topology. The basic configuration of a conventional NPC inverter has four insulated-gate bipolar transistors (IGBT) switches ( $S_{x1}/D_{x1}$ ,  $S_{x4}/D_{x4}$ – $S_{x6}/D_{x6}$ ) with their associated diodes in addition to two active diodes ( $D_{x2}$  and  $D_{x3}$ ) in each phase, where  $x$  represents the  $A$ ,  $B$ , or  $C$  phase. However, the NPC suffers from uneven distribution of the losses between switching devices. To overcome this issue, the two active diodes ( $D_{x2}$  and  $D_{x3}$ ) are replaced with two active switches ( $S_{x2}/D_{x2}$  and  $S_{x3}/D_{x3}$ ).

However, this topology is still limited to a specific switching frequency of up to 10 kHz, and it needs to have a balance between different switches [24–26]. Therefore, this topology is updated by changing the active switches with two metal–oxide–semiconductor field-effect transistor (MOSFET) switches, as shown in Fig. 1. This change results in improved performance and allows the system to work at high

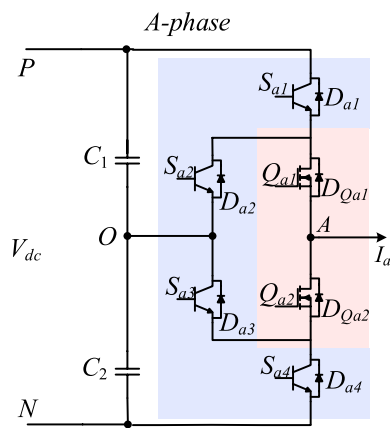


Fig. 1 Typical one leg of an HANPC inverter

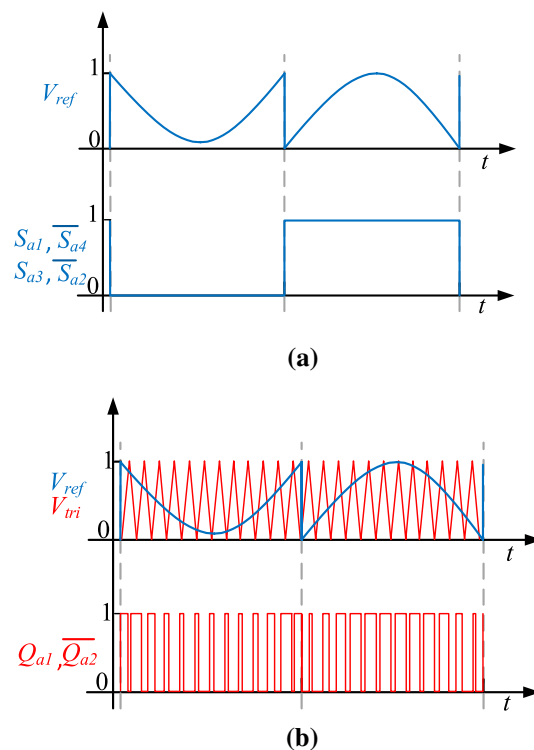


Fig. 2 HANPC switching sequences for: a IGBTs at 50 Hz; b MOSFETs at 30 kHz

switching frequencies without the need to consider balancing the switches among all of the devices. Consequently, the switching losses for the MOSFETs are smaller than the conduction losses. However, they can work at higher operating temperatures than standard Si-IGBT switches. In this regard, the IGBT switches operate at the lowest possible frequency (50 Hz), while the MOSFET switches operate at higher frequencies (equal to or higher than 30 kHz), as shown in Fig. 2. It is worth mentioning that IGBTs are not

designed to work under very fast switching frequencies, since they operate at a maximum switching frequency of up to 10 kHz (an allowable frequency for the Si-IGBTs) to withstand high voltage applications. However, for higher switching frequencies of up to 20 kHz, the maximum voltage is reduced to lower the voltage range and the total efficiency of the system [27]. While the maximum allowable switching frequency for MOSFETs can be tens of kHz or higher [27]. Nevertheless, values higher than 30 kHz result in reductions in the withstand voltage capability with respect to lower voltage and current ranges, while lower switching frequencies increase the losses of the MOSFET devices. Meanwhile, it should be noted that the HANPC topology is regarded as a new topology that requests special control and switching sequences for each of the IGBTs and MOSFETs devices, where a 30 kHz has been considered to be a suitable switching frequency that allows for a lower filter size and better harmonics performance as illustrated in [28]. For the loss distribution in HANPCs, when compared to other common topologies such as neutral point converters (NPC) and T-type inverters, where the losses are considered to be a major issue that needs to balance the losses between all of the switching devices. Nevertheless, in HANPCs, to achieve a high efficiency at higher switching frequencies with lower switching losses a higher switching frequency is more desirable [29]. Meanwhile, using SiC diodes significantly reduce the reverse recovery loss on diodes and decreases the turn-on loss on Si IGBTs [30–33]. Hence, IGBTs can be optimized for the lowest conduction losses while having high switching losses compared to SiC MOSFETs. In this way, switching losses only occur in fast and highly efficient SiC

components. Thus, the number of SiC devices is reduced to a minimum, which achieves an optimal cost-performance ratio at the lowest possible cost. SiC MOSFET devices are up to eight times more expensive than the Si IGBT devices [28]. Therefore, instead of using a full SiC topology, four Si active switches and two SiC MOSFETs are used. Thus, it has a lower total cost at the highest possible efficiency. As a result, the switching losses are significantly reduced and high efficiency is achieved.

### 3 Algorithm implementation process

In this section, the implementation of the FPGA alongside the DSP in controlling a HANPC is highlighted and clarified.

#### 3.1 Integration and modulation reference signals

The main configuration of the system is shown in Fig. 3. In this system, the ADC unit is an analog to a digital unit that is used to convert analog data that was fed from the system by voltage sensors and current probes. The voltage sensor is responsible for measuring the DC link voltage (i.e., the upper capacitor  $C_1$  and the lower capacitor  $C_2$ , as shown in Fig. 1). In addition, the current probes measure the three-phase currents. These signals are then converted into digital signals and used to complete the closed-loop control cycle. The measured voltages and currents for each of the phases represent feedback vital information. The reference voltages are generated based on them. Consequently, the DSP

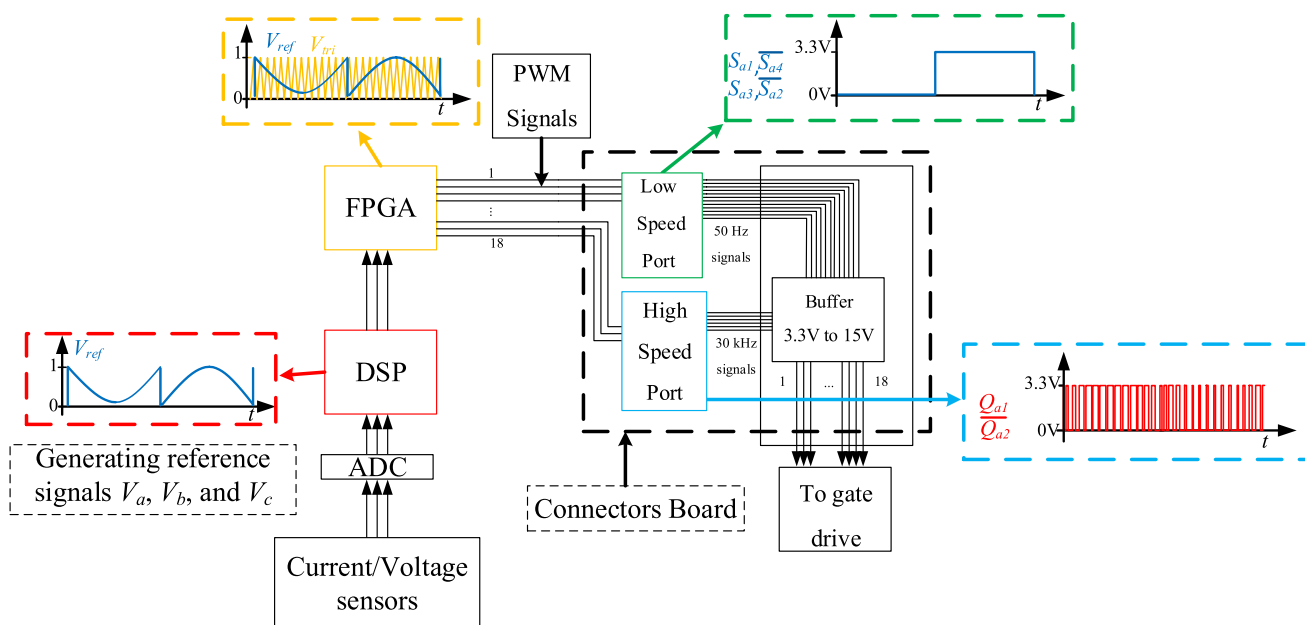


Fig. 3 System configuration, including the DSP, FPGA, and connection board between the FPGA and the gate drivers of an HANPC

generates sinusoidal voltage references for three phases: *A*, *B*, and *C* phases. Then, the FPGA performs the comparison and the PWM signal generation process. In the FPGA, the reference voltage signals are converted from analog to digital signals, and the carriers are generated at the proposed switching frequency. The references are generated by the DSP and sent to the FPGA due to the limitations of FPGAs in generating a variable sinusoidal signal without predefined values for the memory file. The generated voltage references  $V_x$  (where  $x$  is the *A*, *B*, and *C* phases) are shown in (1):

$$V_x = V_m \cdot \sin(\omega t). \quad (1)$$

where  $V_m$  is the magnitude of the three-phase voltage references *A*, *B*, and *C* phases with a  $120^\circ$  phase shift,  $t$  is the time, and  $\omega$  is the fundamental frequency. Then, these voltage references are normalized to obtain a unity voltage output, as shown in (2):

$$V_{\text{Nor}} = 1 + \left( \frac{2 \cdot [V_{\text{ref}}]}{V_{\text{dc}}} \right). \quad (2)$$

where  $V_{\text{dc}}$  is the DC-link voltage. Subsequently, all of the necessary comparisons are performed to generate the final.

PWM signals and send them to the buffering circuit and gate drives for the IGBT and MOSFET switching devices. Here, it is necessary to clarify the process performed within the FPGA. An FPGA is usually used to perform multiple functions, including complex processes, such as those in arithmetic logic units, memories, and image processing. In addition to its high flexibility and fast response, the FPGA is suitable for performing multi-input/output tasks. Therefore, it is suitable for implementing modulation techniques that involve duty cycle evaluations at high speeds and precise accuracy. This is due to its ability to choose from a wide range of clock cycle signals followed by fixing the duty cycle, as shown in Fig. 4. The following sections present a detailed overview of the key technical aspects relevant to the design, implementation, and simulation of the control algorithm.

### 3.2 Features of the FPGA implementation

To generate a carrier, designing a robust digital system is needed to modulated different signals and to adequately evaluate them. Therefore, all of the operations must be coordinated concerning the desired switching frequencies.

The proposed converter (HANPC) is modulated within a wide range of frequencies, including high and low frequencies. The low frequency was modulated at 50 Hz and the high frequency was modulated at 30–40 kHz. The high frequency is used by the MOSFET switching devices, whereas the low frequency is the fundamental frequency used by the IGBT switching devices. 30 kHz is chosen for hybrid generation, and the carrier is generated within the FPGA based on this. 50 Hz is based on the zero-crossing of the reference frequency, which does not require any special arrangement for the carrier. Depending on the type of modulation, the sample size is chosen for the modulated signal [24]. For synchronous output signals, the number of samples  $N_s$  needed to structure the proposed frequencies of the fundamental 50 Hz with respect to the requested 30 kHz modulating signal is determined as shown in (3):

$$N_s = \frac{f_{\text{hybrid}}}{f_{\text{fundamental}}}, \quad (3)$$

where  $f_{\text{hybrid}}$  and  $f_{\text{fundamental}}$  are the hybrid frequencies at 30 kHz and the fundamental frequency at 50 Hz, respectively.

The size for the collected samples of the modulating signals is 600. To update the modulating cycles, the clock signal cycle (CLK) is managed concerning the hybrid frequency  $f_{\text{hybrid}}$ . In addition, with regard to the number of samples of the carrier waves  $N_{\text{car}}$  to achieve a higher resolution,  $N_{\text{car}}$  is selected to be 1000 in this study.

The frequency of the clock signal needed for resetting the carrier samples can be determined based on this value, as shown in (4):

$$\text{CLK} = f_{\text{hybrid}} \cdot N_{\text{car}}. \quad (4)$$

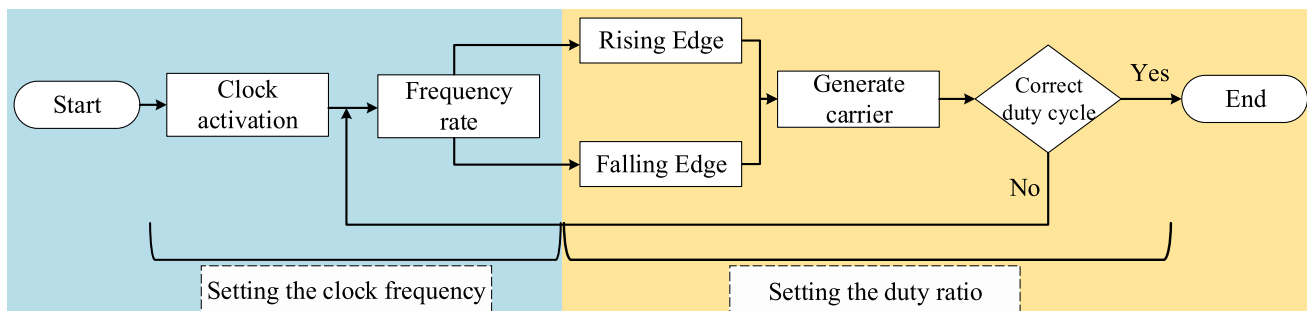


Fig. 4 Clock and typical duty cycle sequence inside a FPGA

Thus, the resultant frequency of the required CLK signal is 30 MHz. It is necessary to evaluate the effects of the harmonics that are found in the output voltage generated by the sinusoidal pulse width modulation (SPWM) used in this paper. First, the harmonic components of the pole voltage ( $V_{an}$ ) consider the *A* phase for carrying out all the needed explanations.  $V_{an}$  contains harmonics at the carrier frequency ( $f_c$ ) and frequencies of its integer multiples ( $M$ ), and the sidebands ( $N$ ) of all the frequencies. These harmonics are also known as switching harmonics, which can be expressed as shown in (5) and (6):

$$V_{o-h} = V_h \sin [2\pi(Mf_c \pm Nf_o)t + \phi_h], \tag{5}$$

$$V_{o-h} = V_h \sin [2\pi f_o(Mm_f \pm N)t + \phi_h]. \tag{6}$$

Here,  $f_o$  is the fundamental frequency,  $m_f$  is the frequency modulation index,  $m_f$  represents the ratio between the carrier frequency  $f_c$  and  $f_o$  i.e.,  $m_f = f_c/f_o$ . In addition, *M* and *N* are integer numbers and their summation gives an odd value, and  $\phi_h$  is the phase harmonics component. The order of the harmonics is representing in (7):

$$\begin{cases} m_f, & m_f \pm 2, & m_f \pm 4, \dots \\ 2m_f \pm 1, & 2m_f \pm 3, & 2m_f \pm 5, \dots \\ 3m_f, & 3m_f \pm 2, & 3m_f \pm 4, \dots \\ 4m_f \pm 1, & 4m_f \pm 3, & 4m_f \pm 5, \dots \end{cases} \tag{7}$$

Among these harmonics, the component of order  $m_f$  has the largest magnitude. This means that the harmonic with a frequency equal to switching frequency  $f_c$  is the largest one as clarified in Fig. 5. In this figure, an example is provided. The fundamental frequency is considered to be 50 Hz and the frequency modulation index is set to be 21. In this case, a harmonic of 1050 Hz ( $21 \times 50$ ) means that the switching frequency has the largest component. This implies that the higher switching frequency has a higher order of harmonics. Therefore, using a higher switching frequency results in improving the output waveforms, reducing the needed

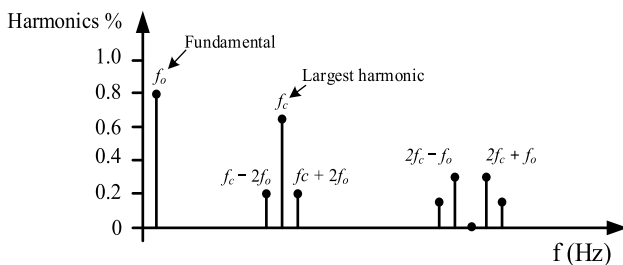


Fig. 5 Frequency spectrum of pole voltage using the SPWM technique

filter in terms of size and simplifying the design. However, a higher switching frequency can add extra switching losses to the systems [34]. Thus, the switching frequency is set to be as high as possible using SiC MOSFETs switches (operating at 30 kHz) in a hybrid combination with Si IGBTs at the lowest possible frequency (operating at the fundamental frequency at 50 Hz).

### 3.3 Implementation of the control algorithm

In this study, a Digilent Zybo-Z7-20 FPGA board is used to implement the control algorithm. Very High-Speed Integrated Circuit Hardware Description Language (VHDL) is used to program the board. The main parts of the system are divided into a comparator, a buffer (integrator and power splitter), a dead-time director, and a combination block. As mentioned earlier, the FPGA is preferred over other microcontrolling devices due to its advantages in terms of low cost, fast speed, and multi-input/output implementation with high-performance capability.

The typical design for an FPGA has a number of steps from the start of the design up to the programming stage. The flowchart shown in Fig. 6 represents a typical design process for an FPGA.

In this figure, the process starts with a description of the design in a step entitled by its behavioral description. In this step, the hardware description language (HDL) code is written in an editor, and syntax errors (if there are any) are corrected. Second, validation is performed. In this stage, the developed HDL code proceeds within an extensive simulation process, where the code is validated for further

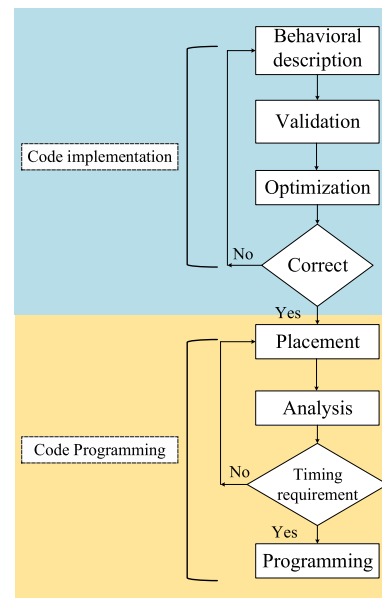
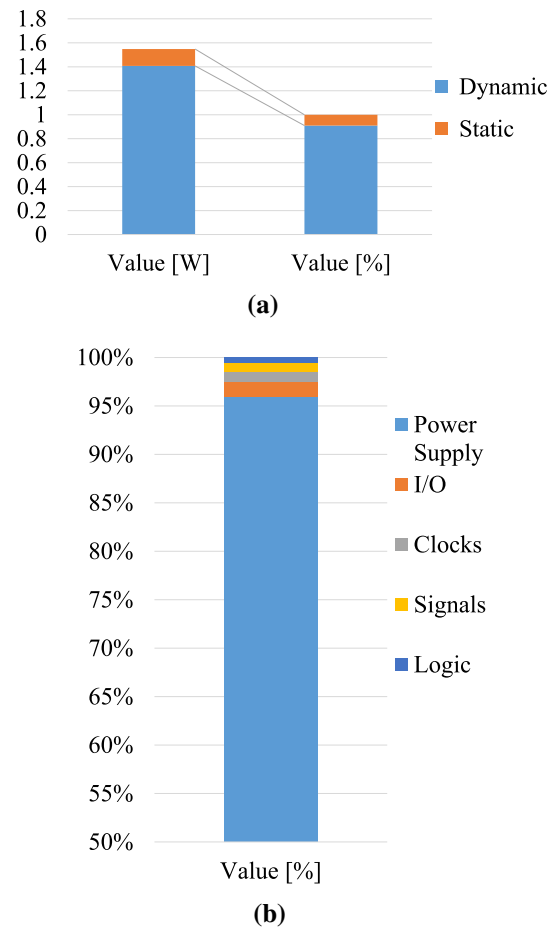


Fig. 6 Typical VHDL code process through an FPGA

functional processes. Third, optimization is conducted, where the validated code is synthesized into an implementation of the solid-state using straightforward tools (e.g., and, or, not). Meanwhile, there are some issues related to the FPGA performance that still need to be considered in the proposed FPGA code, which is used by the user and its metrics. Following the placement stage, this stage starts right after the actual functionality of the algorithm is optimized, where the function placement is performed and the routing phases are processed. In this stage, special attention is given to power consumption when working at full load. The next stage is the timing analysis. Once the optimization and placement stages are completed, the system is now able to compile the final output with each specific rigor for the project. Therefore, in this stage, all of the timing requirements are fit by analyzing the project requirements over the placement and routing phases of the implemented design. Finally, the FPGA programming is conducted, where the complete design is written in a bit file that is used at the final stage to directly program the FPGA board and to obtain the required output. Meanwhile, the on-chip power calculation should be clarified, as the power consumed during the process of the proposed implementation in the FPGA. Hence, the power analysis for the on-chip power is calculated after the implemented netlist, as well as the activity derived from constraints files, simulation files, or vector less analysis as shown in Fig. 7. As can be seen in this figure, the total on-chip power calculated by the Vivado is around 1.548 W. The largest part of this power is consumed in processing the dynamic process of supplying power to the chip parts (96%), processing the initiating of the I/O (1.5%), the clock (< 1%), the signal (< 1%), and different logic processing (< 1%). Thus, it is clear that dynamic power is responsible for most of the analysis related to the order processing of the device. Whereas, static power is defined as the necessary action to keep the core operating for the processing of all the dynamic operational performances. Moreover, the statistic logical report using the proposed algorithm to use the statistical operations should be clarified. In addition, there is another serious issue that should be noted which is the synchronization between the IGBTs and the MOSFETs since generating the PWM signals and sending them to the gate drives must take into account the deadtime of each module. This protects the system from short circuits due to the hardware limitations as illustrated in Table 1. As a result, the VHDL algorithm is established in the final stage of the implementation to control the HANPC converter. To operate the whole system effectively and to meet the desired modulation output of the HANPC converter, various modules need to be synthesized and connected as shown in Fig. 8. Meanwhile, the HDL coding as well as the design implementation and programming are carried out using Vivado 2019 design software from Xilinx.



**Fig. 7** Vivado power calculation results: **a** on-chip dynamic and static power analysis; **b** distribution for on-chip dynamic power analysis

**Table 1** Statistic logical parameters

Site type	Value
Slice LUTs	275
Slice registers as flip flop	399
Processing time	8,575 ns
Deadtime for IGBTs	3 $\mu$ s
Deadtime for MOSFETs	1 $\mu$ s

## 4 Results and discussion

In this section, the main purpose of the system implementation and its processes are extensively discussed. The main concern is generating binary signals, which are used for modulation in the HANPC converter. Furthermore, the modulation reference signal is designed to have a specific modulation index that is computed through a comparison with the integrator in the internal process.

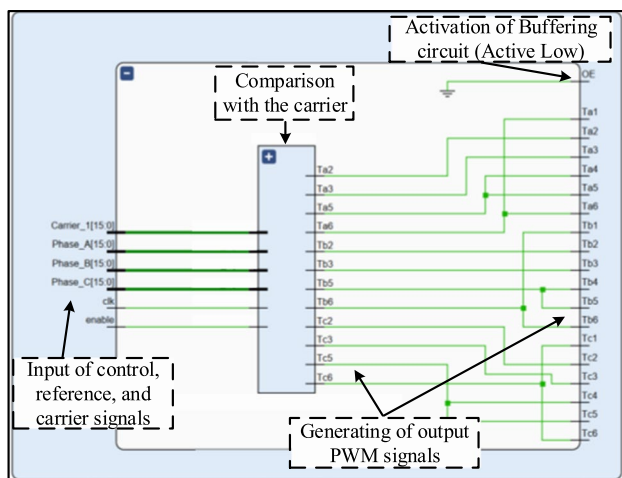


Fig. 8 FPGA scheme diagram using Vivado software

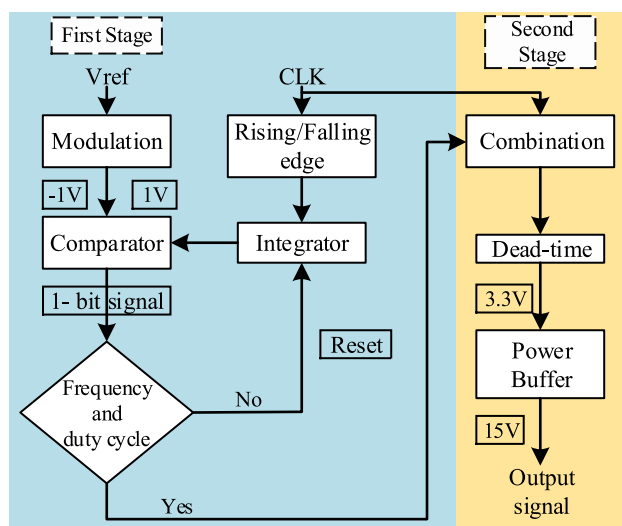


Fig. 9 Block diagram of algorithm implementation

### 4.1 Modulation process

Before analyzing simulation and experimental results, the comparator process should be clarified. Figure 9 shows an event and measures of the reference signals by converting them into single-bit signals. As mentioned earlier, the frequency of the accumulator block is fixed at 30 kHz,

whereas the input signals are modulated at a fundamental frequency of 50 Hz. Each of the inputs and the clock signal are compared and converted to a binary output in the present working phase. Two inputs are entered into the combinational block and the computational block CLK along with the reference signal. During one cycle of the algorithm process, the reference signal is fetched to yield binary output signals that are organized with the respective bridge, which is implemented in the utilized FPGA Digilent Zybo-Z7-20.

In this diagram, the first level of the modulation produces  $-1$  and  $+1$  V waveforms of the reference signal. In the same stage, the CLK is entered to activate the integrator, which includes the generated carrier waveform. The configurable sub-block is then checked to determine whether the proposed frequency and duty cycles are obtained by the comparator. If the obtained 1-bit signal is not combined with the system, the integrator is reconfigured. In the second stage, the driver manages a combination of different signals to choose the output port to which the 1-bit signal should be sent at the combination block. The dead time is then applied to choose the real-time delay for each of the switching device. Here, the HANPC has two different time delays: one is fixed at 300 ns for the IGBTs and the other is fixed at 100 ns for the MOSFETs. The dead-time block is responsible for calculating the time-period between the opening and closing of two switches connected in the same leg of the HANPC converter. It is worth noting that the dead-time needs to be considered to prevent short-circuit failures in the HANPC converter switching sequences, which is shown in Table 2. To accurately calculate the deadtime, some parameters have to be taken into consideration. These parameters include the rise time, the fall time, and both ON and OFF times. In short, for safe operation, the dead-time is usually set to be either equal to or greater than the sum of the OFF-fall time. Here, the final output is almost ready to be used by the gate drives of the switching devices. However, the generated signals are associated with a low voltage level at 3.3 V. Therefore, the last stage includes a power buffer block, which makes it possible to increase the voltage level up to 5 V and then amplify it again to 15 V. As a result, it can be used by the gate drives of the switching devices. Meanwhile, the buffering circuit is not a part of the FPGA board.

Table 2 Normal switching sequence for the HANPC

Switching states	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	$Q_{a1}$	$Q_{a2}$
P	1	0	1	0	1	0
O+	1	0	1	0	0	1
O-	0	1	0	1	1	0
N	0	1	0	1	0	1

However, it is regarded as a necessary part of controlling power converters, such as the HANPC, and it must be able to work at high frequencies. In the 30 kHz case, the used buffering integrated circuit is 74LVX3245.

## 4.2 Simulation results

Vivado software is used to perform the necessary simulations and programming of the FPGA board. The VHDL language is used to program the FPGA and to carry out the necessary simulations, to explain the working principle. As mentioned in Sect. 2, the HANPC operates based on two different frequencies: 50 Hz and 30 kHz for IGBTs and MOSFETs, respectively. In this regard, Fig. 8 presents simulation results for the on-phase leg (*A* phase). As shown in this figure, the MOSFET switches operate at a high frequency, which is related to the triangular carrier frequency. Meanwhile, in the VHDL language, it is difficult to simulate the normalized voltage reference, as shown in Fig. 2. Therefore, the voltage reference shown in Fig. 8 is used to clarify the comparison principle. Nevertheless, in the experiment, the normalized reference is received from the DSP.

The switching for IGBT switching devices is the same as that for the fundamental frequency of the voltage reference. However, MOSFET switching devices operate at higher switching frequencies. The switching difference is clarified by comparing the zoomed in part of Fig. 10 with the original full-scale part.

## 4.3 Experimental verification

The experimental setup is shown in Fig. 11, where all of the parts of the system are shown, including an FPGA, a DSP, a load, and a 15 kW prototype HANPC inverter setup. Meanwhile, the system is run and tested with a resistor–inductor load. The proposed module inverter is this work depends on using discrete devices that are separate for each of the IGBTs and MOSFETs. SEMIKRON-SK75GGB066Ts are used for the Si IGBTs and CREE-C2M0040120Ds are used for the SiC MOSFETs. To achieve compatibility with the high-speed SiC MOSFETs a CREE-C2M0040120D (SiC MOSFET) module is used. It includes a SiC switch and a SiC diode that can handle the fast speed of the SiC-MOSFET. The main characteristics of the associated diode based on the datasheet are shown in Table 3. Moreover, the sensors used in the experimental setup are Seri2B-IVS-D4-500H05-12Ds and Lem-LAH 50-Ps for the voltage sensors and current probes, respectively.

Each device has a separate gate drive—for each of the MOSFETs (CGD15SG00D2) and a dual gate drive for the two IGBTs (SKHI-22A/B), as shown in the experimental setup in Fig. 11. The use of these gate drives allows for the separate control of each switch (including the SKHI-22A/Bs of the IGBTs) since they depend on using a separated gate control signals for each of the switches, which adds great capability to control the inverter for different cases, especially for fault tolerance under different condition of open and short circuit fault conditions. However, some inverter modules (e.g., F3L11MR12W2M1\_B65 by Infineon) are based on one module design for all of the parts (including the IGBTs and the MOSFETs) which

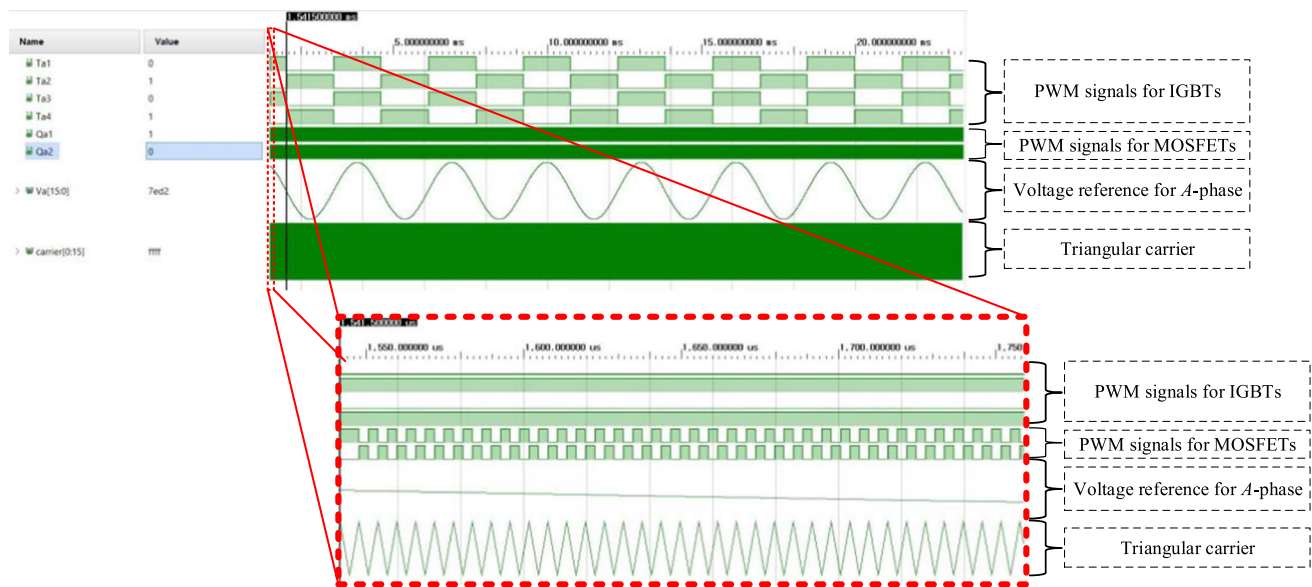
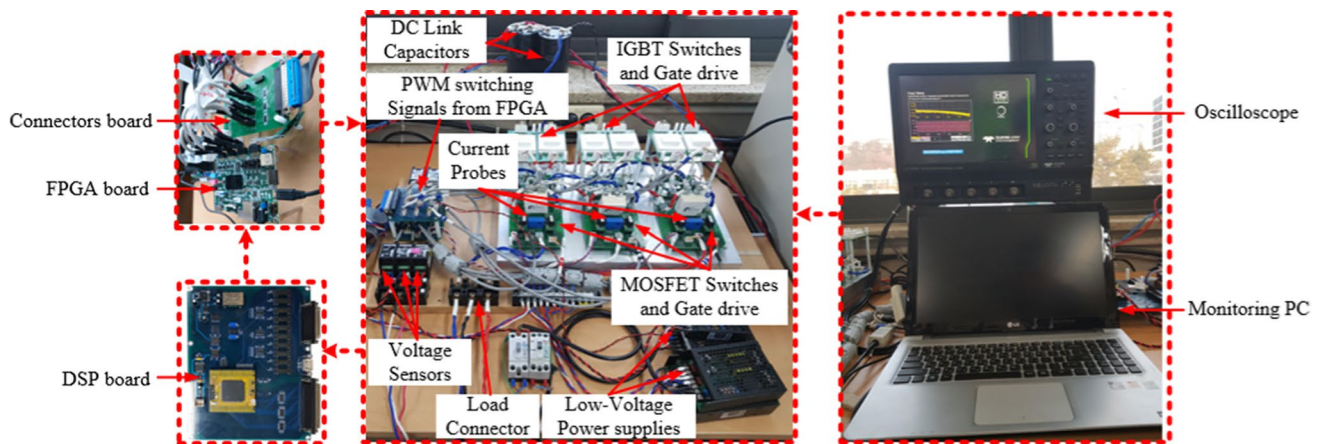


Fig. 10 Vivado simulation result of the A phase





**Fig. 11** Experimental setup

**Table 3** Associated SiC diode characteristics

Parameter	Value	Unit
Diode forward voltage	3.6	V
Reverse recover time	54	ns
Reverse recovery charge	283	nC
Peak reverse recovery current	15	A

**Table 4** Experimental parameters

Parameter	Value
Inductance	1 mH
Resistance	10 $\Omega$
Fundamental frequency	50 Hz
IGBT switching frequency	50 Hz
MOSFET switching frequency	30 kHz

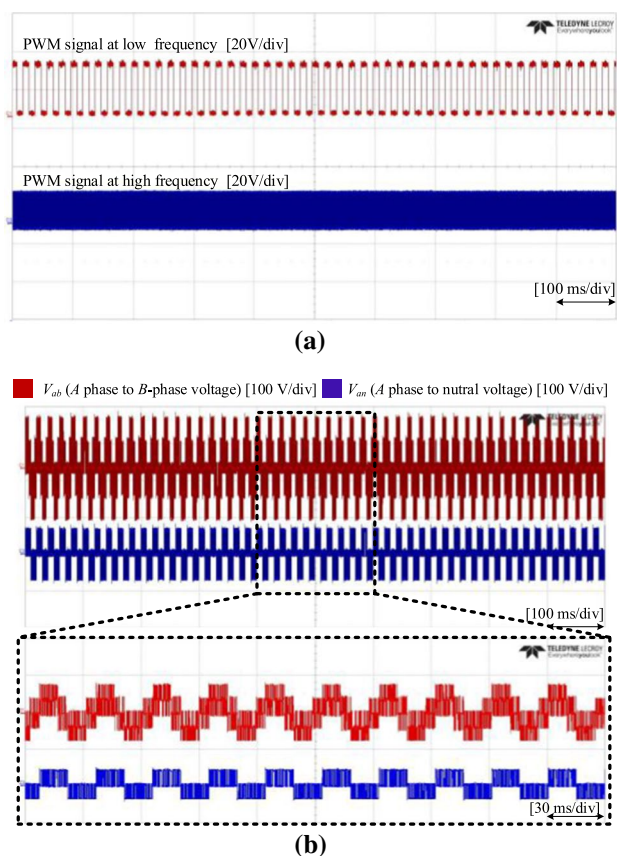
may limit future diagnosis and tolerance for the inverter topology under faulty conditions. It may also result in the need to replace all of the modules, three modules for each phase of the inverters for the *A*, *B*, and *C* phases. Therefore, the proposed topology offers more degree of freedom, easier control, lower maintenance, and the ability of future developments, such as from 3-level to 5-level without the need of replacing any of the already used parts. It is necessary to mention this to improve the existing designs that consist of DSP boards. The design flow using FPGA kits separately is unfamiliar to most DSP engineers. Therefore, total replacement of the DSP would have the disadvantage of modifying the overall design and hardware implementation. Although the ZYBO-PS (ARM) part can be implemented to work individually, it would include higher complexity. Meanwhile, the programming language for using FPGA is regarded as a complex task using the VHDL language. This would add greater complexity to the design and may require additional hardware components to measure the hardware feedback signals. The FPGA adds greater flexibility to the DSP system performance as well as the capability of working under a wide range of frequencies without being affected by the sampling and computation time limitations of the DSP as illustrated earlier in Sect. 3. In addition, the DSP generation of the reference signals is still necessary since the proposed implementation of the FPGA/DSP design can be considered as a reference

framework for improving and developing commonly used DSP systems for different topologies for future usage.

It is worth mentioning that the main experimental parameters are shown in Table 4. Meanwhile, due to hardware limitations, the DC-link voltage is reduced to 100 V for testing purposes, which can be extended to future works. This method is also verified in the experimental testing of other topologies in many studies as shown in [31–33]. The results of running the system are shown in Fig. 12. In Fig. 12a, the switching of the inverter is shown for the IGBT and the MOSFET at 50 Hz and 30 kHz, respectively. Figure 12b shows the line-to-line voltage ( $V_{ab}$ ) and the pole voltage ( $V_a$ ). As clarified in Sect. 2, one of the main features of the HANPC is that there is no need to balance the switching losses among all of the switches. The IGBT switching devices are limited to lower frequencies with less capability to withstand higher operating temperatures when compared to MOSFET switching devices.

## 5 Conclusions

In this study, the hardware implementation of an FPGA along with a DSP is illustrated and explained. The main advantages of using the FPGA over the DSP are highlighted and clarified. In addition, the working principle of



**Fig. 12** Experimental results of: **a** switching PWM signals; **b** line-to-line voltage ( $V_{ab}$ ) and pole voltage ( $V_{an}$ )

the algorithm implementation is explained in detail. The FPGA displays higher speed in processing the algorithm with greater flexibility in addition to the possibility of simultaneously multitasking (operations). The proposed hardware configuration is verified on a Vivado simulation and an experimental setup, where the FPGA showed high effectiveness and robust performance. The outcomes of this study can be used as a reference guideline for future developments in controlling multi-level inverters and motor drive applications as well as developing standalone FPGA systems.

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